USB Power Manager with Li-Ion Charger and Three Step-Down Regulators

FEATURES

- **Seamless Transition Between Input Power Sources: Li-Ion Battery, USB, 5V Wall Adapter or High Voltage Buck Regulator with Bat-Track™**
- **200mΩ Internal Ideal Diode Plus Optional External Ideal Diode Controller Provides Low Loss Power Path When Input Current is Limited or Unavailable**
- **Triple Adjustable High Efficiency Step-Down Switching Regulators (600mA, 400mA, 400mA I_{OUT})**
- Pin Selectable Burst Mode® Operation
- Full Featured Li-Ion/Polymer Battery Charger
- 1.5A Maximum Charge Current with Thermal Limiting
- Battery Float Voltage:
  - 4.2V (LTC3557)
  - 4.1V (LTC3557-1)
- Low Profile 4mm × 4mm 28-Pin QFN Package

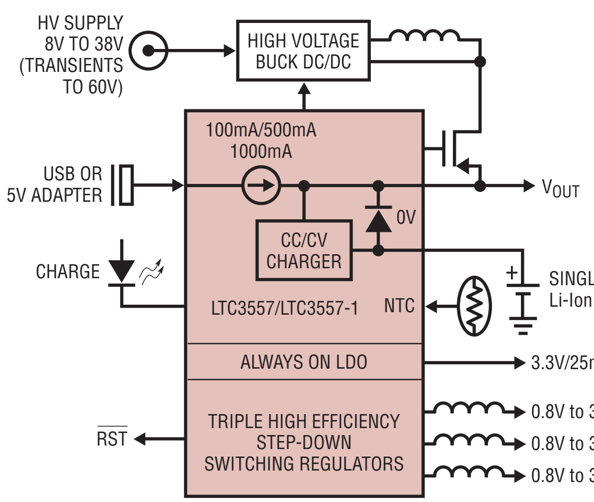
APPLICATIONS

- HDD-Based MP3 Players
- PDA, PMP, PND/GPS
- USB-Based Handheld Products

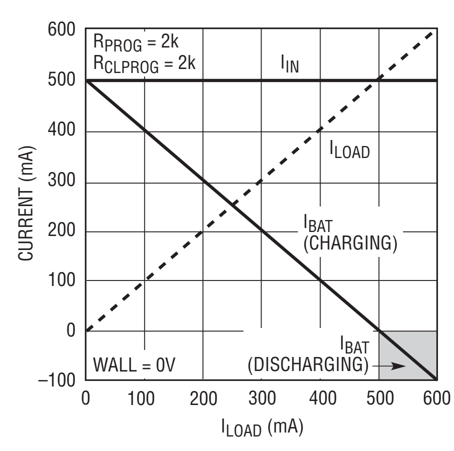
DESCRIPTION

The LTC®3557/LTC3557-1 is a highly integrated power management and battery charger IC for single cell Li-Ion/Polymer battery applications. It includes a PowerPath™ manager with automatic load prioritization, a battery charger, an ideal diode and numerous internal protection features. Designed specifically for USB applications, the LTC3557/LTC3557-1 power manager automatically limits input current to a maximum of either 100mA or 500mA for USB applications or 1A for wall adapter powered applications. Battery charge current is automatically reduced such that the sum of the load current and the charge current does not exceed the programmed input current limit. The LTC3557/LTC3557-1 also includes three adjustable synchronous step-down switching regulators and a high voltage buck regulator output controller with Bat-Track that allows efficient charging from supplies as high as 38V. The LTC3557/LTC3557-1 is available in a low profile 4mm x 4mm x 0.75mm 28-pin QFN package.

TYPICAL APPLICATION



Input and Battery Current vs Load Current



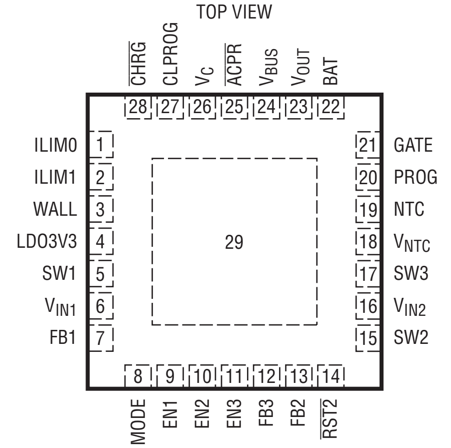
ABSOLUTE MAXIMUM RATINGS

(Notes 1-4)

V_{BUS}, V_{OUT}, V_{IN1}, V_{IN2}
- t < 1ms and Duty Cycle < 1% .... –0.3V to 7V
- Steady State... –0.3V to 6V

BAT, NTC, $\overline{CHRG}$, WALL, V_C,
MODE, FB1, FB2, FB3, $\overline{RST2}$....................... –0.3V to 6V
EN1, EN2, EN3 ....–0.3V to V_{OUT} + 0.3V
ILIM0, ILIM1, PROG ....–0.3V to V_{CC} + 0.3V
I_{VBUS}, I_{VOUT}, I_{BAT} 2A
I_{SW1} 850mA
I_{SW2}, I_{SW3} 600mA
$I_{\overline{RST2}}$, $I_{\overline{CHRG}}$, $I_{\overline{ACPR}}$ 75mA
I_{CLPROG}, I_{PROG}..2mA
Maximum Operating Junction Temperature .... 110°C
Operating Ambient Temperature Range ... –40°C to 85°C
Storage Temperature Range................... –65°C to 125°C

PIN CONFIGURATION



UF PACKAGE
28-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 110°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3557EUF#PBF	LTC3557EUF#TRPBF	3557	28-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C
LTC3557EUF-1#PBF	LTC3557EUF-1#TRPBF	35571	28-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

POWER MANAGER ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{BUS} = 5V, V_{BAT} = 3.8V, ILIM0 = ILIM1 = 5V, WALL = EN1 = EN2 = EN3 = 0V, R_{PROG} = 2k, R_{CLPROG} = 2.1k.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Power Supply							
V_{BUS}	Input Supply Voltage			4.35		5.5	V
$I_{BUS(LIM)}$	Total Input Current (Note 5)	ILIM0 = 0V, ILIM1 = 0V (1x Mode) ILIM0 = 5V, ILIM1 = 5V (5x Mode) ILIM0 = 5V, ILIM1 = 0V (10x Mode)	 ● ●	80 450 900	90 475 950	100 500 1000	mA mA mA
I_{BUSQ}	Input Quiescent Current	1x, 5x, 10x Modes ILIM0 = 0V, ILIM1 = 5V (Suspend Mode)			0.35 0.05	 0.1	mA mA
h_{CLPROG}	Ratio of Measured V_{BUS} Current to CLPROG Program Current	1x, 5x, 10x Modes			1000		mA/mA
V_{CLPROG}	CLPROG Servo Voltage in Current Limit	1x Mode 5x Mode 10x Mode			0.2 1.0 2.0		V V V
V_{UVLO}	V_{BUS} Undervoltage Lockout	Rising Threshold Falling Threshold		 3.5	3.8 3.7	3.9	V V

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DUVLO}	V_{BUS} to V_{OUT} Differential Undervoltage Lockout	Rising Threshold Falling Threshold			50 –50	100	mV mV
R_{ON_LIM}	Input Current Limit Power FET On-Resistance (Between V_{BUS} and V_{OUT})				0.2		Ω
Battery Charger							
V_{FLOAT}	V_{BAT} Regulated Output Voltage	LTC3557 LTC3557, 0°C ≤ T_A ≤ 85°C LTC3557-1 LTC3557-1, 0°C ≤ T_A ≤ 85°C		4.179 4.165 4.079 4.065	4.200 4.200 4.100 4.100	4.221 4.235 4.121 4.135	V V V V
I_{CHG}	Constant Current Mode Charge Current	R_{PROG} = 1k, Input Current Limit = 2A R_{PROG} = 2k, Input Current Limit = 1A R_{PROG} = 5k, Input Current Limit = 400mA	● ● ●	950 465 180	1000 500 200	1050 535 220	mA mA mA
I_{BAT}	Battery Drain Current	V_{BUS} > V_{UVLO}, Charger Off, I_{OUT} = 0µA V_{BUS} = 0V, I_{OUT} = 0µA (Ideal Diode Mode)			6 55	27 100	µA µA
V_{PROG} $V_{PROG(TRKL)}$	PROG Pin Servo Voltage PROG Pin Servo Voltage in Trickle Charge	 BAT < V_{TRKL}			1.000 0.100		V V
h_{PROG}	Ratio of I_{BAT} to PROG Pin Current				1000		mA/mA
I_{TRKL}	Trickle Charge Current	BAT < V_{TRKL}		40	50	60	mA
V_{TRKL}	Trickle Charge Rising Threshold Trickle Charge Falling Threshold	BAT Rising BAT Falling		 2.5	2.85 2.75	3.0	V V
ΔV_{RECHRG}	Recharge Battery Threshold Voltage	Threshold Voltage Relative to V_{FLOAT}		–75	–100	–115	mV
t_{TERM}	Safety Timer Termination Period	Timer Starts when BAT = V_{FLOAT} – 50mV		3.2	4	4.8	Hour
t_{BADBAT}	Bad Battery Termination Time	BAT < V_{TRKL}		0.4	0.5	0.6	Hour
$h_{C/10}$	End-of-Charge Indication Current Ratio	(Note 6)		0.085	0.1	0.115	mA/mA
$R_{ON(CHG)}$	Battery Charger Power FET On-Resistance (Between V_{OUT} and BAT)				200		mΩ
T_{LIM}	Junction Temperature in Constant Temperature Mode				110		°C
NTC							
V_{COLD}	Cold Temperature Fault Threshold Voltage	Rising NTC Voltage Hysteresis		75	76 1.3	77	%V_{VNTC} %V_{VNTC}
V_{HOT}	Hot Temperature Fault Threshold Voltage	Falling NTC Voltage Hysteresis		34	35 1.3	36	%V_{VNTC} %V_{VNTC}
V_{DIS}	NTC Disable Threshold Voltage	Falling NTC Voltage Hysteresis	●	1.2	1.7 50	2.2	%V_{VNTC} mV
I_{NTC}	NTC Leakage Current	NTC = V_{BUS} = 5V		–50		50	nA
Ideal Diode							
V_{FWD}	Forward Voltage Detection	I_{OUT} = 10mA		5	15	25	mV
$R_{DROPOUT}$	Diode On-Resistance, Dropout	I_{OUT} = 1A			200		mΩ
I_{MAX}	Diode Current Limit	(Note 7)			3.6		A
Always On 3.3V Supply							
V_{LDO3V3}	Regulated Output Voltage	0mA < I_{LDO3V3} < 25mA		3.1	3.3	3.5	V
$R_{OL(LDO3V3)}$	Open-Loop Output Resistance	BAT = 3.0V, V_{BUS} = 0V			24		Ω
$R_{CL(LDO3V3)}$	Closed-Loop Output Resistance				3.2		Ω

POWER MANAGER ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Wall Adapter							
$V_{\overline{ACPR}}$	$\overline{\text{ACPR}}$ Pin Output High Voltage $\overline{\text{ACPR}}$ Pin Output Low Voltage	$I_{\overline{ACPR}}$ = 1mA $I_{\overline{ACPR}}$ = 1mA		V_{OUT}–0.3	V_{OUT} 0	 0.3	V V
V_W	Absolute Wall Input Threshold Voltage	WALL Rising WALL Falling		 3.1	4.3 3.2	4.45	V V
ΔV_W	Differential Wall Input Threshold Voltage	WALL – BAT Falling WALL – BAT Rising		0	25 75	 150	mV mV
I_{QWALL}	Wall Operating Quiescent Current	I_{WALL} + I_{VOUT}, I_{BAT} = 0mA, WALL = V_{OUT} = 5V			440		µA
Logic (I_{LIM0}, I_{LIM1} and $\overline{\text{CHRG}}$)							
V_{IL}	Input Low Voltage	ILIM0, ILIM1				0.4	V
V_{IH}	Input High Voltage	ILIM0, ILIM1		1.2			V
I_{PD}	Static Pull-Down Current	ILIM0, ILIM1; V_{PIN} = 1V			2		µA
$V_{\overline{CHRG}}$	$\overline{\text{CHRG}}$ Pin Output Low Voltage	$I_{\overline{CHRG}}$ = 10mA			0.15	0.4	V
$I_{\overline{CHRG}}$	$\overline{\text{CHRG}}$ Pin Input Current	BAT = 4.5V, $\overline{\text{CHRG}}$ = 5V			0	1	µA

SWITCHING REGULATOR ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{OUT} = V_{IN1} = V_{IN2} = 3.8V, MODE = EN1 = EN2 = EN3 = 0V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Step-Down Switching Regulators 1, 2 and 3							
V_{IN1}, V_{IN2}	Input Supply Voltage	(Note 10)	●	2.7		5.5	V
V_{OUT} UVLO	V_{OUT} Falling V_{OUT} Rising	V_{IN1} and V_{IN2} Connected to V_{OUT} Through Low Impedance. Switching Regulators are Disabled Below V_{OUT} UVLO		2.5	2.7 2.8	 2.9	V V
f_{OSC}	Oscillator Frequency			1.91	2.25	2.59	MHz
V_{IL}	Input Low Voltage	MODE, EN1, EN2, EN3				0.4	V
V_{IH}	Input High Voltage	MODE, EN1, EN2, EN3		1.2			V
I_{PD}	Static Pull-Down Current	MODE, EN1, EN2, EN3 (V_{PIN} = 1V)			1		µA
Step-Down Switching Regulator 1							
I_{VIN1}	Pulse-Skip Mode Input Current (Note 11)	I_{OUT} = 0, EN1 = 3.8V, MODE = 0V			220		µA
	Burst Mode Input Current (Note 11)	I_{OUT} = 0, EN1 = MODE = 3.8V			35	50	µA
	Shutdown Input Current	I_{OUT} = 0, EN1 = 0V, FB1 = 0V			0.01	1	µA
I_{LIM1}	Peak PMOS Current Limit	EN1 = 3.8V, MODE = 0V or 3.8V (Note 7)		900	1200	1500	mA
V_{FB1}	Feedback Voltage	EN1 = 3.8V, MODE = 0V EN1 = MODE = 3.8V	● ●	0.78 0.78	0.8 0.8	0.82 0.824	V V
I_{FB1}	FB1 Input Current (Note 11)	EN1 = 3.8V		–0.05		0.05	µA
D1	Maximum Duty Cycle	FB1 = 0V, EN1 = 3.8V		100			%
R_{P1}	$R_{DS(ON)}$ of PMOS	EN1 = 3.8V			0.3		Ω
R_{N1}	$R_{DS(ON)}$ of NMOS	EN1 = 3.8V			0.4		Ω
$R_{SW1(PD)}$	SW1 Pull-Down in Shutdown	EN1 = 0V			10		kΩ

SWITCHING REGULATOR ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{OUT} = V_{IN1} = V_{IN2} = 3.8V, MODE = EN1 = EN2 = EN3 = 0V.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Step-Down Switching Regulator 2							
I_{VIN2}	Pulse-Skip Mode Input Current (Note 11)	I_{OUT} = 0, EN2 = 3.8V, MODE = 0V			220		µA
	Burst Mode Input Current (Note 11)	I_{OUT} = 0, EN2 = MODE = 3.8V			35	50	µA
	Shutdown Input Current	I_{OUT} = 0, EN2 = 0V, FB2 = 0V			0.01	1	µA
I_{LIM2}	Peak PMOS Current Limit	EN2 = 3.8V, MODE = 0V or 3.8V (Note 7)		600	800	1000	mA
V_{FB2}	Feedback Voltage	EN2 = 3.8V, MODE = 0V EN2 = MODE = 3.8V	● ●	0.78 0.78	0.8 0.8	0.82 0.824	V V
I_{FB2}	FB2 Input Current (Note 11)	EN2 = 3.8V		–0.05		0.05	µA
D2	Maximum Duty Cycle	FB2 = 0V, EN2 = 3.8V		100			%
R_{P2}	$R_{DS(ON)}$ of PMOS	EN2 = 3.8V			0.6		Ω
R_{N2}	$R_{DS(ON)}$ of NMOS	EN2 = 3.8V			0.6		Ω
$R_{SW2(PD)}$	SW2 Pull-Down in Shutdown	EN2 = 0V			10		kΩ
$V_{\overline{RST2}}$	Power-On $\overline{RST2}$ Pin Output Low Voltage	$I_{\overline{RST2}}$ = 1mA, FB2 = 0V, EN2 = 3.8V			0.1	0.35	V
$I_{\overline{RST2}}$	Power-On $\overline{RST2}$ Pin Input Current (Note 11)	$V_{\overline{RST2}}$ = 5.5V, EN2 = 3.8V				1	µA
$V_{TH(\overline{RST2})}$	Power-On $\overline{RST2}$ Pin Threshold	(Note 9)			–8		%
$t_{\overline{RST2}}$	Power-On $\overline{RST2}$ Pin Delay	From $\overline{RST2}$ Threshold to $\overline{RST2}$ Hi-Z			230		ms
Step-Down Switching Regulator 3							
I_{VIN2}	Pulse-Skip Mode Input Current (Note 11)	I_{OUT} = 0, EN3 = 3.8V, MODE = 0V			220		µA
	Burst Mode Input Current (Note 11)	I_{OUT} = 0, EN3 = MODE = 3.8V			35	50	µA
	Shutdown Input current	I_{OUT} = 0, EN3 = 0V, FB3 = 0V			0.01	1	µA
I_{LIM3}	Peak PMOS Current Limt	EN3 = 3.8V, MODE = 0V or 3.8V (Note 7)		600	800	1000	mA
V_{FB3}	Feedback Voltage	EN3 = 3.8V, MODE = 0V EN3 = MODE = 3.8V	● ●	0.78 0.78	0.8 0.8	0.82 0.824	V V
I_{FB3}	FB3 Input Current (Note 11)	EN3 = 3.8V		–0.05		0.05	µA
D3	Maximum Duty Cycle	FB3 = 0V, EN3 = 3.8V		100			%
R_{P3}	$R_{DS(ON)}$ of PMOS	EN3 = 3.8V			0.6		Ω
R_{N3}	$R_{DS(ON)}$ of NMOS	EN3 = 3.8V			0.6		Ω
$R_{SW3(PD)}$	SW3 Pull-Down in Shutdown	EN3 = 0V			10		kΩ

Note 1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. The LTC3557/LTC3557-1 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3. This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperatures will exceed 110°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

Note 4. V_{CC} is the greater of V_{BUS}, V_{OUT} or BAT.

Note 5. Total input current is the sum of quiescent current, I_{BUSQ}, and measured current given by $V_{CLPROG}/R_{CLPROG} \cdot (h_{CLPROG} + 1)$

Note 6. $h_{C/10}$ is expressed as a fraction of measured full charge current with indicated PROG resistor.

Note 7. The current limit features of this part are intended to protect the IC from short term or intermittent fault conditions. Continuous operation above the maximum specified pin current rating may result in device degradation or failure.

Note 8. Inductor series resistance adds to open-loop R_{OUT}.

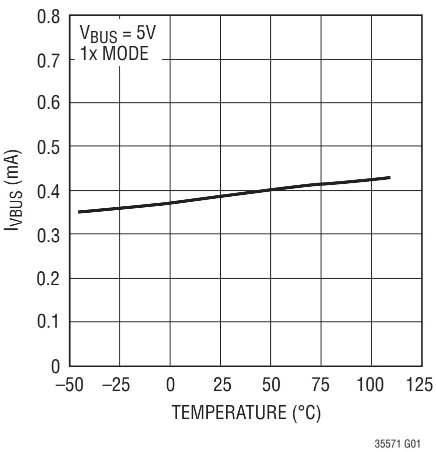
Note 9. $\overline{RST2}$ threshold is expressed as a percentage difference from the FB2 regulation voltage. The threshold is measured for FB2 rising.

Note 10. V_{OUT} not in UVLO.

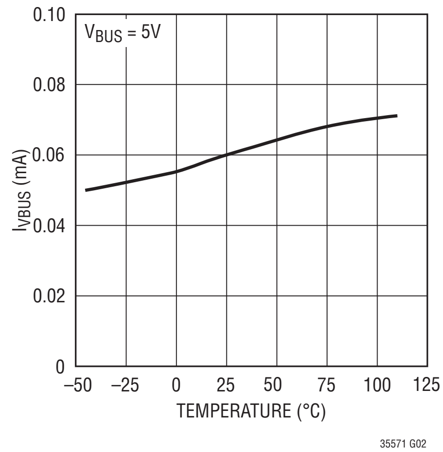
Note 11. FB high, not switching.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified

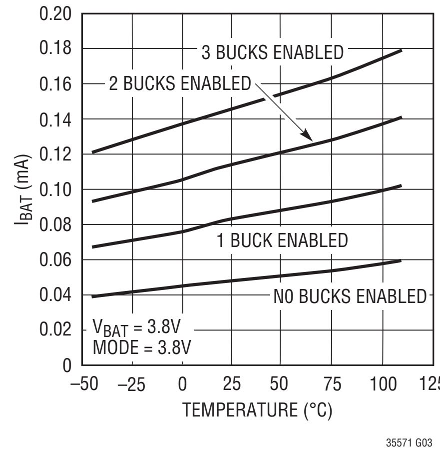
Input Supply Current vs Temperature



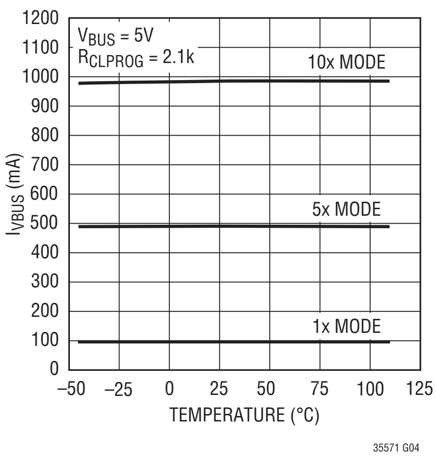
Input Supply Current vs Temperature (Suspend Mode)



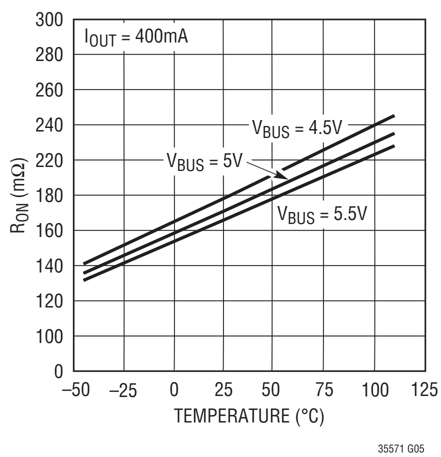
Battery Drain Current vs Temperature



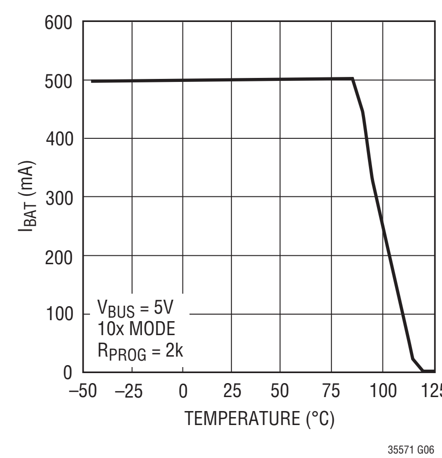
Input Current Limit vs Temperature



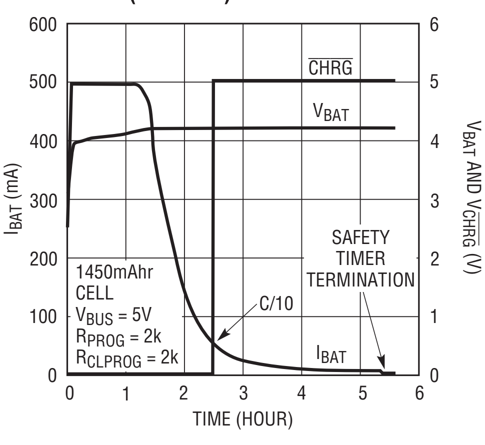
Input R_{ON} vs Temperature



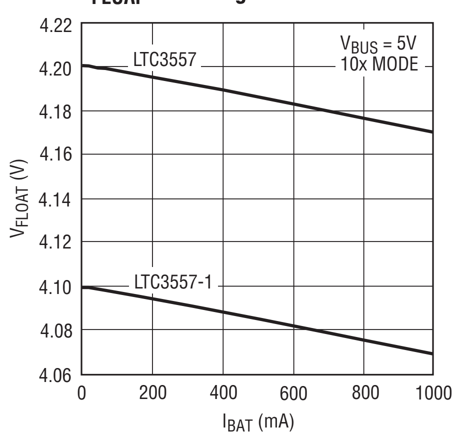
Charge Current vs Temperature (Thermal Regulation)



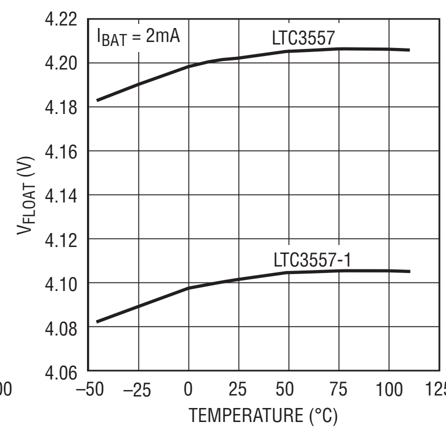
Battery Current and Voltage vs Time (LTC3557)



V_{FLOAT} Load Regulation

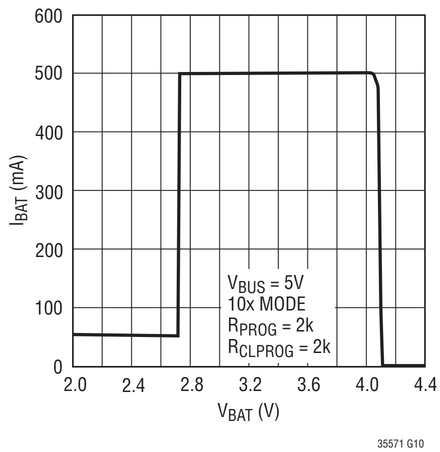


Battery Regulation (Float) Voltage vs Temperature

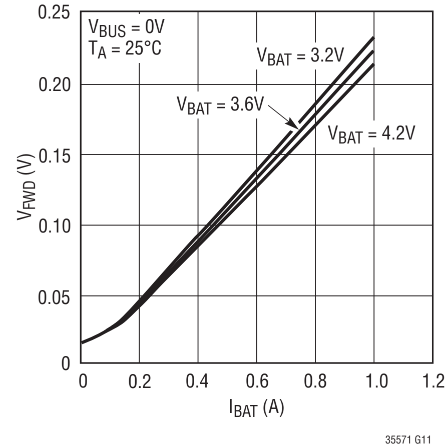


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified

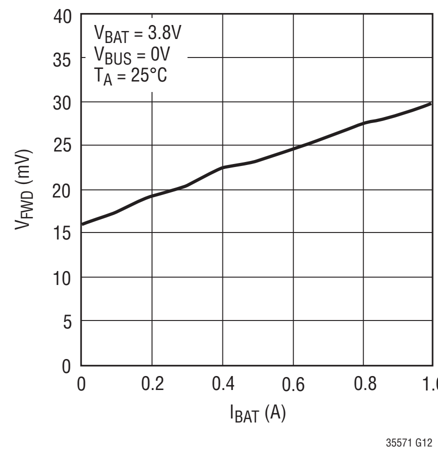
I_{BAT} vs V_{BAT}



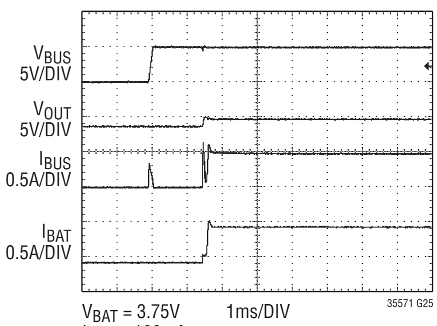
Forward Voltage vs Ideal Diode Current (No External FET)



Forward Voltage vs Ideal Diode Current (with Si2333DS External FET)

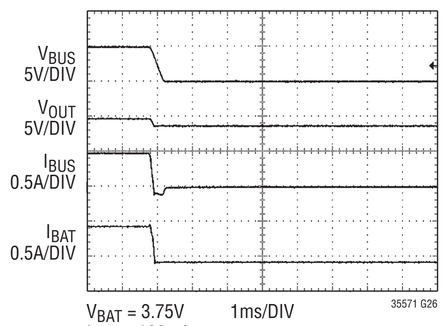


Input Connect Waveform



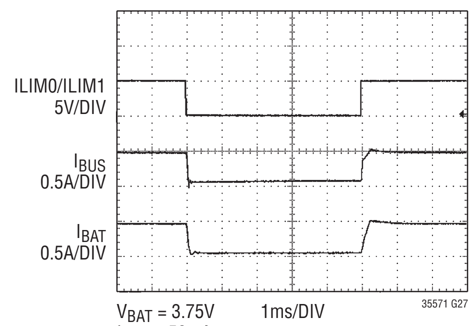
V_{BAT} = 3.75V 1ms/DIV
I_{OUT} = 100mA
R_{CLPROG} = 2k
R_{PROG} = 2k

Input Disconnect Waveform



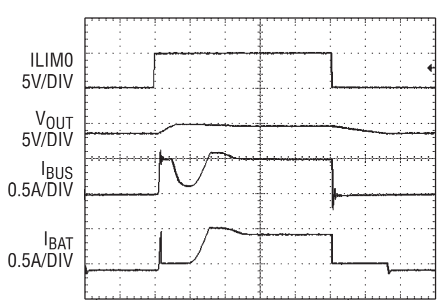
V_{BAT} = 3.75V 1ms/DIV
I_{OUT} = 100mA
R_{CLPROG} = 2k
R_{PROG} = 2k

Switching from 1x to 5x Mode



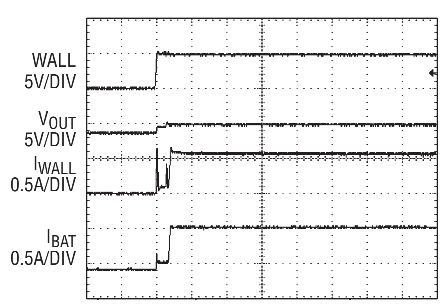
V_{BAT} = 3.75V 1ms/DIV
I_{OUT} = 50mA
R_{CLPROG} = 2k
R_{PROG} = 2k

Switching from Suspend Mode to 5x Mode



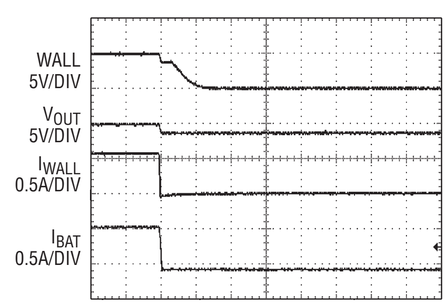
V_{BAT} = 3.75V 100μs/DIV
I_{OUT} = 100mA
R_{CLPROG} = 2k
R_{PROG} = 2k
ILIM1 = 5V

WALL Connect Waveform



V_{BAT} = 3.75V 1ms/DIV
I_{OUT} = 100mA
R_{PROG} = 2k

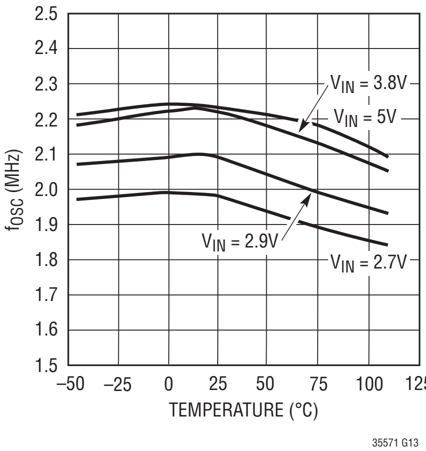
WALL Disconnect Waveform



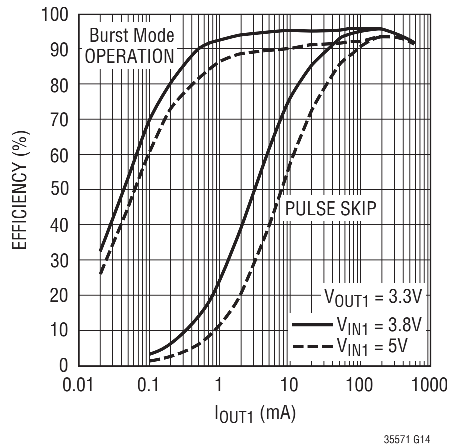
V_{BAT} = 3.75V 1ms/DIV
I_{OUT} = 100mA
R_{PROG} = 2k

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$ unless otherwise specified

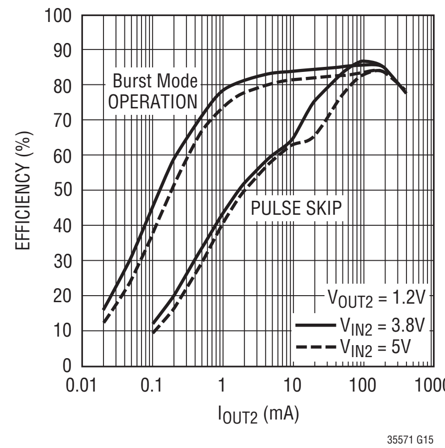
Oscillator Frequency vs Temperature



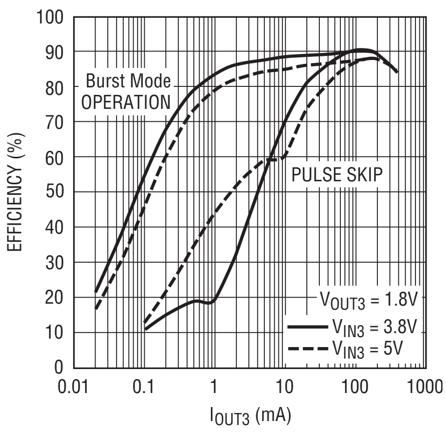
Step-Down Switching Regulator 1 3.3V Output Efficiency vs I_{OUT1}



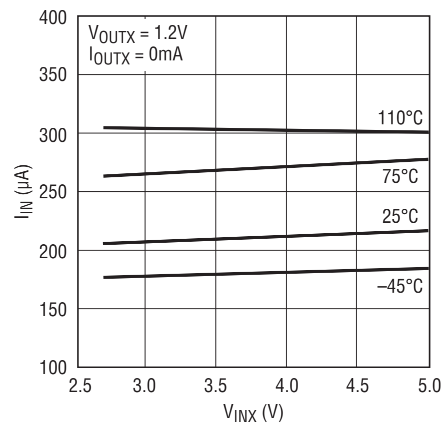
Step-Down Switching Regulator 2 1.2V Output Efficiency vs I_{OUT2}



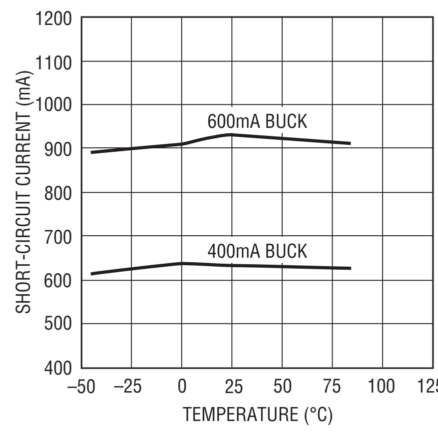
Step-Down Switching Regulator 3 1.8V Output Efficiency vs I_{OUT3}



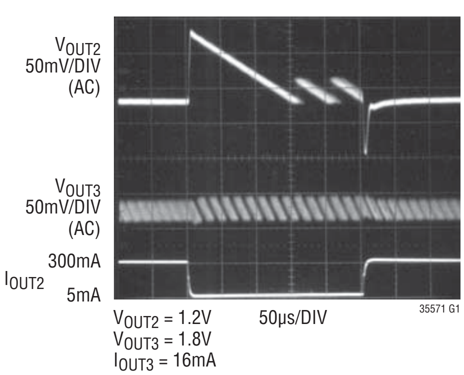
Step-Down Switching Regulator Pulse Skip Supply Current vs V_{INX}



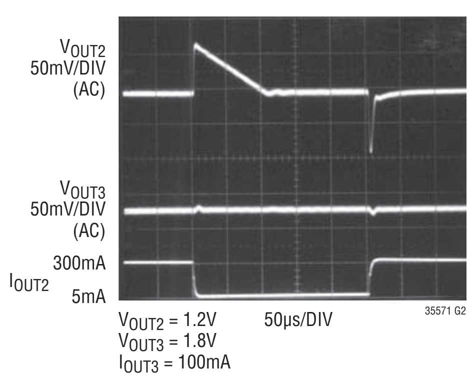
Step-Down Switching Regulator Short-Circuit Current vs Temperature



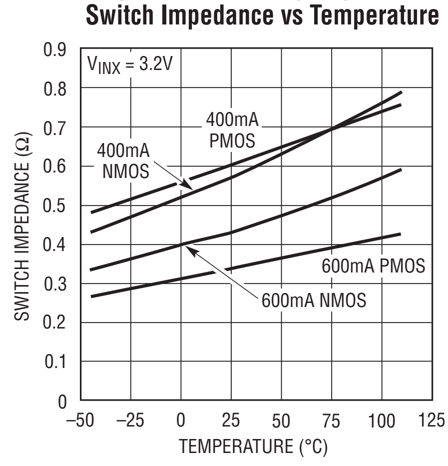
Step-Down Switching Regulator Output Transient (MODE = 1)



Step-Down Switching Regulator Output Transient (MODE = 0)

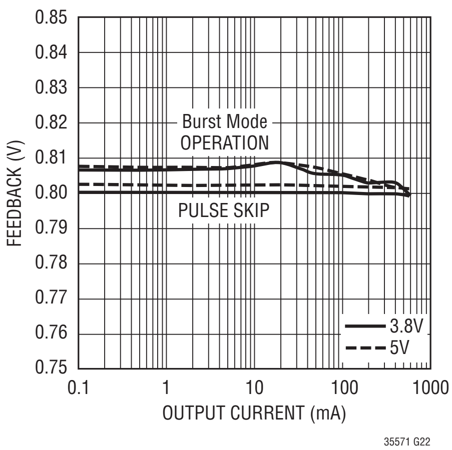


Step-Down Switching Regulator Switch Impedance vs Temperature

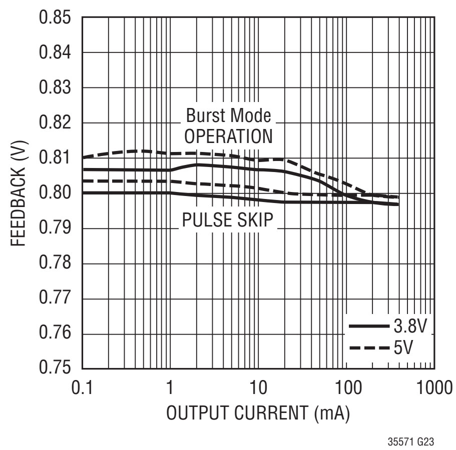


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified

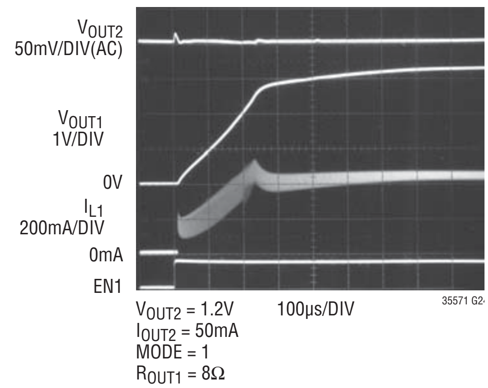
600mA Step-Down Switching Regulator Feedback Voltage vs Output Current



400mA Step-Down Switching Regulator Feedback Voltage vs Output Current



Step-Down Switching Regulator Start-Up Waveform



PIN FUNCTIONS

ILIM0, ILIM1 (Pins 1, 2): Input Current Control Pins. ILIM0 and ILIM1 control the input current limit. See Table 1. Both pins are pulled low by a weak current sink.

WALL (Pin 3): Wall Adapter Present Input. Pulling this pin above 4.3V will disconnect the power path from V_{BUS} to V_{OUT}. The $\overline{ACPR}$ pin will also be pulled low to indicate that a wall adapter has been detected.

LDO3V3 (Pin 4): Always On 3.3V LDO Output. The LDO3V3 pin provides a regulated, always-on 3.3V supply voltage. This pin gets its power from V_{OUT}. It may be used for light loads such as a real-time clock or housekeeping microprocessor. A 1µF capacitor is required from LDO3V3 to ground if it will be called upon to deliver current. If the LDO3V3 output is not used it should be disabled by connecting it to V_{OUT}.

SW1 (Pin 5): Power Transmission (Switch) Pin for Step-Down Switching Regulator 1.

V_{IN1} (Pin 6): Power Input for Step-Down Switching Regulator 1. This pin will generally be connected to V_{OUT}.

FB1 (Pin 7): Feedback Input for Step-Down Switching Regulator 1. This pin servos to a fixed voltage of 0.8V when the control loop is complete.

MODE (Pin 8): Low Power Mode Enable. When this pin is pulled high, the three step-down switching regulators are set to low power Burst Mode operation.

EN1 (Pin 9): Logic Input Enables Step-Down Switching Regulator 1.

EN2 (Pin 10): Logic Input Enables Step-Down Switching Regulator 2.

EN3 (Pin 11): Logic Input Enables Step-Down Switching Regulator 3.

FB3 (Pin 12): Feedback Input for Step-Down Switching Regulator 3. This pin servos to a fixed voltage of 0.8V when the control loop is complete.

FB2 (Pin 13): Feedback Input for Step-Down Switching Regulator 2. This pin servos to a fixed voltage of 0.8V when the control loop is complete.

$\overline{RST2}$ (Pin 14): This is an open-drain output which indicates that step-down switching regulator 2 has settled to its final value. It can be used as a power on reset for the primary microprocessor or to enable the other buck regulators for supply sequencing.

SW2 (Pin 15): Power Transmission (Switch) Pin for Step-Down Switching Regulator 2.

PIN FUNCTIONS

V_{IN2} (Pin 16): Power Input for Step-Down Switching Regulators 2 and 3. This pin will generally be connected to V_{OUT}.

SW3 (Pin 17): Power Transmission (Switch) Pin for Step-Down Switching Regulator 3.

V_{NTC} (Pin 18): Output Bias Voltage for NTC. A resistor from this pin to the NTC pin will bias the NTC thermistor.

NTC (Pin 19): The NTC pin connects to a battery's thermistor to determine if the battery is too hot or too cold to charge. If the battery's temperature is out of range, charging is paused until it drops back into range. A low drift bias resistor is required from V_{NTC} to NTC and a thermistor is required from NTC to ground. If the NTC function is not desired, the NTC pin should be grounded.

PROG (Pin 20): Charge Current Program and Charge Current Monitor Pin. Connecting a resistor from PROG to ground programs the charge current:

$$I_{CHG}(A) = \frac{1000V}{R_{PROG}}$$

If sufficient input power is available in constant current mode, this pin servos to 1V. The voltage on this pin always represents the actual charge current.

GATE (Pin 21): Ideal Diode Gate Connection. This pin controls the gate of an optional external P-channel MOSFET transistor used to supplement the internal ideal diode. The source of the P-channel MOSFET should be connected to V_{OUT} and the drain should be connected to BAT. It is important to maintain high impedance on this pin and minimize all leakage paths.

BAT (Pin 22): Single Cell Li-Ion Battery Pin. Depending on available power and load, a Li-Ion battery on BAT will either deliver system power to V_{OUT} through the ideal diode or be charged from the battery charger.

V_{OUT} (Pin 23): Output Voltage of the PowerPath Controller and Input Voltage of the Battery Charger. The majority of the portable product should be powered from V_{OUT}. The LTC3557/LTC3557-1 will partition the available power between the external load on V_{OUT} and the internal battery charger. Priority is given to the external load and any extra power is used to charge the battery. An ideal diode from BAT to V_{OUT} ensures that V_{OUT} is powered even if the load exceeds the allotted input current from V_{BUS} or if the V_{BUS} power source is removed. V_{OUT} should be bypassed with a low impedance multilayer ceramic capacitor. The total capacitance on V_{OUT} should maintain a minimum of TBDμF over operating voltage and temperature.

V_{BUS} (Pin 24): USB Input Voltage. V_{BUS} will usually be connected to the USB port of a computer or a DC output wall adapter. V_{BUS} should be bypassed with a low impedance multilayer ceramic capacitor.

$\overline{\text{ACPR}}$ (Pin 25): Wall Adapter Present Output (Active Low). A low on this pin indicates that the wall adapter input comparator has had its input pulled above its input threshold (typically 4.3V). This pin can be used to drive the gate of an external P-channel MOSFET to provide power to V_{OUT} from a power source other than a USB port.

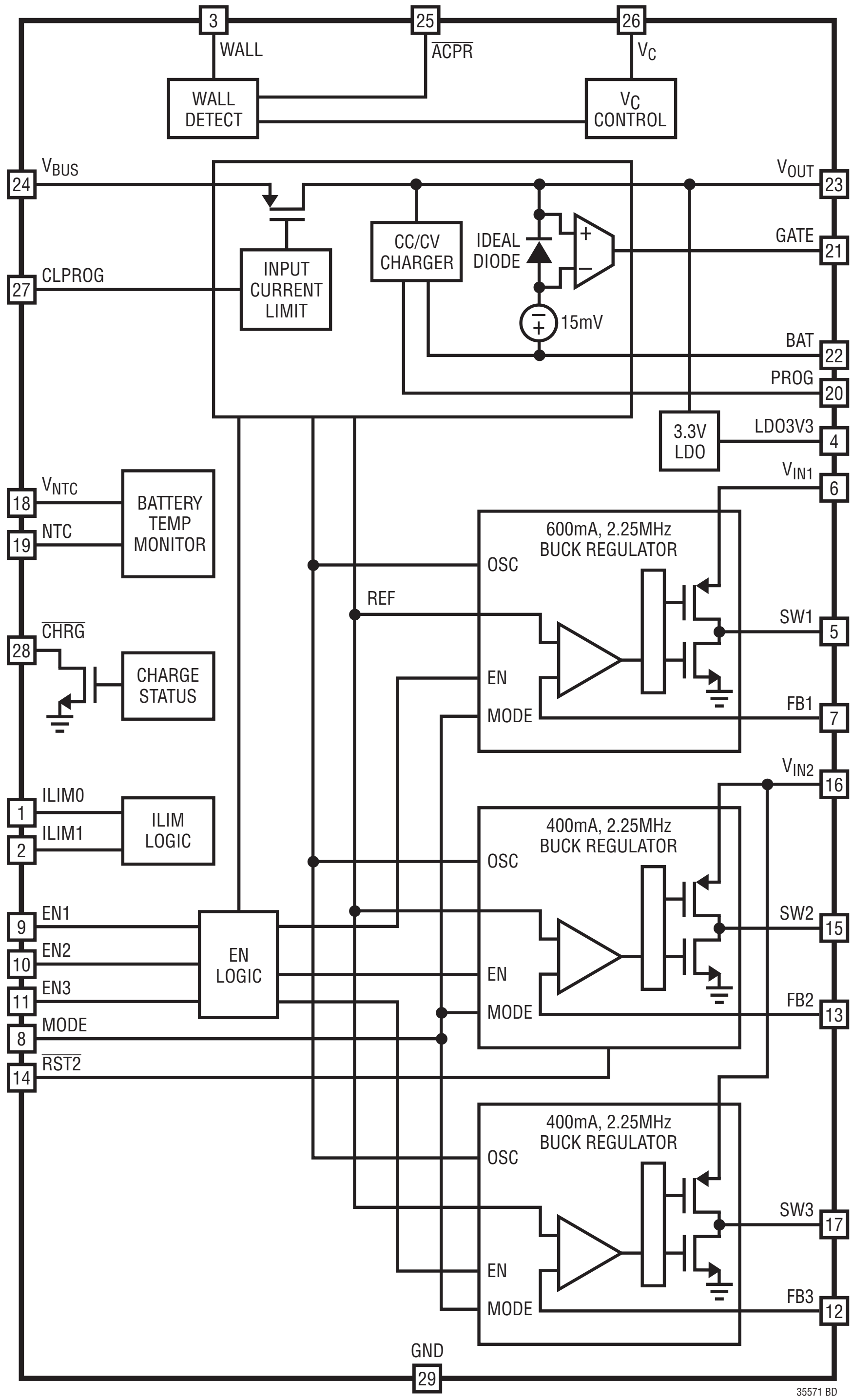
V_C (Pin 26): High Voltage Buck Regulator Control Pin. This pin can be used to drive the V_C pin of an approved external high voltage buck switching regulator. An external P-channel MOSFET is required to provide power to V_{OUT} with its gate tied to the $\overline{\text{ACPR}}$ pin. The V_C pin is designed to work with the LT®3480, LT3481 and LT3505.

CLPROG (Pin 27): Input Current Program and Input Current Monitor Pin. A resistor from CLPROG to ground determines the upper limit of the current drawn from the V_{BUS} pin (i.e., the input current limit). A precise fraction of the input current, h_{CLPROG}, is sent to the CLPROG pin. The input PowerPath delivers current until the CLPROG pin reaches 2.0V (10x Mode), 1.0V (5x Mode) or 0.2V (1x Mode). Therefore, the current drawn from V_{BUS} will be limited to an amount given by h_{CLPROG} and R_{CLPROG}. In USB applications the resistor R_{CLPROG} should be set to no less than 2.1k.

$\overline{\text{CHRG}}$ (Pin 28): Open-Drain Charge Status Output. The $\overline{\text{CHRG}}$ pin indicates the status of the battery charger. Four possible states are represented by $\overline{\text{CHRG}}$: charging, not charging (i.e., float charge current less than 1/10th programmed charge current), unresponsive battery (i.e., its voltage remains below 2.8V after 1/2 hour of charging) and battery temperature out of range. $\overline{\text{CHRG}}$ requires a pull-up resistor and/or LED to provide indication.

Exposed Pad (Pin 29): Ground. The exposed package pad is ground and must be soldered to the PC board for proper functionality and for maximum heat transfer.

BLOCK DIAGRAM



OPERATION

Introduction

The LTC3557/LTC3557-1 is a highly integrated power management IC that includes a PowerPath controller, battery charger, an ideal diode, an always-on LDO, three synchronous step-down switching regulators as well as a buck regulator V_C controller. Designed specifically for USB applications, the PowerPath controller incorporates a precision input current limit which communicates with the battery charger to ensure that input current never violates the USB specifications.

The ideal diode from BAT to V_{OUT} guarantees that ample power is always available to V_{OUT} even if there is insufficient or absent power at V_{BUS}.

The LTC3557/LTC3557-1 also has the ability to receive power from a wall adapter or other non-current-limited power source. Such a power supply can be connected to the V_{OUT} pin of the LTC3557/LTC3557-1 through an external device such as a power Schottky or FET as shown in Figure 1.

The LTC3557/LTC3557-1 has the unique ability to use the output, which is powered by an external supply, to charge the battery while providing power to the load. A comparator on the WALL pin is configured to detect the presence of the wall adapter and shut off the connection to the USB. This prevents reverse conduction from V_{OUT} to V_{BUS} when a wall adapter is present.

The LTC3557/LTC3557-1 provides a V_C output pin which can be used to drive the V_C pin of an external high voltage buck switching regulator such as the LT3480, LT3481, or LT3505 to provide power to the V_{OUT} pin. The V_C control circuitry adjusts the regulation point of the switching regulator to a small voltage above the BAT pin voltage. This control method provides a high input voltage, high efficiency battery charger and PowerPath function.

An “always on” LDO provides a regulated 3.3V from V_{OUT}. This LDO will be on at all times and can be used to supply up to 25mA.

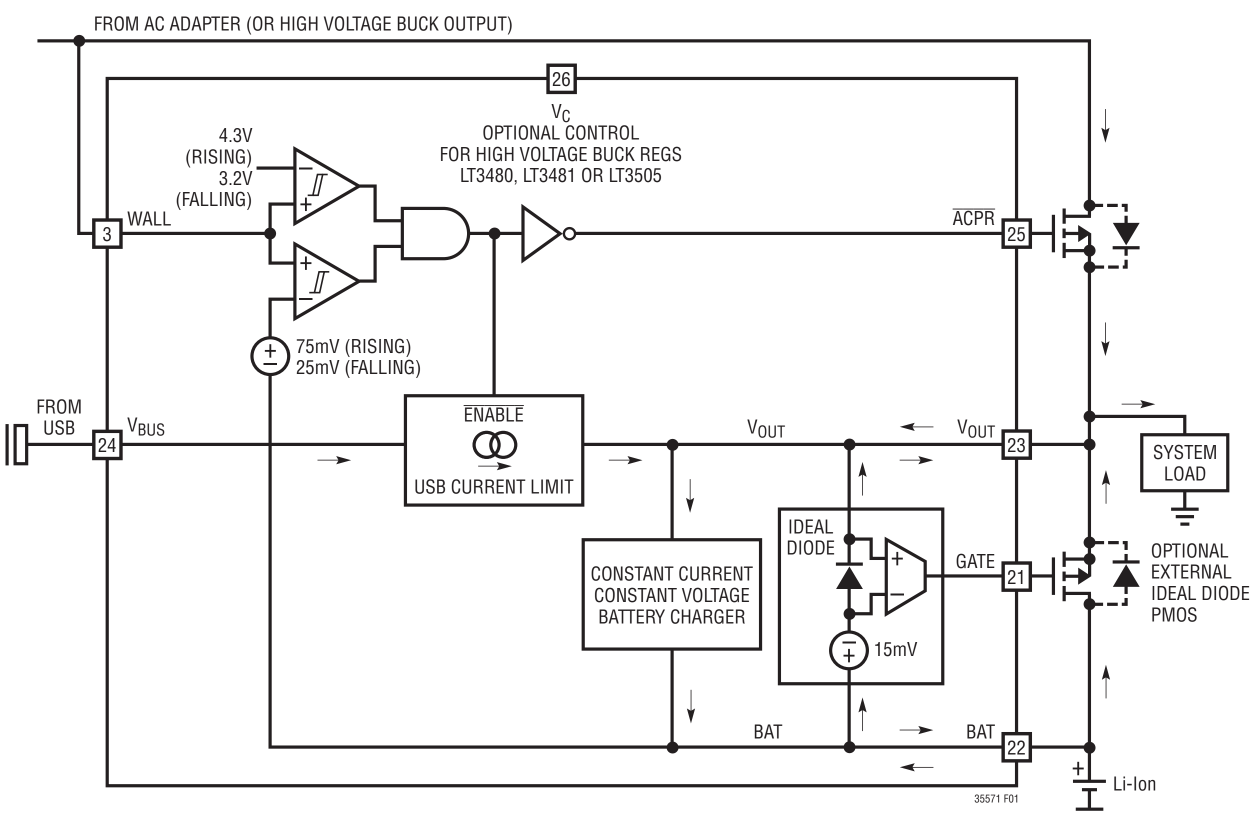


Figure 1. Simplified PowerPath Block Diagram

OPERATION

The LTC3557/LTC3557-1 includes three 2.25MHz constant frequency current mode step-down switching regulators providing 400mA, 400mA and 600mA each. All step-down switching regulators can be programmed for a minimum output voltage of 0.8V and can be used to power a microcontroller core, microcontroller I/O, memory or other logic circuitry. All step-down switching regulators support 100% duty cycle operation and are capable of operating in Burst Mode operation for highest efficiencies at light loads (Burst Mode operation is pin selectable). No external compensation components are required for the switching regulators.

USB PowerPath Controller

The input current limit and charge control circuits of the LTC3557/LTC3557-1 are designed to limit input current as well as control battery charge current as a function of I_{VOUT}. V_{OUT} drives the combination of the external load, the three step-down switching regulators, always on 3.3V LDO and the battery charger.

If the combined load does not exceed the programmed input current limit, V_{OUT} will be connected to V_{BUS} through an internal 200mΩ P-channel MOSFET.

If the combined load at V_{OUT} exceeds the programmed input current limit, the battery charger will reduce its charge current by the amount necessary to enable the external load to be satisfied while maintaining the programmed input current. Even if the battery charge current is set to exceed the allowable USB current, the average input current USB specification will not be violated. Furthermore, load current at V_{OUT} will always be prioritized and only excess available current will be used to charge the battery.

The current out of the CLPROG pin is a fraction ($1/h_{CLPROG}$) of the V_{BUS} current. When a programming resistor is connected from CLPROG to GND, the voltage on CLPROG represents the input current:

$$I_{VBUS} = I_{BUSQ} + \frac{V_{CLPROG}}{R_{CLPROG}} \bullet h_{CLPROG}$$

where I_{BUSQ} and h_{CLPROG} are given in the Electrical Characteristics.

The input current limit is programmed by the ILIM0 and ILIM1 pins. The LTC3557/LTC3557-1 can be configured to limit input current to one of several possible settings as well as be deactivated (USB Suspend). The input current limit will be set by the appropriate servo voltage and the resistor on CLPROG according to the following expression:

$$I_{VBUS} = I_{BUSQ} + \frac{0.2V}{R_{CLPROG}} \bullet h_{CLPROG} \text{ (1x Mode)}$$

$$I_{VBUS} = I_{BUSQ} + \frac{1V}{R_{CLPROG}} \bullet h_{CLPROG} \text{ (5x Mode)}$$

$$I_{VBUS} = I_{BUSQ} + \frac{2V}{R_{CLPROG}} \bullet h_{CLPROG} \text{ (10x Mode)}$$

Under worst-case conditions, the USB specification will not be violated with an R_{CLPROG} resistor of greater than 2.1k.

Table 1 shows the available settings for the I_{LIM0} and I_{LIM1} pins:

Table 1: Controlled Input Current Limit

ILIM1	ILIM0	$I_{BUS(LIM)}$
0	0	100mA (1x)
0	1	1A (10x)
1	0	Suspend
1	1	500mA (5x)

Notice that when ILIM0 is high and ILIM1 is low, the input current limit is set to a higher current limit for increased charging and current availability at V_{OUT}. This mode is typically used when there is power available from a wall adapter.

Ideal Diode from BAT to V_{OUT}

The LTC3557/LTC3557-1 has an internal ideal diode as well as a controller for an optional external ideal diode. Both the internal and the external ideal diodes respond quickly whenever V_{OUT} drops below BAT.

If the load increases beyond the input current limit, additional current will be pulled from the battery via the ideal diodes. Furthermore, if power to V_{BUS} (USB) or V_{OUT} (external wall power or high voltage regulator) is removed, then all of the application power will be provided

OPERATION

by the battery via the ideal diodes. The ideal diodes are fast enough to keep V_{OUT} from dropping with just the recommended output capacitor. The ideal diode consists of a precision amplifier that enables an on-chip P-channel MOSFET whenever the voltage at V_{OUT} is approximately 15mV (V_{FWD}) below the voltage at BAT. The resistance of the internal ideal diode is approximately 210mΩ. If this is sufficient for the application, then no external components are necessary. However, if more conductance is needed, an external P-channel MOSFET can be added from BAT to V_{OUT}.

The GATE pin of the LTC3557/LTC3557-1 drives the gate of the external P-channel MOSFET for automatic ideal diode control. The source of the MOSFET should be connected to V_{OUT} and the drain should be connected to BAT. Capable of driving a 1nF load, the GATE pin can control an external P-channel MOSFET having extremely low on-resistance.

Using the WALL Pin to Detect the Presence of an External Power Source

The WALL input pin can be used to identify the presence of an external power source (particularly one that is not subject to a fixed current limit like the USB V_{BUS} input). Typically, such a power supply would be a 5V wall adapter output or the low voltage output of a high voltage buck regulator (specifically, LT3480, LT3481 or LT3505). When the wall adapter output (or buck regulator output) is connected directly to the WALL pin, and the voltage exceeds the WALL pin threshold, the USB power path (from V_{BUS} to V_{OUT}) will be disconnected. Furthermore, the $\overline{ACPR}$ pin will be pulled low. In order for the presence of an external power supply to be acknowledged, both of the following conditions must be satisfied:

1. The WALL pin voltage must exceed approximately 4.3V.
2. The WALL pin voltage must exceed 75mV above the BAT pin voltage.

The input power path (between V_{BUS} and V_{OUT}) is re-enabled and the $\overline{ACPR}$ pin is pulled high when either of the following conditions is met:

1. The WALL pin voltage falls to within 25mV of the BAT pin voltage.
2. The WALL pin voltage falls below 3.2V.

Each of these thresholds is suitably filtered in time to prevent transient glitches on the WALL pin from falsely triggering an event.

See the Applications Information section for an explanation of high voltage buck regulator control using the V_C pin.

Suspend Mode

When ILIM0 is pulled low and ILIM1 is pulled high the LTC3557/LTC3557-1 enters Suspend mode to comply with the USB specification. In this mode, the power path between V_{BUS} and V_{OUT} is put in a high impedance state to reduce the V_{BUS} input current to 50µA. If no other power source is available to drive WALL and V_{OUT}, the system load connected to V_{OUT} is supplied through the ideal diodes connected to BAT. If an external power source drives WALL and V_{OUT} such that $V_{OUT} < V_{BUS}$, the Suspend mode V_{BUS} input current can be as high as 200µA.

3.3V Always-On Supply

The LTC3557/LTC3557-1 includes an ultralow quiescent current low dropout regulator that is always powered. This LDO can be used to provide power to a system pushbutton controller or standby microcontroller. Designed to deliver up to 25mA, the always-on LDO requires a 1µF MLCC bypass capacitor for compensation. The LDO is powered from V_{OUT}, and therefore will enter dropout at loads less than 25mA as V_{OUT} falls near 3.3V. If the LDO3V3 output is not used, it should be disabled by connecting it to V_{OUT}.

V_{BUS} Undervoltage Lockout (UVLO)

An internal undervoltage lockout circuit monitors V_{BUS} and keeps the input current limit circuitry off until V_{BUS} rises above the rising UVLO threshold (3.8V) and at least 50mV above V_{OUT}. Hysteresis on the UVLO turns off the input current limit if V_{BUS} drops below 3.7V or 50mV below V_{OUT}. When this happens, system power at V_{OUT} will be drawn from the battery via the ideal diode. To minimize the possibility of oscillation in and out of UVLO when using resistive input supplies, the input current limit is reduced when V_{BUS} falls to within a few hundred millivolts of the UVLO threshold. To ensure that full input current limit is available, apply at least 4.5V to V_{BUS}.

OPERATION

Battery Charger

The LTC3557/LTC3557-1 includes a constant current/constant voltage battery charger with automatic recharge, automatic termination by safety timer, low voltage trickle charging, bad cell detection and thermistor sensor input for out of temperature charge pausing.

When a battery charge cycle begins, the battery charger first determines if the battery is deeply discharged. If the battery voltage is below V_{TRKL}, typically 2.85V, an automatic trickle charge feature sets the battery charge current to 10% of the programmed value. If the low voltage persists for more than 1/2 hour, the battery charger automatically terminates and indicates via the $\overline{CHRG}$ pin that the battery was unresponsive.

Once the battery voltage is above 2.85V, the battery charger begins charging in full power constant current mode. The current delivered to the battery will try to reach 1000V/R_{PROG}. Depending on available input power and external load conditions, the battery charger may or may not be able to charge at the full programmed rate. The external load will always be prioritized over the battery charge current. The USB current limit programming will always be observed and only additional current will be available to charge the battery. When system loads are light, battery charge current will be maximized.

Charge Termination

The battery charger has a built-in safety timer. When the battery voltage approaches the float voltage (4.2V for LTC3557 or 4.1V for LTC3557-1), the charge current begins to decrease as the LTC3557/LTC3557-1 enters constant voltage mode. Once the battery charger detects that it has entered constant voltage mode, the four hour safety timer is started. After the safety timer expires, charging of the battery will terminate and no more current will be delivered.

Automatic Recharge

After the battery charger terminates, it will remain off drawing only microamperes of current from the battery. If the portable product remains in this state long enough, the battery will eventually self discharge. To ensure that the battery is always topped off, a charge cycle will automatically begin when the battery voltage falls below V_{RECHRG} (typically 4.1V for the LTC3557 or 4V for LTC3557-1). In the event that the safety timer is running when the battery voltage falls below V_{RECHRG}, the timer will reset back to zero. To prevent brief excursions below V_{RECHRG} from resetting the safety timer, the battery voltage must be below V_{RECHRG} for more than 1.3ms. The charge cycle and safety timer will also restart if the V_{BUS} UVLO cycles low and then high (e.g., V_{BUS}, is removed and then replaced).

Charge Current

The charge current is programmed using a single resistor from PROG to ground. 1/1000th of the battery charge current is delivered to PROG which will attempt to servo to 1.000V. Thus, the battery charge current will try to reach 1000 times the current in the PROG pin. The program resistor and the charge current are calculated using the following equations:

$$R_{PROG} = \frac{1000V}{I_{CHG}}, \quad I_{CHG} = \frac{1000V}{R_{PROG}}$$

In either the constant current or constant voltage charging modes, the PROG pin voltage will be proportional to the actual charge current delivered to the battery. Therefore, the actual charge current can be determined at any time by monitoring the PROG pin voltage and using the following equation:

$$I_{BAT} = \frac{V_{PROG}}{R_{PROG}} \bullet 1000$$

In many cases, the actual battery charge current, I_{BAT}, will be lower than I_{CHG} due to limited input current available and prioritization with the system load drawn from V_{OUT}.

Thermal Regulation

To prevent thermal damage to the IC or surrounding components, an internal thermal feedback loop will automatically decrease the programmed charge current if the die temperature rises to approximately 110°C. Thermal regulation protects the LTC3557/LTC3557-1 from excessive temperature due to high power operation

OPERATION

or high ambient thermal conditions and allows the user to push the limits of the power handling capability with a given circuit board design without risk of damaging the LTC3557/LTC3557-1 or external components. The benefit of the LTC3557/LTC3557-1 thermal regulation loop is that charge current can be set according to actual conditions rather than worst-case conditions with the assurance that the battery charger will automatically reduce the current in worst-case conditions.

Charge Status Indication

The $\overline{CHRG}$ pin indicates the status of the battery charger. Four possible states are represented by $\overline{CHRG}$ which include charging, not charging, unresponsive battery and battery temperature out of range.

The signal at the $\overline{CHRG}$ pin can be easily recognized as one of the above four states by either a human or a microprocessor. An open-drain output, the $\overline{CHRG}$ pin can drive an indicator LED through a current limiting resistor for human interfacing or simply a pull-up resistor for microprocessor interfacing.

To make the $\overline{CHRG}$ pin easily recognized by both humans and microprocessors, the pin is either a DC signal of ON for charging, OFF for not charging, or it is switched at high frequency (35kHz) to indicate the two possible faults, unresponsive battery, and battery temperature out of range.

When charging begins, $\overline{CHRG}$ is pulled low and remains low for the duration of a normal charge cycle. When charging is complete, i.e., the charger enters constant voltage mode and the charge current has dropped to one-tenth of the programmed value, the $\overline{CHRG}$ pin is released (high impedance). The $\overline{CHRG}$ pin does not respond to the C/10 threshold if the LTC3557/LTC3557-1 is in input current limit. This prevents false end of charge indications due to insufficient power available to the battery charger. If a fault occurs, the pin is switched at 35kHz. While switching, its duty cycle is modulated between a high and low value at a very low frequency. The low and high duty cycles are disparate enough to make an LED appear to be on or off thus giving the appearance of "blinking". Each of the two faults has its own unique "blink" rate for human recognition as well as two unique duty cycles for machine recognition.

Table 2: illustrates the four possible states of the $\overline{CHRG}$ pin when the battery charger is active.

Table 2: $\overline{CHRG}$ Output Pin

STATUS	FREQUENCY	MODULATION (BLINK) FREQUENCY	DUTY CYCLE
Charging	0Hz	0Hz (Lo-Z)	100%
I_{BAT} < C/10	0Hz	0Hz (Hi-Z)	0%
NTC Fault	35kHz	1.5Hz at 50%	6.25% or 93.75%
Bad Battery	35kHz	6.1Hz at 50%	12.5% or 87.5%

An NTC fault is represented by a 35kHz pulse train whose duty cycle toggles between 6.25% and 93.75% at a 1.5Hz rate. A human will easily recognize the 1.5Hz rate as a "slow" blinking which indicates the out-of-range battery temperature while a microprocessor will be able to decode either the 6.25% or 93.75% duty cycles as an NTC fault.

If a battery is found to be unresponsive to charging (i.e., its voltage remains below V_{TRKL}, typically 2.8V, for 1/2 hour), the $\overline{CHRG}$ pin gives the battery fault indication. For this fault, a human would easily recognize the frantic 6.1Hz "fast" blink of the LED while a microprocessor would be able to decode either the 12.5% or 87.5% duty cycles as a bad battery fault. Note that the LTC3557/LTC3557-1 is a 3-terminal PowerPath product where system load is always prioritized over battery charging. Due to excessive system load, there may not be sufficient power to charge the battery beyond the trickle charge threshold voltage within the bad battery timeout period. In this case, the battery charger will falsely indicate a bad battery. System software may then reduce the load and reset the battery charger to try again.

Although very improbable, it is possible that a duty cycle reading could be taken at the bright-dim transition (low duty cycle to high duty cycle). When this happens the duty cycle reading will be precisely 50%. If the duty cycle reading is 50%, system software should disqualify it and take a new duty cycle reading.

OPERATION

NTC Thermistor

The battery temperature is measured by placing a negative temperature coefficient (NTC) thermistor close to the battery pack. The NTC circuitry is shown in Figure 4. To use this feature connect the NTC thermistor, R_{NTC}, between the NTC pin and ground and a bias resistor, R_{NOM}, from V_{NTC} to NTC. R_{NOM} should be a 1% resistor with a value equal to the value of the chosen NTC thermistor at 25°C (R25). A 100k thermistor is recommended since thermistor current is not measured by the LTC3557/LTC3557-1 and will have to be considered for USB compliance.

The LTC3557/LTC3557-1 will pause charging when the resistance of the NTC thermistor drops to 0.54 times the value of R25 or approximately 54k (for a Vishay "Curve 1" thermistor, this corresponds to approximately 40°C). If the battery charger is in constant voltage (float) mode, the safety timer also pauses until the thermistor indicates a return to a valid temperature. As the temperature drops, the resistance of the NTC thermistor rises. The LTC3557/LTC3557-1 is also designed to pause charging when the value of the NTC thermistor increases to 3.25 times the value of R25. For a Vishay "Curve 1" thermistor this resistance, 325k, corresponds to approximately 0°C. The hot and cold comparators each have approximately 3°C of hysteresis to prevent oscillation about the trip point. Grounding the NTC pin disables all NTC functionality.

General Purpose Step-Down Switching Regulators

The LTC3557/LTC3557-1 includes three 2.25MHz constant frequency current mode step-down switching regulators providing 400mA, 400mA and 600mA each. All step-down switching regulators can be programmed for a minimum output voltage of 0.8V and can be used to power a microcontroller core, microcontroller I/O, memory or other logic circuitry. All step-down switching regulators support 100% duty cycle operation (low dropout mode) when the input voltage drops very close to the output voltage and are also capable of Burst Mode operation for highest efficiencies at light loads (Burst Mode operation is pin selectable). The step-down switching regulators also include soft-start to limit inrush current when powering on, short-circuit current protection, and switch node slew limiting circuitry to reduce EMI radiation. No external compensation components are required for the switching regulators.

A single MODE pin sets all step-down switching regulators in Burst Mode or pulse-skip mode operation, while each regulator is enabled individually through their respective enable pins (EN1, EN2 and EN3). It is recommended that the step-down switching regulator input supplies (V_{IN1} and V_{IN2}) be connected to the system supply pin (V_{OUT}). This allows the undervoltage lock out circuit on the V_{OUT} pin (V_{OUT} UVLO)to disable the step-down switching regulators when the V_{OUT} voltage drops below V_{OUT} UVLO threshold. If driving the step-down switching regulator input supplies from a voltage other than V_{OUT} the regulators should not be operated outside the specified operating range as operation is not guaranteed beyond this range.

Step-Down Switching Regulator Output Voltage Programming

Figure 2 shows the step-down switching regulator application circuit. The full-scale output voltage for each step-down switching regulator is programmed using a resistor divider from the step-down switching regulator output connected to the feedback pins (FB1, FB2 and FB3) such that:

$$V_{OUTx} = 0.8V \bullet \left(\frac{R1}{R2} + 1\right)$$

Typical values for R1 are in the range of 40k to 1M. The capacitor C_{FB} cancels the pole created by feedback resistors and the input capacitance of the FB pin and also helps to improve transient response for output voltages much greater than 0.8V. A variety of capacitor sizes can be used for C_{FB} but a value of 10pF is recommended for most applications. Experimentation with capacitor sizes between 2pF and 22pF may yield improved transient response.

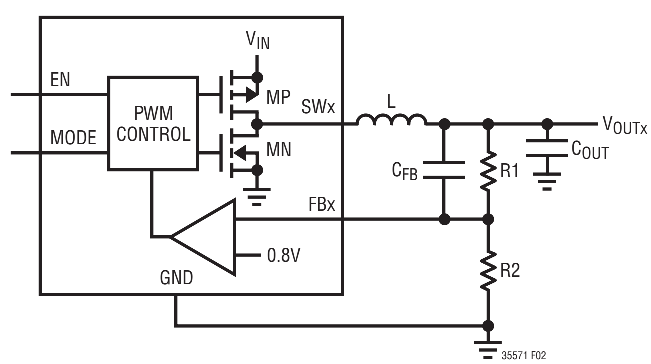


Figure 2. Buck Converter Application Circuit

OPERATION

Step-Down Switching Regulator $\overline{RST2}$ Operation

The $\overline{RST2}$ pin is an open-drain output used to indicate that step-down switching regulator 2 has been enabled and has reached its final voltage. A 230ms delay is included from the time switching regulator 2 reaches 92% of its regulation value to allow a system controller ample time to reset itself. $\overline{RST2}$ may be used as a power-on reset to the microprocessor powered by regulator 2 or may be used to enable regulators 1 and/or 3 for supply sequencing. $\overline{RST2}$ is an open-drain output and requires a pull-up resistor to the output voltage of regulator 2 or another appropriate power source.

Step-Down Switching Regulator Operating Modes

The step-down switching regulators include two possible operating modes to meet the noise/power needs of a variety of applications.

In pulse-skip mode, an internal latch is set at the start of every cycle, which turns on the main P-channel MOSFET switch. During each cycle, a current comparator compares the peak inductor current to the output of an error amplifier. The output of the current comparator resets the internal latch, which causes the main P-channel MOSFET switch to turn off and the N-channel MOSFET synchronous rectifier to turn on. The N-channel MOSFET synchronous rectifier turns off at the end of the 2.25MHz cycle or if the current through the N-channel MOSFET synchronous rectifier drops to zero. Using this method of operation, the error amplifier adjusts the peak inductor current to deliver the required output power. All necessary compensation is internal to the step-down switching regulator requiring only a single ceramic output capacitor for stability. At light loads in pulse-skip mode, the inductor current may reach zero on each pulse which will turn off the N-channel MOSFET synchronous rectifier. In this case, the switch node (SW1, SW2 or SW3) goes high impedance and the switch node voltage will "ring". This is discontinuous operation, and is normal behavior for a switching regulator. At very light loads in pulse-skip mode, the step-down switching regulators will automatically skip pulses as needed to maintain output regulation. At high duty cycle ($V_{OUTX} > V_{INX}/2$) it is possible for the inductor current to reverse at light loads causing the stepped down switching regulator to operate continuously. When operating continuously, regulation and low noise output voltage are maintained, but input operating current will increase to a few milliamps.

In Burst Mode operation, the step-down switching regulators automatically switch between fixed frequency PWM operation and hysteretic control as a function of the load current. At light loads the step-down switching regulators control the inductor current directly and use a hysteretic control loop to minimize both noise and switching losses. While operating in Burst Mode operation, the output capacitor is charged to a voltage slightly higher than the regulation point. The step-down switching regulator then goes into sleep mode, during which the output capacitor provides the load current. In sleep mode, most of the switching regulator's circuitry is powered down, helping conserve battery power. When the output voltage drops below a pre-determined value, the step-down switching regulator circuitry is powered on and another burst cycle begins. The sleep time decreases as the load current increases. Beyond a certain load current point (about 1/4 rated output load current) the step-down switching regulators will switch to a low noise constant frequency PWM mode of operation, much the same as pulse-skip operation at high loads. For applications that can tolerate some output ripple at low output currents, Burst Mode operation provides better efficiency than pulse-skip at light loads.

The step-down switching regulators allow mode transition on-the-fly, providing seamless transition between modes even under load. This allows the user to switch back and forth between modes to reduce output ripple or increase low current efficiency as needed. Burst Mode operation is set by driving the MODE pin high, while pulse-skip mode is achieved by driving the MODE pin low.

Step-Down Switching Regulator in Shutdown

The step-down switching regulators are in shutdown when not enabled for operation. In shutdown all circuitry in the step-down switching regulator is disconnected from the switching regulator input supply leaving only a few nanoamps of leakage current. The step-down switching regulator outputs are individually pulled to ground through a 10k resistor on the switch pin (SW1, SW2 or SW3) when in shutdown.

OPERATION

Step-down Switching Regulator Dropout Operation

It is possible for a step-down switching regulator's input voltage to approach its programmed output voltage (e.g., a battery voltage of 3.4V with a programmed output voltage of 3.3V). When this happens, the PMOS switch duty cycle increases until it is turned on continuously at 100%. In this dropout condition, the respective output voltage equals the regulator's input voltage minus the voltage drops across the internal P-channel MOSFET and the inductor.

Step-Down Switching Regulator Soft-Start Operation

Soft-start is accomplished by gradually increasing the peak inductor current for each step-down switching regulator over a 500µs period. This allows each output to rise slowly, helping minimize inrush current required to charge up the switching regulator output capacitor. A soft-start cycle occurs whenever a given switching regulator is enabled, or after a fault condition has occurred (thermal shutdown or UVLO). A soft-start cycle is not triggered by changing operating modes. This allows seamless output transition when actively changing between operating modes.

Step-Down Switching Regulator Switching Slew Rate Control

The step-down switching regulators contain new patent-pending circuitry to limit the slew rate of the switch node (SW1, SW2 and SW3). This new circuitry is designed to transition the switch node over a period of a couple nano-seconds, significantly reducing radiated EMI and conducted supply noise while maintaining high efficiency.

Step-Down Switching Regulator Low Supply Operation

An undervoltage lockout (UVLO) circuit on V_{OUT} shuts down the step-down switching regulators when V_{OUT} drops below about 2.6V. It is recommended that the step-down switching regulators input supplies be connected to the power path output (V_{OUT}). This UVLO prevents the step-down switching regulators' from operating at low supply voltages where loss of regulation or other undesirable operation may occur. If driving the step-down switching regulator input supplies from a voltage other than the V_{OUT} pin, the regulators should not be operate outside the specified operating range as operation is not guaranteed beyond this range.

Step-Down Switching Regulator Inductor Selection

Many different sizes and shapes of inductors are available from numerous manufacturers. Choosing the right inductor from such a large selection of devices can be overwhelming, but following a few basic guidelines will make the selection process much simpler.

The step-down converters are designed to work with inductors in the range of 2.2µH to 10µH. For most applications a 4.7µH inductor is suggested for step-down switching regulators providing up to 400mA of output current while a 3.3µH inductor is suggested for step-down switching regulators providing up to 600mA. Larger value inductors reduce ripple current, which improves output ripple voltage. Lower value inductors result in higher ripple current and improved transient response time, but will reduce the available output current. To maximize efficiency, choose an inductor with a low DC resistance. For a 1.2V output, efficiency is reduced about 2% for 100mΩ series resistance at 400mA load current, and about 2% for 300mΩ series resistance at 100mA load current. Choose an inductor with a DC current rating at least 1.5 times larger than the maximum load current to ensure that the inductor does not saturate during normal operation. If output short circuit is a possible condition, the inductor should be rated to handle the maximum peak current specified for the step-down converters.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or Permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. Inductors that are very thin or have a very small volume typically have much higher core and DCR losses, and will not give the best efficiency. The choice of which style inductor to use often depends more on the price vs size, performance, and any radiated EMI requirements than on what the step-down switching regulators requires to operate.

OPERATION

The inductor value also has an effect on Burst Mode operation. Lower inductor values will cause Burst Mode switching frequency to increase.

Table 3 shows several inductors that work well with the step-down switching regulators. These inductors offer a good compromise in current rating, DCR and physical size. Consult each manufacturer for detailed information on their entire selection of inductors.

Step-Down Switching Regulator Input/Output Capacitor Selection

Low ESR (equivalent series resistance) ceramic capacitors should be used at both step-down switching regulator outputs as well as at each step-down switching regulator input supply. Only X5R or X7R ceramic capacitors should be used because they retain their capacitance over wider voltage and temperature ranges than other ceramic types. A 10μF output capacitor is sufficient for the step-down switching regulator outputs. For good transient response and stability the output capacitor for step-down switching regulators should retain at least 4μF of capacitance over operating temperature and bias voltage. Each switching regulator input supply should be bypassed with a 2.2μF capacitor. Consult with capacitor manufacturers for detailed information on their selection and specifications of ceramic capacitors. Many manufacturers now offer very thin (<1mm tall) ceramic capacitors ideal for use in height-restricted designs. Table 4 shows a list of several ceramic capacitor manufacturers.

Table 4. Ceramic Capacitor Manufacturers

AVX	www.avxcorp.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
Vishay Siliconix	www.vishay.com
TDK	www.tdk.com

Table 3. Recommended Inductors for Step-Down Switching Regulators

INDUCTOR TYPE	L (μH)	MAX I_{DC} (A)	MAX DCR (Ω)	SIZE in mm (L × W × H)	MANUFACTURER
DE2818C	4.7 3.3	1.25 1.45	0.072 0.053	3.0 × 2.8 × 1.8 3.0 × 2.8 × 1.8	Toko www.toko.com
D312C	4.7 3.3	0.79 0.90	0.24 0.20	3.6 × 3.6 × 1.2 3.6 × 3.6 × 1.2	
DE2812C	4.7 3.3	1.2 1.4	0.13* 0.105*	3.0 × 2.8 × 1.2 3.0 × 2.8 × 1.2	
CDRH3D16	4.7 3.3	0.9 1.1	0.11 0.085	4.0 × 4.0 × 1.8 4.0 × 4.0 × 1.8	Sumida www.sumida.com
CDRH2D11	4.7 3.3	0.5 0.6	0.17 0.123	3.2 × 3.2 × 1.2 3.2 × 3.2 × 1.2	
CLS4D09	4.7	0.75	0.19	4.9 × 4.9 × 1	
SD3118	4.7 3.3	1.3 1.59	0.162 0.113	3.1 × 3.1 × 1.8 3.1 × 3.1 × 1.8	Cooper www.cooperet.com
SD3112	4.7 3.3	0.8 0.97	0.246 0.165	3.1 × 3.1 × 1.2 3.1 × 3.1 × 1.2	
SD12	4.7 3.3	1.29 1.42	0.117* 0.104*	5.2 × 5.2 × 1.2 5.2 × 5.2 × 1.2	
SD10	4.7 3.3	1.08 1.31	0.153* 0.108*	5.2 × 5.2 × 1.0 5.2 × 5.2 × 1.0	
LPS3015	4.7 3.3	1.1 1.3	0.2 0.13	3.0 × 3.0 × 1.5 3.0 × 3.0 × 1.5	Coil Craft www.coilcraft.com

*Typical DCR

APPLICATIONS INFORMATION

External HV Buck Control Through the V_C Pin

The WALL, $\overline{ACPR}$ and V_C pins can be used in conjunction with an external high voltage buck regulator such as the LT®3480, LT3481 or LT3505 to provide power directly to the V_{OUT} pin through a power P-channel MOSFET as shown in Figures 3-5 (consult the factory for a complete list of approved high voltage buck regulators). When the WALL pin voltage exceeds 4.3V, V_C pin control circuitry is enabled and drives the V_C pin of the LT3480, LT3481 or LT3505. The V_C pin control circuitry is designed so that no compensation components are required on the V_C node. The voltage at the V_{OUT} pin is regulated to the larger of (BAT + 300mV) or 3.6V as shown in Figures 6 and 7. The feedback network of the high voltage regulator should be set to generate an output voltage higher than 4.4V (be sure to include the output voltage tolerance of the buck regulator). The V_C control of the LTC3557 overdrives the local V_C control of the external high voltage buck. Therefore, once the V_C control is enabled, the output voltage is set independent of the buck regulator feedback network.

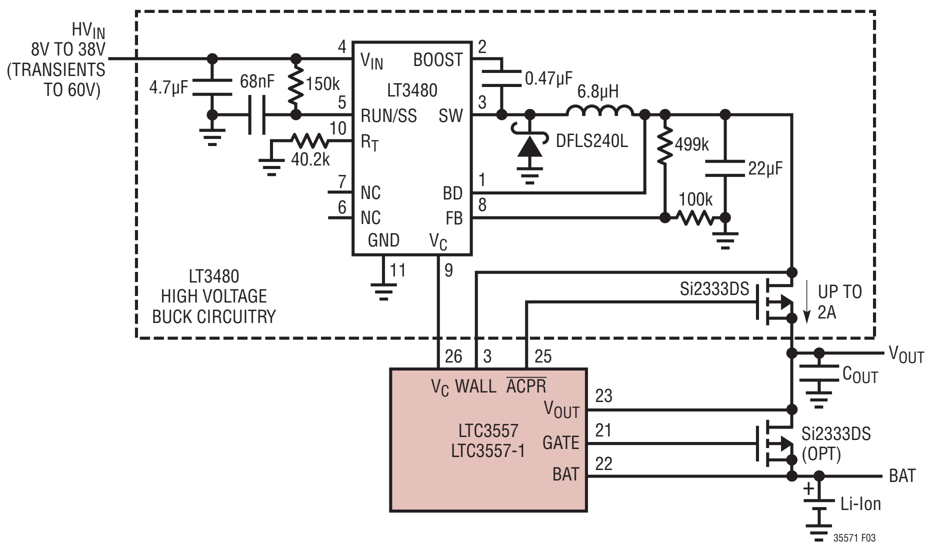


Figure 3. LT3480 Buck Control Using V_C (800kHz Switching)

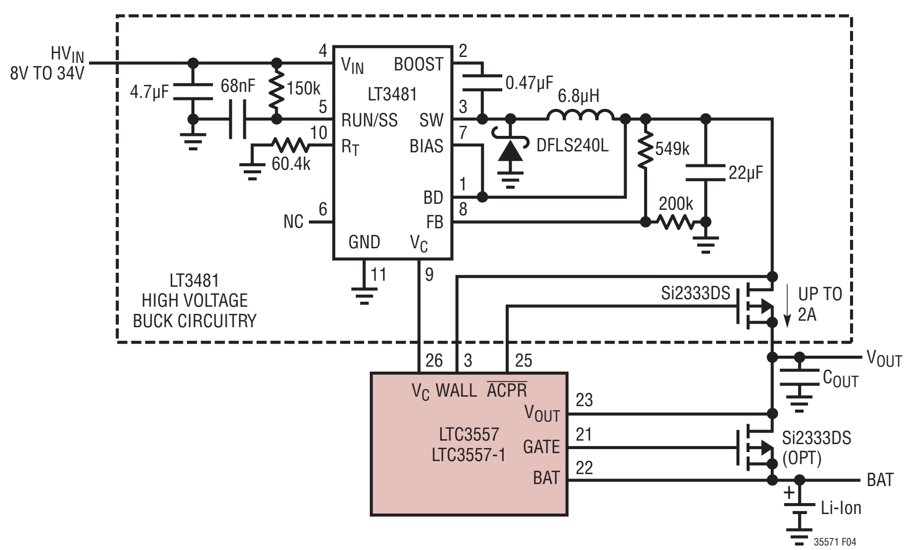


Figure 4. LT3481 Buck Control Using V_C (800kHz Switching)

APPLICATIONS INFORMATION

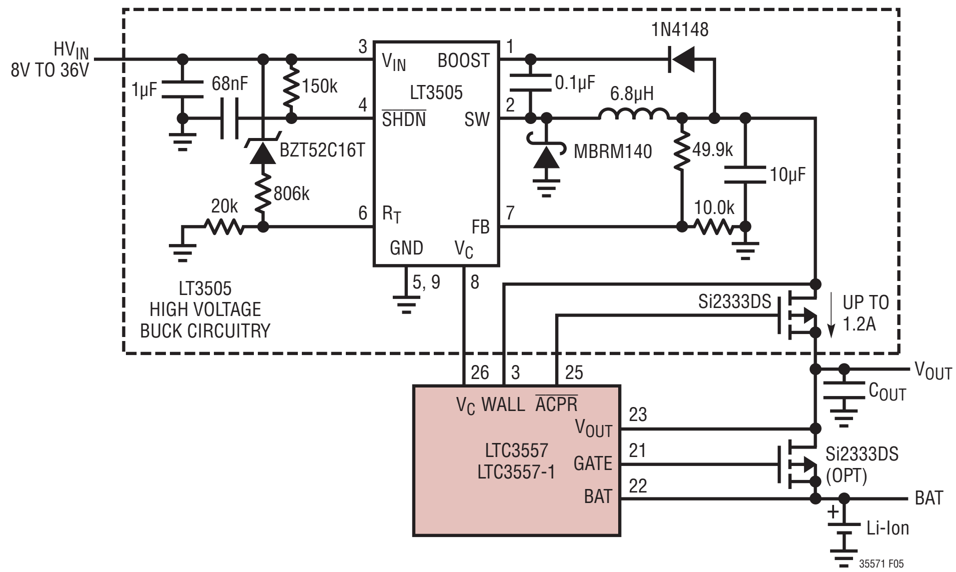


Figure 5. LT3505 Buck Control Using V_C (2.2MHz Switching with Frequency Foldback)

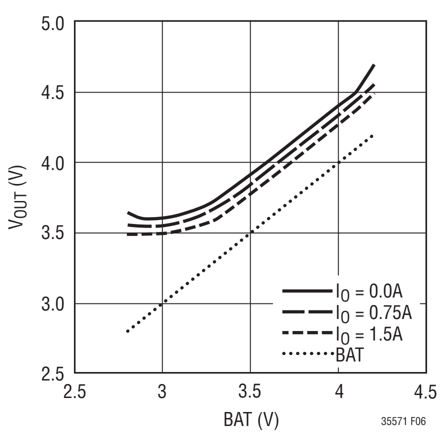


Figure 6. LTC3557 V_{OUT} Voltage vs Battery Voltage with the LT3480

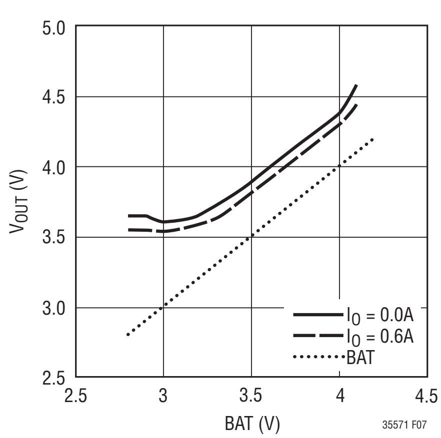


Figure 7. LTC3557-1V_{OUT} Voltage vs Battery Voltage with the LT3505

This technique provides a significant efficiency advantage over the use of a 5V buck to drive the battery charger. With a simple 5V buck output driving V_{OUT}, battery charger efficiency is approximately:

$$\eta_{CHARGER} = \eta_{BUCK} \bullet \frac{V_{BAT}}{5V}$$

where η_{BUCK} is the efficiency of the high voltage buck regulator and 5V is the output voltage of the buck regulator. With a typical buck efficiency of 87% and a typical battery voltage of 3.8V, the total battery charger efficiency is approximately 66%. Assuming a 1A charge current, this works out to nearly 2W of power dissipation just to charge the battery!

With the V_C control technique, battery charger efficiency is approximately:

$$\eta_{CHARGER} = \eta_{BUCK} \bullet \frac{V_{BAT}}{0.3V + V_{BAT}}$$

With the same assumptions as above, the total battery charger efficiency is approximately 81%. This example works out to just 900mW of power dissipation. For applications, component selection and board layout information beyond those listed here please refer to the respective LT3480, LT3481 or LT3505 data sheet.

APPLICATIONS INFORMATION

Alternate NTC Thermistors and Biasing

The LTC3557/LTC3557-1 provides temperature qualified charging if a grounded thermistor and a bias resistor are connected to NTC. By using a bias resistor whose value is equal to the room temperature resistance of the thermistor (R25) the upper and lower temperatures are pre-programmed to approximately 40°C and 0°C, respectively (assuming a Vishay "Curve 1" thermistor).

The upper and lower temperature thresholds can be adjusted by either a modification of the bias resistor value or by adding a second adjustment resistor to the circuit. If only the bias resistor is adjusted, then either the upper or the lower threshold can be modified but not both. The other trip point will be determined by the characteristics of the thermistor. Using the bias resistor in addition to an adjustment resistor, both the upper and the lower temperature trip points can be independently programmed with the constraint that the difference between the upper and lower temperature thresholds cannot decrease. Examples of each technique are given below.

NTC thermistors have temperature characteristics which are indicated on resistance-temperature conversion tables. The Vishay-Dale thermistor NTHS0603N011-N1003F, used in the following examples, has a nominal value of 100k and follows the Vishay "Curve 1" resistance-temperature characteristic.

In the explanation below, the following notation is used.

R25 = Value of the Thermistor at 25°C

$R_{NTC|COLD}$ = Value of thermistor at the cold trip point

$R_{NTC|HOT}$ = Value of the thermistor at the hot trip point

r_{COLD} = Ratio of $R_{NTC|COLD}$ to R25

r_{HOT}= Ratio of $R_{NTC|HOT}$ to R25

R_{NOM} = Primary thermistor bias resistor (see Figure 8)

R1 = Optional temperature range adjustment resistor (see Figure 9)

The trip points for the LTC3557/LTC3557-1's temperature qualification are internally programmed at 0.349 • V_{VNTC} for the hot threshold and 0.765 • V_{VNTC} for the cold threshold.

Therefore, the hot trip point is set when:

$$\frac{R_{NTC|HOT}}{R_{NOM} + R_{NTC|HOT}} \bullet V_{VNTC} = 0.349 \bullet V_{VNTC}$$

and the cold trip point is set when:

$$\frac{R_{NTC|COLD}}{R_{NOM} + R_{NTC|COLD}} \bullet V_{VNTC} = 0.765 \bullet V_{VNTC}$$

Solving these equations for $R_{NTC|COLD}$ and $R_{NTC|HOT}$ results in the following:

$$R_{NTC|HOT} = 0.536 \bullet R_{NOM}$$

and

$$R_{NTC|COLD} = 3.25 \bullet R_{NOM}$$

By setting R_{NOM} equal to R25, the above equations result in r_{HOT} = 0.536 and r_{COLD} = 3.25. Referencing these ratios to the Vishay Resistance-Temperature Curve 1 chart gives a hot trip point of about 40°C and a cold trip point of about 0°C. The difference between the hot and cold trip points is approximately 40°C.

By using a bias resistor, R_{NOM}, different in value from R25, the hot and cold trip points can be moved in either direction. The temperature span will change somewhat due to the non-linear behavior of the thermistor. The following equations can be used to easily calculate a new value for the bias resistor:

$$R_{NOM} = \frac{r_{HOT}}{0.536} \bullet R25$$

$$R_{NOM} = \frac{r_{COLD}}{3.25} \bullet R25$$

where r_{HOT} and r_{COLD} are the resistance ratios at the *desired* hot and cold trip points. Note that these equations are linked. Therefore, only one of the two trip points can be chosen, the other is determined by the default ratios designed in the IC. Consider an example where a 60°C hot trip point is desired.

APPLICATIONS INFORMATION

From the Vishay Curve 1 R-T characteristics, r_{HOT} is 0.2488 at 60°C. Using the above equation, R_{NOM} should be set to 46.4k. With this value of R_{NOM}, the cold trip point is about 16°C. Notice that the span is now 44°C rather than the previous 40°C. This is due to the decrease in "temperature gain" of the thermistor as absolute temperature increases.

The upper and lower temperature trip points can be independently programmed by using an additional bias resistor as shown in Figure 9. The following formulas can be used to compute the values of R_{NOM} and R1:

$$R_{NOM} = \frac{r_{COLD} - r_{HOT}}{2.714} \bullet R25$$

$$R1 = 0.536 \bullet R_{NOM} - r_{HOT} \bullet R25$$

For example, to set the trip points to 0°C and 45°C with a Vishay Curve 1 thermistor choose

$$R_{NOM} = \frac{3.266 - 0.4368}{2.714} \bullet 100k = 104.2k$$

the nearest 1% value is 105k.

$$R1 = 0.536 \bullet 105k - 0.4368 \bullet 100k = 12.6k$$

the nearest 1% value is 12.7k. The final solution is shown in Figure 9 and results in an upper trip point of 45°C and a lower trip point of 0°C.

Battery Charger Stability Considerations

The LTC3557/LTC3557-1's battery charger contains both a constant voltage and a constant current control loop. The constant voltage loop is stable without any compensation when a battery is connected with low impedance leads. Excessive lead length, however, may add enough series inductance to require a bypass capacitor of at least 1µF from BAT to GND. Furthermore, a 4.7µF capacitor in series with a 0.2Ω to 1Ω resistor from BAT to GND is required to keep ripple voltage low when the battery is disconnected.

High value, low ESR multilayer ceramic chip capacitors reduce the constant voltage loop phase margin, possibly resulting in instability. Ceramic capacitors up to 22µF may be used in parallel with a battery, but larger ceramics should be decoupled with 0.2Ω to 1Ω of series resistance.

In constant current mode, the PROG pin is in the feedback loop rather than the battery voltage. Because of the additional pole created by any PROG pin capacitance, capacitance on this pin must be kept to a minimum. With

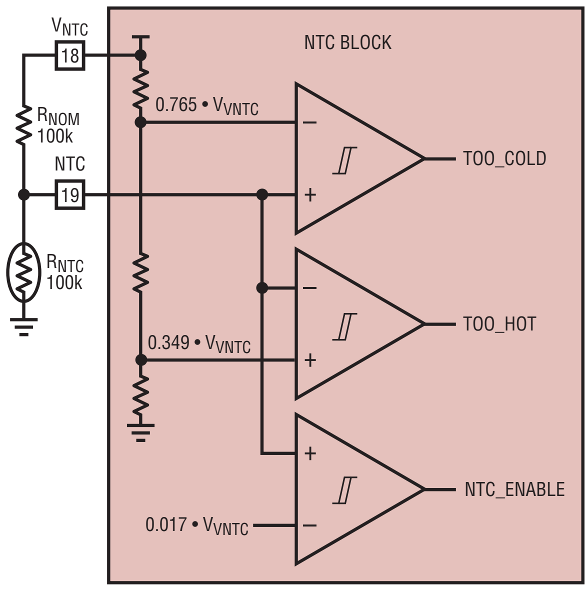


Figure 8. Typical NTC Thermistor Circuit

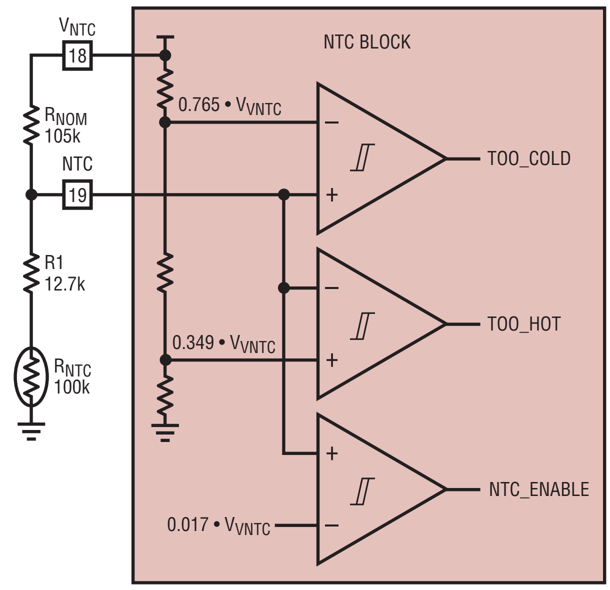


Figure 9. NTC Thermistor Circuit with Additional Bias Resistor

APPLICATIONS INFORMATION

no additional capacitance on the PROG pin, the battery charger is stable with program resistor values as high as 25k. However, additional capacitance on this node reduces the maximum allowed program resistor. The pole frequency at the PROG pin should be kept above 100kHz. Therefore, if the PROG pin has a parasitic capacitance, C_{PROG}, the following equation should be used to calculate the maximum resistance value for R_{PROG}:

$$R_{PROG} \le \frac{1}{2\pi \bullet 100kHz \bullet C_{PROG}}$$

Printed Circuit Board Power Dissipation Considerations

In order to be able to deliver maximum charge current under all conditions, it is critical that the Exposed Pad on the backside of the LTC3557/LTC3557-1 package is soldered to a ground plane on the board. Correctly soldered to a $2500mm^2$ ground plane on a double-sided 1oz copper board, the LTC3557/LTC3557-1 has a thermal resistance (θ_{JA}) of approximately 37°C/W. Failure to make good thermal contact between the Exposed Pad on the backside of the package and an adequately sized ground plane will result in thermal resistances far greater than 37°C/W.

The conditions that cause the LTC3557/LTC3557-1 to reduce charge current due to the thermal protection feedback can be approximated by considering the power dissipated in the part. For high charge currents and a wall adapter applied to V_{OUT}, the LTC3557/LTC3557-1 power dissipation is approximately:

$$P_D = (V_{OUT} - BAT) \bullet I_{BAT} + P_{D(SW1)} + P_{D(SW2)} + P_{D(SW3)}$$

where, P_D is the total power dissipated, V_{OUT} is the supply voltage, BAT is the battery voltage and I_{BAT} is the battery charge current. $P_{D(SWx)}$ is the power loss by the step-down switching regulators. The power loss for a step-down switching regulator can be calculated as follows:

$$P_{D(SWx)} = (OUTx \bullet I_{OUT}) \bullet (100 - Eff)/100$$

where OUTx is the programmed output voltage, I_{OUT} is the load current and Eff is the % efficiency which can be measured or looked up on an efficiency graph for the programmed output voltage.

It is not necessary to perform any worst-case power dissipation scenarios because the LTC3557/LTC3557-1 will automatically reduce the charge current to maintain the die temperature at approximately 110°C. However, the approximate ambient temperature at which the thermal feedback begins to protect the IC is:

$$T_A = 110°C - P_D \bullet \theta_{JA}$$

Example: Consider the LTC3557/LTC3557-1 operating from a wall adapter with 5V (V_{OUT}) providing 1A (I_{BAT}) to charge a Li-Ion battery at 3.3V (BAT). Also assume $P_{D(SW1)} = P_{D(SW2)} = P_{D(SW3)} = 0.05W$, so the total power dissipation is:

$$P_D = (5V - 3.3V) \bullet 1A + 0.15W = 1.85W$$

The ambient temperature above which the LTC3557/LTC3557-1 will begin to reduce the 1A charge current, is approximately:

$$T_A = 110°C - 1.85W \bullet 37°C/W = 42°C$$

The LTC3557/LTC3557-1 can be used above 42°C, but the charge current will be reduced below 1A. The charge current at a given ambient temperature can be approximated by:

$$P_D = \frac{110°C - T_A}{\theta_{JA}}$$

$$= \left(V_{OUT} - BAT\right) \bullet I_{BAT} + P_{D(SW1)} + P_{D(SW2)} + P_{D(SW3)}$$

thus:

$$I_{BAT} = \frac{\dfrac{110°C - T_A}{\theta_{JA}} - P_{D(SW1)} - P_{D(SW2)} - P_{D(SW3)}}{V_{OUT} - BAT}$$

Consider the above example with an ambient temperature of 55°C. The charge current will be reduced to approximately:

$$I_{BAT} = \frac{\dfrac{110°C - 55°C}{37°C/W} - 0.15W}{5V - 3.3V}$$

$$= \frac{1.49W - 0.15W}{1.7V} = 786mA$$

APPLICATIONS INFORMATION

If an external buck switching regulator controlled by the LTC3557/LTC3557-1 V_C pin is used instead of a 5V wall adapter we see a significant reduction in power dissipated by the LTC3557/LTC3557-1. This is because the external buck switching regulator will drive the PowerPath output (V_{OUT}) to about 3.6V with the battery at 3.3V. If you go through the example above and substitute 3.6V for V_{OUT} we see that thermal regulation does not kick in until about 93°C. Thus, the external regulator not only allows higher charging currents, but lower power dissipation means a cooler running application.

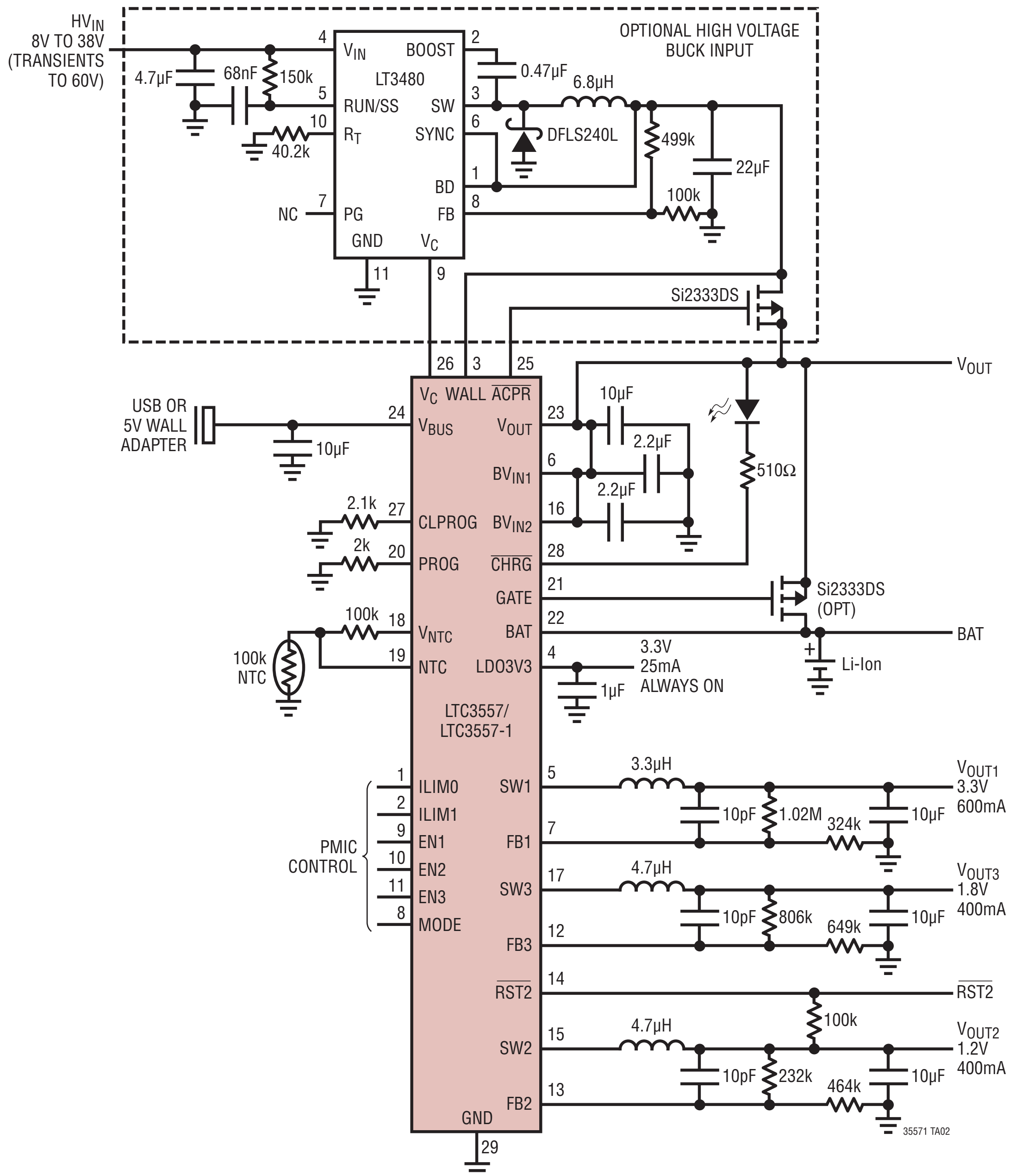
Printed Circuit Board Layout Considerations

When laying out the printed circuit board, the following list should be followed to ensure proper operation of the LTC3557/LTC3557-1:

1. The Exposed Pad of the package (Pin 29) should connect directly to a large ground plane to minimize thermal and electrical impedance.
2. The trace connecting the step-down switching regulator input supply pins (V_{IN1} and V_{IN2}) and their respective decoupling capacitors should be kept as short as possible. The GND side of these capacitors should connect directly to the ground plane of the part. These capacitors provide the AC current to the internal power MOSFETs and their drivers. It's important to minimize inductance from these capacitors to the pins of the LTC3557/LTC3557-1. Connect V_{IN1} and V_{IN2} to V_{OUT} through a short low impedance trace.
3. The switching power traces connecting SW1, SW2 and SW3 to their respective inductors should be minimized to reduce radiated EMI and parasitic coupling. Due to the large voltage swing of the switching nodes, sensitive nodes such as the feedback nodes (FB1, FB2 and FB3) should be kept far away or shielded from the switching nodes or poor performance could result.
4. Connections between the step-down switching regulator inductors and their respective output capacitors should be kept as short as possible. The GND side of the output capacitors should connect directly to the thermal ground plane of the part.
5. Keep the feedback pin traces (FB1, FB2 and FB3) as short as possible. Minimize any parasitic capacitance between the feedback traces and any switching node (i.e., SW1, SW2, SW3 and logic signals). If necessary shield the feedback nodes with a GND trace

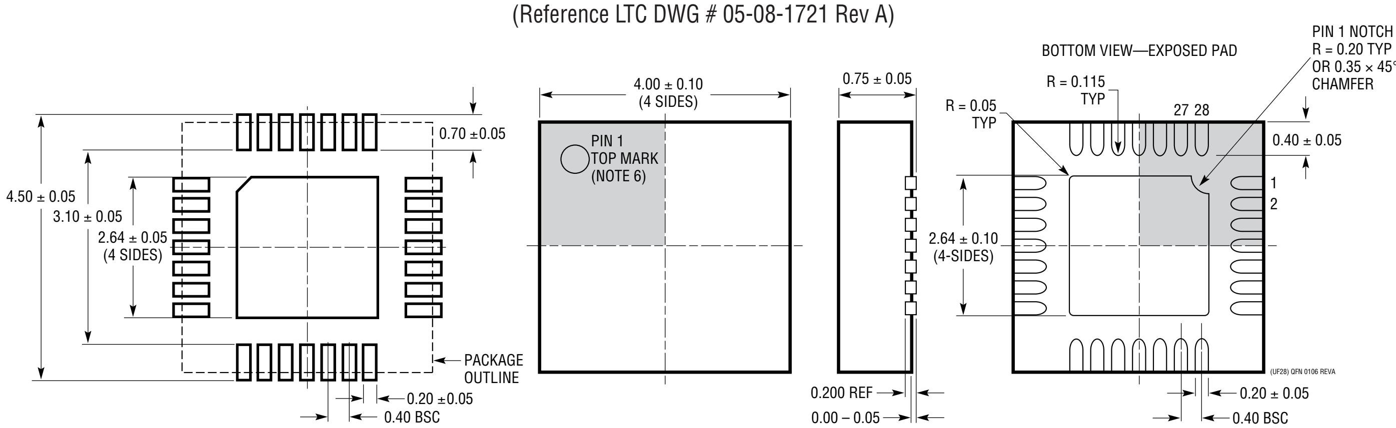
6) Connections between the LTC3557/LTC3557-1 power path pins (V_{BUS} and V_{OUT}) and their respective decoupling capacitors should be kept as short as possible. The GND side of these capacitors should connect directly to the ground plane of the part. V_{OUT} should be decoupled with a 10µF or greater ceramic capacitor as close as possible to the LTC3557/LTC3557-1.

TYPICAL APPLICATION



PACKAGE DESCRIPTION

UF Package
28-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1721 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Power Management		
LTC3455	Dual DC/DC Converter with USB Power Management and Li-Ion Battery Charger	Efficiency >96%, Accurate USB Current Limiting (500mA/100mA), 4mm × 4mm 24-Pin QFN Package
LTC3456	2-Cell Multi-Output DC/DC Converter with USB Power Manager	Seamless Transition Between 2-Cell Battery, USB and AC Wall Adapter Input Power Sources, QFN Package
LTC3555	Switching USB Power Manager with Li-Ion/Polymer Charger, Triple Synchronous Buck Converter + LDO	Complete Multifunction PMIC: Switch Mode Power Manager and Three Buck Regulators + LDO, Charge Current Programmable up to 1.5A from Wall Adapter Input, Thermal Regulation Synchronous Buck Converters Efficiency: >95%, ADJ Outputs: 0.8V to 3.6V at 400mA/400mA/1A Bat-Track Adaptive Output Control, 200mΩ Ideal Diode, 4mm × 5mm 28-Pin QFN Package
LTC3559	Linear USB Li-Ion/Polymer Battery Charger with Dual Synchronous Buck Converter	Adjustable Synchronous Buck Converters, Efficiency: >90%, Outputs: Down to 0.8V at 400mA for each, Charge Current Programmable up to 950mA, USB Compatible, 3mm × 3mm 16-Pin QFN Package
Battery Chargers		
LTC4055	USB Power Controller and Battery Charger	Charges Single Cell Li-Ion Batteries Directly from a USB Port, Thermal Regulation, 200mΩ Ideal Diode, 4mm × 4mm 16-Pin QFN Package
LTC4066	USB Power Controller and Li-Ion Battery Charger with Low Loss Ideal Diode	Charges Single Cell Li-Ion Batteries Directly from a USB Port, Thermal Regulation, 50mΩ Ideal Diode, 4mm × 4mm 24-Pin QFN Package
LTC4085	USB Power Manager with Ideal Diode Controller and Li-Ion Charger	Charges Single Cell Li-Ion Batteries Directly from a USB Port, Thermal Regulation, 200mΩ Ideal Diode with <50mΩ Option, 4mm × 3mm 14-Pin DFN Package
LTC4088	High Efficiency USB Power Manager and Battery Charger	Maximizes Available Power from USB Port, Bat-Track, "Instant On" Operation, 1.5A Max Charge Current, 180mΩ Ideal Diode with <50mΩ Option, 3.3V/25mA Always On LDO, 4mm × 3mm 14-Pin DFN Package
LTC4089/LTC4089-5	USB Power Manager with Ideal Diode Controller and High Efficiency Li-Ion Battery Charger	1.2A Charger, 6V to 36V (40V_{MAX}), 200mΩ Ideal Diode with 50mΩ Option, 6mm × 3mm 22-Pin DFN Package

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