Triple Output Synchronous 3-Phase DC/DC Controller with Up/Down Tracking

FEATURES

- **Current Mode Controller with Onboard MOSFET Drivers**
- **Programmable Power Up/Down Tracking**
- **Wide V_{IN} Range: 3.3V to 36V (V_{CC} = 5V)**
- ±1% 0.6V V_{FB} Accuracy Over Temperature
- Power Good Output Voltage Monitor
- Phase-Lockable or Adjustable Frequency: 160kHz to 700kHz
- OPTI-LOOP® Compensation Minimizes C_{OUT}
- Current Foldback and Overvoltage Protection
- Selectable Continuous, Discontinuous or Burst Mode® Operation at Light Load
- Programmable Phase Operation
- Available in 5mm x 7mm QFN and 36-Lead SSOP Packages

APPLICATIONS

- Servers, Telecom, Industrial Power Supplies
- General Purpose Multiple Rail DC/DC
- FPGA and DSP Requirements

DESCRIPTION

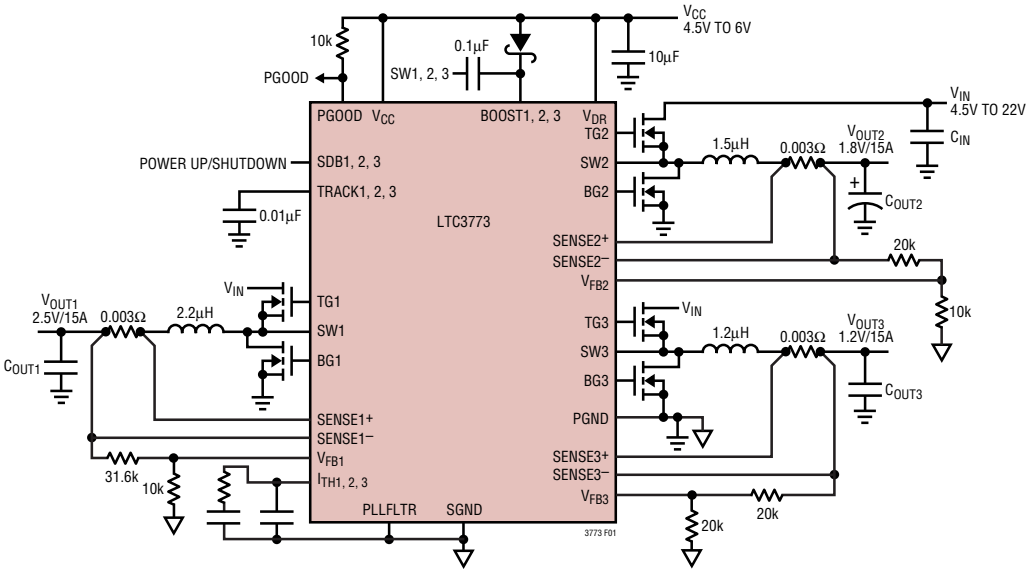
The LTC®3773 is a high performance, 3-phase, triple output synchronous step-down switching regulator controller with output voltage power up/down tracking capability. The controller allows for sequential, coincident or ratiometric tracking.

This 3-phase controller drives its output stages with 120° phase separation at frequencies of up to 700kHz per phase minimizing the RMS input current. Light load efficiency can be maximized by using selectable Burst Mode operation. The 0.6V precision reference supports output voltages from 0.6V to 5V.

Fault protection features include output overvoltage, input undervoltage lockout plus current foldback under short-circuit or overload conditions.

TYPICAL APPLICATION

High Efficiency, 3-Phase, Triple Synchronous DC/DC Step-Down Controller

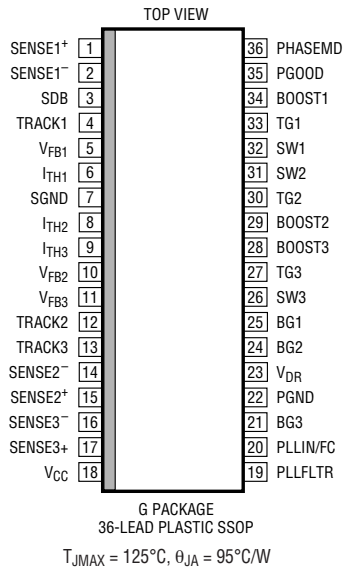


ABSOLUTE MAXIMUM RATINGS (Note 1)

Topside Driver Voltage (BOOSTn) ..... 42V to –0.3V
Switch Voltage (SWn) ..... 36V to –1V
Boosted Driver Voltage (BOOSTn – SWn) .... 7V to –0.3V
Supply Voltages (V_{CC}, V_{DR}) ..... 7V to –0.3V
PGOOD, PHASEMD, PLLFLTR, PLLIN/FC, SDBn,
TRACKn, V_{FB}n ..... (V_{CC} + 0.3V) to –0.3V
SENSE$^+$n, SENSE$^-$n ..... (1.1 • V_{CC}) to –0.3V
I_{THn} Voltage ..... 2.7V to –0.3V

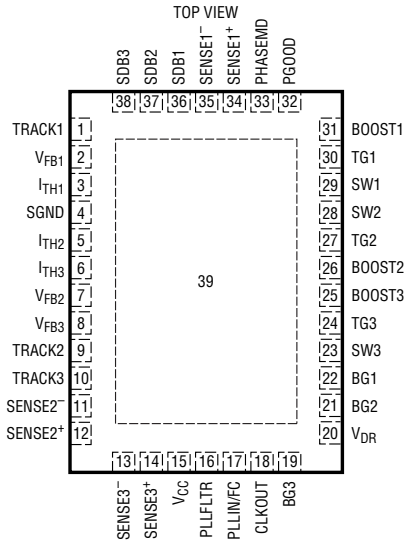
Extended Commercial Operating
Temperature Range (Note 2) ..... –40°C to 85°C
Junction Temperature (Note 2) ..... 125°C
Storage Temperature Range ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec)
G Package ..... 300°C
Peak Body Temperature UHF Package ..... 240°C

PIN CONFIGURATIONS



G PACKAGE
36-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 95°C/W



UHF PACKAGE
38-LEAD (5mm × 7mm) PLASTIC QFN
EXPOSED PAD IS PGND (PIN 39),
MUST BE SOLDERED TO PCB

T_{JMAX} = 125°C, θ_{JA} = 34°C/W

ORDERING INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3773EG#PBF	LTC3773EG#TRPBF		36-Lead Plastic SSOP	–40°C to 85°C
LTC3773EUHF#PBF	LTC3773EUHF#TRPBF	3773E	38-Lead (5mm x 7mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

(Note 3) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = V_{DR} = V_{BOOST} = V_{SDB} = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
V_{FB}	Feedback Voltage	V_{ITH} = 1.2V, 0°C ≤ T ≤ 85°C (Note 4)	 ●	0.594 0.591	0.600 0.600	0.606 0.609	V V
I_{VFB}	Feedback Pin Input Current	0 ≤ V_{FB} ≤ 1V			–15	–100	nA
$V_{SENSEMAX}$	Maximum Current Sense Threshold	V_{FB} = 0.55V, V_{TRACK} = 1V, V_{SENSE}^- = 2.5V	 ●	65 60	75 75	85 90	mV mV
$V_{FBLOADREG}$	Feedback Voltage Load Regulation	Measured in Servo Loop (Note 4) Δ_{ITH} Voltage = 1.2V to 0.7V Δ_{ITH} Voltage = 1.2V to 2V	 ● ●		 0.15 –0.2	 0.5 –0.5	 % %
$V_{FBLNREG}$	Feedback Voltage Line Regulation	V_{CC} = 4.5V to 6V			0.01		%/V
g_m	Transconductance Amplifier g_m	V_{ITH} = 1.2V, Sink/Source 25µA (Note 4)	●	2.3	2.7	3.2	mmho
f_u	Transconductance Amplifier GBW	V_{ITH} = 1.2V (Note 5)			3		MHz
A_{ERR}	Transconductance Amplifier DC Gain	V_{ITH} = 0.8V to 1.6V	●	50	56		dB
V_{UVR}	V_{CC} Undervoltage Reset Undervoltage Hysteresis	V_{CC} Ramping Positive		3.7	4.1 0.16	4.4	V V
V_{CC}	V_{CC} Supply Voltage		●	4.5	5	6	V
I_{VCC}	V_{CC} Supply Current Normal Mode Shutdown	 V_{CC} = 5V V_{SDB} = 0V			 2.8 20	 4 30	 mA µA
I_{VDR}	V_{DR} Supply Current Normal Mode Shutdown	 V_{DR} = 5V (Note 6) V_{SDB} = 0V			 5 1		 mA µA
I_{BOOST}	V_{BOOST} Supply Current Normal Mode Shutdown	 V_{BOOST} = 5V, V_{SW} = 0V (Note 6) V_{SDB} = 0V			 1 1		 mA µA
I_{SDB}	SDB Source Current SDB1, SDB2, SDB3 Source Content				–1.5 –0.5		µA µA
V_{SDB}	SDB Power Up Threshold SDB1 Pin CH1 ON Threshold SDB2 Pin CH2 ON Threshold SDB3 Pin CH3 ON Threshold	Ramping Positive	● ● ● ●	0.4 1.14 1.71 2.3	 1.2 1.8 2.4	 1.26 1.89 2.5	V V V V
	Channel On Threshold Hysteresis				–10		%
I_{SENSE}	SENSE Pins Source Current	V_{SENSE}^+, V_{SENSE}^- = 1.2V, Current at Each Pin			–13	–20	µA
DF_{MAX}	Maximum Duty Factor	PLLFLTR Floats, In Dropout		97	98.5		%
TG R_{UP}	TG Driver Pull-Up On-Resistance	TG High, I_{OUT} = 100mA (Note 7)			2.2		Ω
TG R_{DOWN}	TG Driver Pull-Down On-Resistance	TG Low, I_{OUT} = 100mA (Note 7)			1.8		Ω
BG R_{UP}	BG Driver Pull-Up On-Resistance	BG High, I_{OUT} = 100mA (Note 7)			2.4		Ω
BG R_{DOWN}	BG Driver Pull-Down On-Resistance	BG Low, I_{OUT} = 100mA (Note 7)			0.9		Ω
TG/BG t_{1D}	Top Gate OFF to Bottom Gate ON Delay Synchronous Switch-On Delay Time	All Controllers			50		ns
BG/TG t_{2D}	Bottom Gate OFF to Top Gate ON Delay Top Switch-On Delay Time	All Controllers			50		ns
$t_{ON(MIN)}$	Minimum On-Time	Tested with a Square Wave (Note 8)			130		ns
Tracking							
I_{TRACK}	TRACK Pin Pull-Up Current	V_{SDB} = 5V, V_{TRACK} = 0V			–1		µA
$V_{FBTRACK}$	V_{FB} Voltage During Tracking	V_{TRACK} = 0.2V, V_{ITH} = 1.2V (Note 4) V_{TRACK} = 0.4V, V_{ITH} = 1.2V (Note 4)		180 380	200 400	220 420	mV mV

ELECTRICAL CHARACTERISTICS

(Note 3) The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = V_{DR} = V_{BOOST} = V_{SDB} = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Good Output Indication							
V_{PGL}	PGOOD Voltage Output Low	I_{PGOOD} = 2mA			0.1	0.3	V
I_{PGOOD}	PGOOD Output Leakage	V_{PGOOD} = 5V				1	µA
$V_{PGTHNEG}$ $V_{PGTHPOS}$	PGOOD Trip Thresholds V_{FB} Ramping Negative V_{FB} Ramping Positive	V_{FB} with Respect to 0.6V Reference PGOOD Goes Low After V_{PGDLY} Delay		 –7 7	 –10 10	 –13 13	 % %
V_{PGDLY}	PGOOD Delay			100	150		µs
Oscillator and Phase-Locked Loop							
f_{NOM}	Nominal Frequency	$V_{PLLFLTR}$ Open		360	400	440	kHz
f_{LOW}	Low Frequency	$V_{PLLFLTR}$ = 0V		190	220	250	kHz
f_{HIGH}	High Frequency	$V_{PLLFLTR}$ = 5V		510	560	630	kHz
f_{PLLLOW}	PLLIN Minimum Input Frequency				160	200	kHz
$f_{PLLHIGH}$	PLLIN Maximum Input Frequency			540	700		kHz
V_{LO} V_{FLOAT} V_{HI}	PLLIN/FC, PHASEMD, PLLFLTR Logic Input Low Level Input Voltage Floating Voltage High Level Input Voltage				 1.0 1.6 3.0		 V V V
V_{PLLIN}	PLLIN Synchronization Input Threshold				1		V
$I_{PLLFLTR}$	Phase Detector Output Current Sinking Capability Sourcing Capability	$V_{PLLFLTR}$ = 1.5V $f_{PLLIN} < f_{OSC}$ $f_{PLLIN} > f_{OSC}$			 25 –25		 µA µA
P_{RELPHS}	Controller 2 - Controller 1 Phase Controller 3 - Controller 1 Phase	PHASEMD Floats or $V_{PHASEMD}$ = 0V			120 240		Deg Deg
	Controller 2 - Controller 1 Phase Controller 3 - Controller 1 Phase	$V_{PHASEMD}$ = 5V			90 270		Deg Deg
CLKOUT	Controller 1 TG to CLKOUT Phase	PHASEMD Floats $V_{PHASEMD}$ = 0V $V_{PHASEMD}$ = 5V			0 60 180		Deg Deg Deg

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3773 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula.

LTC3773EG: $T_J = T_A + (P_D \times 95°C/W)$

LTC3773EUHF: $T_J = T_A + (P_D \times 34°C/W)$

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: The IC is tested in a feedback loop that adjusts V_{FB} to achieve a specified error amplifier output voltage (V_{ITH}).

Note 5: Guaranteed by design, not subject to test.

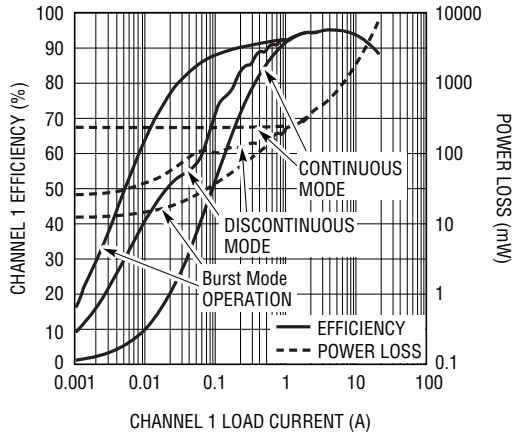
Note 6: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

Note 7: $R_{DS(ON)}$ limit is guaranteed by design and/or correlation to static test.

Note 8: The minimum on-time condition corresponds to an inductor peak-to-peak ripple current of ≥40% of I_{MAX} (see minimum on-time considerations in the Applications Information section).

TYPICAL PERFORMANCE CHARACTERISTICS

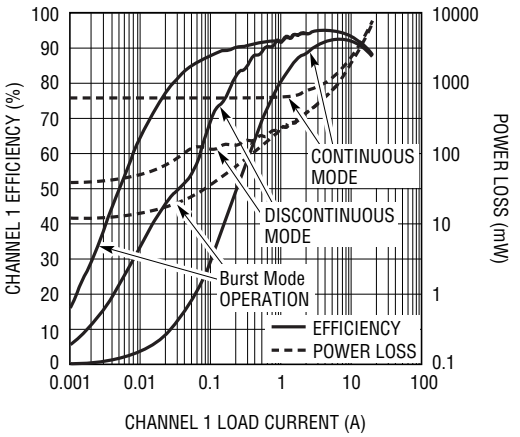
Efficiency vs Load Current, Shutdown CH2 and CH3



V_{IN} = 12V, V_{CC} = 5V, V_{OUT1} = 2.5V
f_{SW} = 220kHz

3773 G01

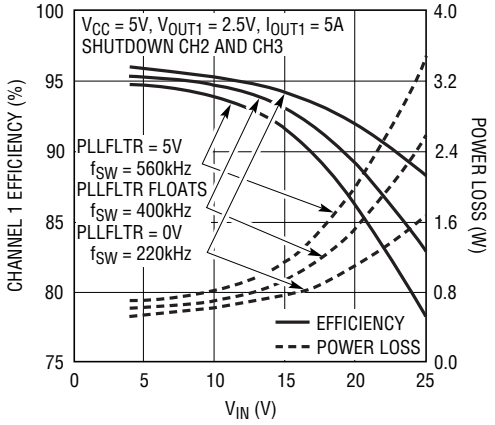
Efficiency vs Load Current, Power-Up CH2 and CH3



V_{IN} = 12V, V_{CC} = 5V, V_{OUT1} = 2.5V
V_{OUT2} = 1.8V (NO LOAD), V_{OUT3} = 1.2V (NO LOAD)
f_{SW} = 220kHz

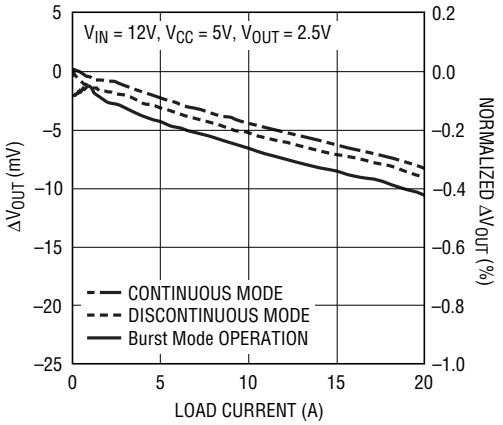
3773 G02

Efficiency vs V_{IN} Shutdown CH2 and CH3



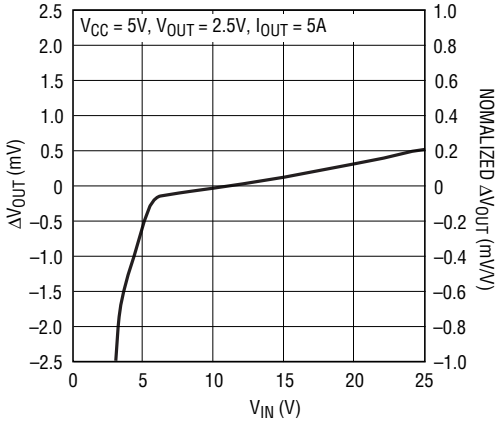
3773 G03

Load Regulation



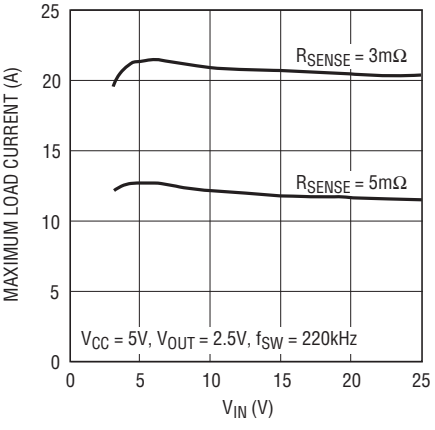
3773 G04

Line Regulation



3773 G05

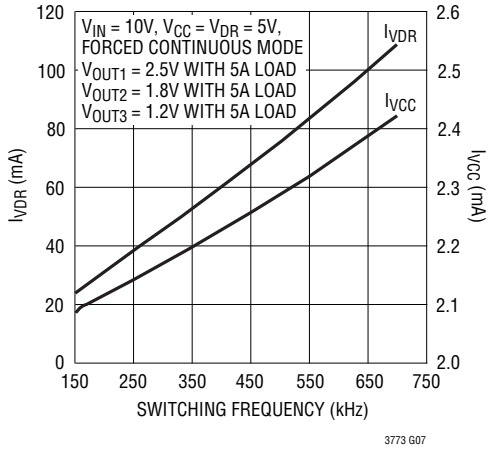
Current Limit vs V_{IN}



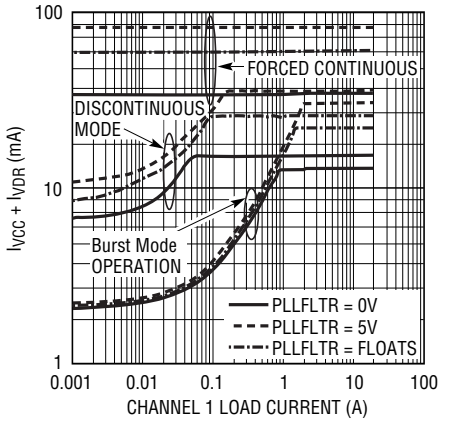
3773 G06

TYPICAL PERFORMANCE CHARACTERISTICS

I_{VDR} and I_{VCC} vs Switching Frequency

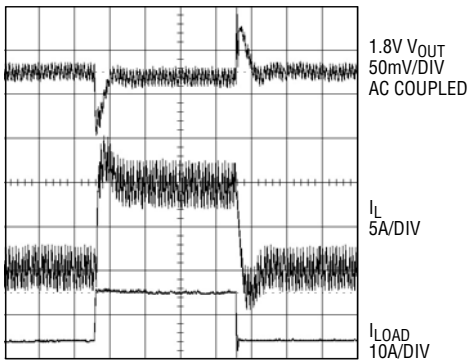


I_{VCC} and I_{VDR} vs Load Current



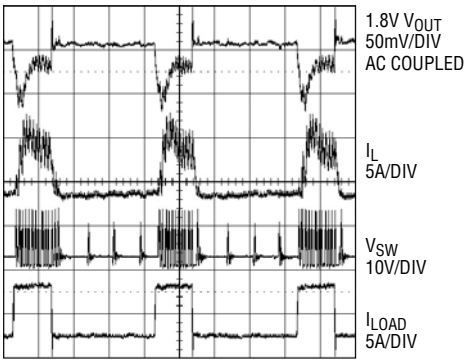
V_{IN} = 12V, V_{CC} = V_{DR} = 5V, V_{OUT1} = 2.5V
V_{OUT2} = 1.8V (NO LOAD), V_{OUT3} = 1.2V (NO LOAD)

Forced Continuous Mode 0A to 10A Load Step



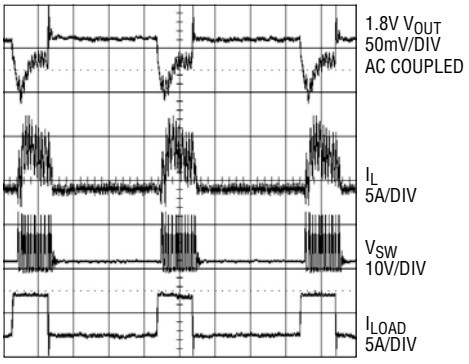
V_{IN} = 12V, f_{SW} = 220kHz

Discontinuous Mode 0A to 5A Load Step at 5kHz Interval



V_{IN} = 12V, f_{SW} = 220kHz

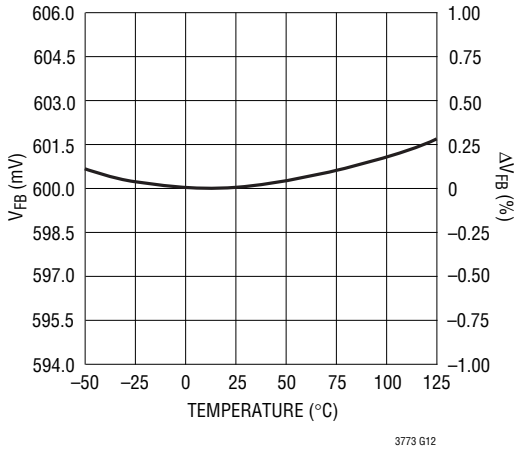
Burst Mode Operation 0A to 5A Load Step at 5kHz Interval



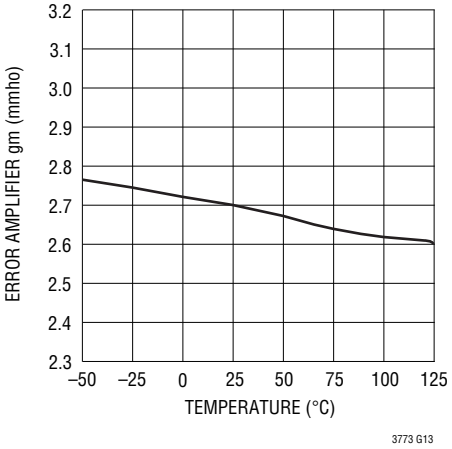
V_{IN} = 12V, f_{SW} = 220kHz

TYPICAL PERFORMANCE CHARACTERISTICS

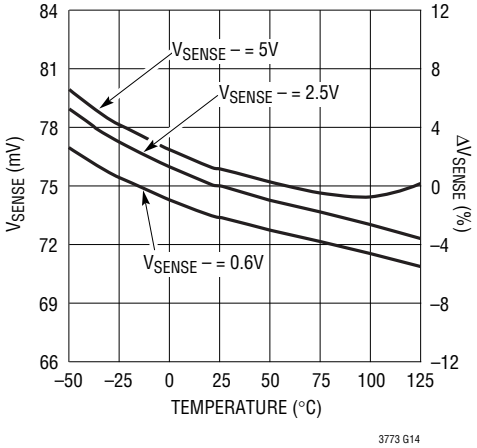
V_{FB} vs Temperature



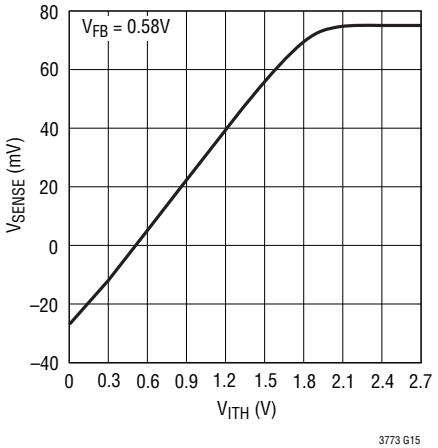
Error Amplifier gm vs Temperature



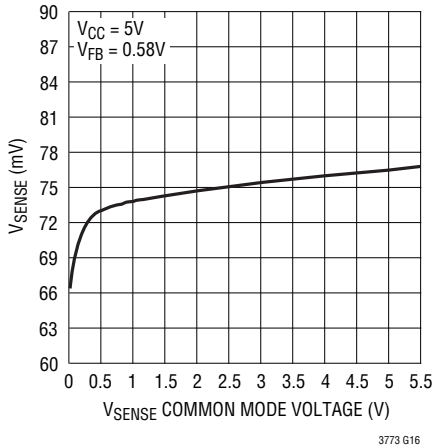
Maximum Current Limit Threshold vs Temperature



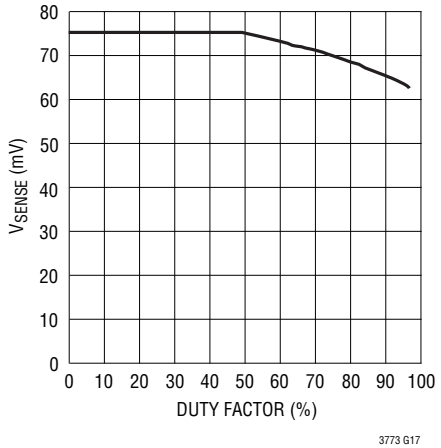
Maximum Current Limit Threshold vs V_{ITH}



Maximum Current Limit Threshold vs SENSE Common Mode Voltage

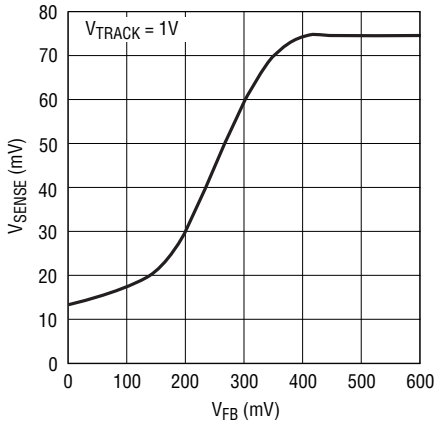


Maximum Current Limit Threshold vs Duty Factor



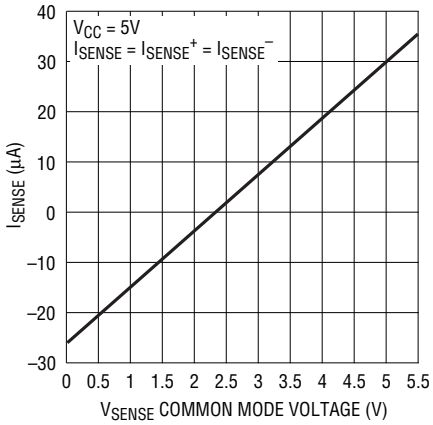
TYPICAL PERFORMANCE CHARACTERISTICS

Maximum Current Limit Threshold vs V_{FB}



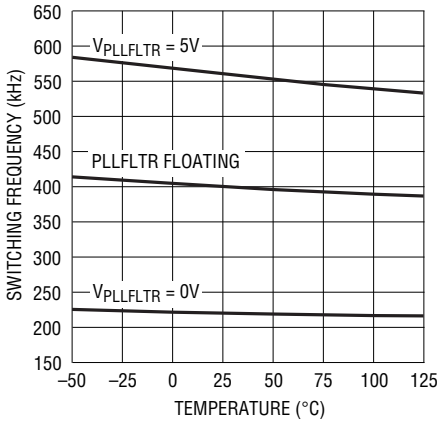
3773 G18

SENSE Pin Input Current vs SENSE Common Mode Voltage



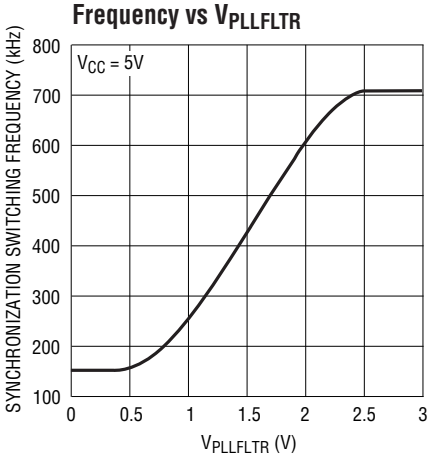
3773 G19

Switching Frequency vs Temperature



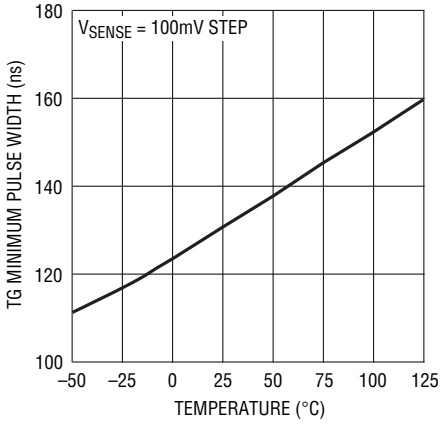
3773 G20

Synchronization Switching Frequency vs $V_{PLLFLTR}$



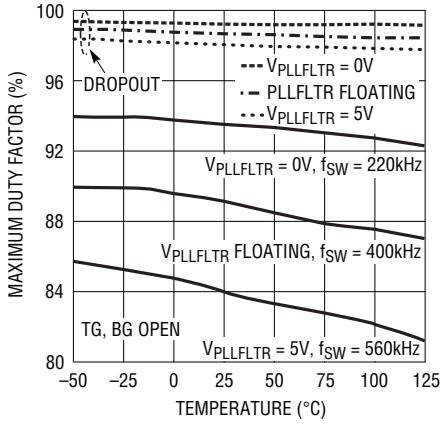
3773 G21

TG Minimum Pulse Width vs Temperature



3773 G22

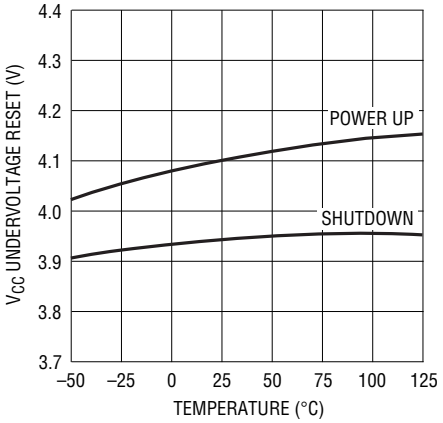
Maximum Duty Factor vs Temperature



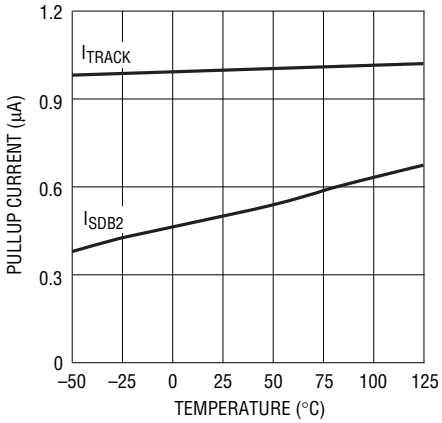
3773 G23

TYPICAL PERFORMANCE CHARACTERISTICS

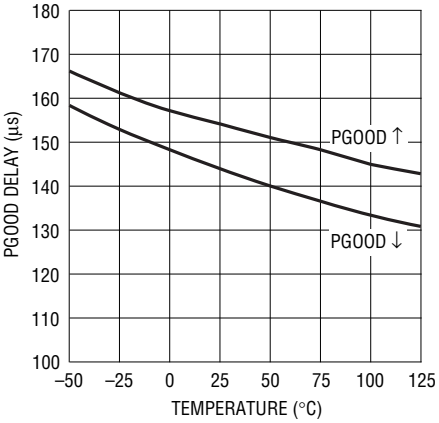
V_{CC} Undervoltage Reset Voltage vs Temperature



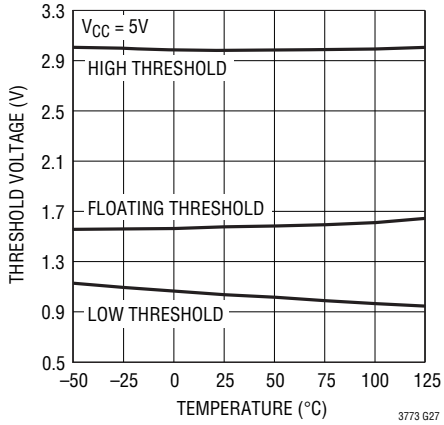
TRACK and SDB Pull-Up Current vs Temperature



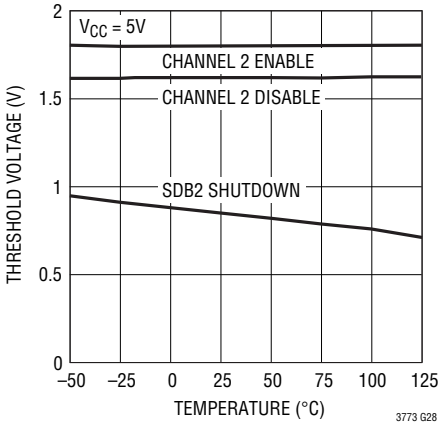
PGOOD Delay vs Temperature



PLLIN/FC, PHASEMD, PLLFLTR, Threshold Voltage vs Temperature



SDB2 Threshold Voltage vs Temperature



PIN FUNCTIONS (G/UHF)

SENSE1$^+$ (Pin 1/Pin 34): The (+) Input to the Channel 1 Differential Current Comparator. The I_{TH1} pin voltage and controlled offsets between the SENSE1$^-$ and SENSE1$^+$ pins in conjunction with R_{SENSE} set the channel 1 current trip threshold.

SENSE1$^-$ (Pin 2/Pin 35): The (–) Input to the Channel 1 Differential Current Comparator.

SDB/SDB1, SDB2, SDB3 (Pin 3/Pins 36, 37, 38): Shutdown, Active Low. For G package, SDB1, SDB2 and SDB3 are shorted at the SDB pin. The power up thresholds for channel 1, 2 and 3 are set at 1.2V, 1.8V and 2.4V respectively. By pulling the SDB1, SDB2 and SDB3 pins below 0.4V, the IC is put into low current shutdown mode (I_{VCCQ} <30µA). There is a 0.5µA pull-up current at each SDB pin. An external capacitor can be added at this pin to provide power up delay.

TRACK1 (Pin 4/Pin 1): Channel 1 Tracking Input. TRACK1 is used for tracking multiple LTC3773s. See the Startup Tracking application. To disable this feature, float this pin or tie it to V_{CC}. TRACK1 provides a 1µA pull-up current. An external capacitor can be added at this pin to provide soft-start. During startup or output short-circuit condition, if the potential at TRACK1 is less than 0.54V, current limit foldback is disabled. When channel 1 is powered down, this pin will be pulled low.

V_{FB1} (Pin 5/Pin 2): Channel 1 Error Amplifier Feedback Input. This pin connects the error amplifier input to an external resistive divider from V_{OUT1}.

I_{TH1} (Pin 6/Pin 3): Channel 1 Error Amplifier Output and Switching Regulator Compensation Point. The current comparator's threshold increases with this control voltage.

SGND (Pin 7/Pin 4): Signal Ground. This pin must be routed separately under the IC to the PGND pin and then to the main ground plane.

I_{TH2} (Pin 8/Pin 5): Channel 2 Error Amplifier Output and Switching Regulator Compensation Point. See I_{TH1}.

I_{TH3} (Pin 9/Pin 6): Channel 3 Error Amplifier Output and Switching Regulator Compensation Point. See I_{TH1}.

V_{FB2} (Pin 10/Pin 7): Channel 2 Error Amplifier Feedback Input. See V_{FB1}.

V_{FB3} (Pin 11/Pin 8): Channel 3 Error Amplifier Feedback Input. See V_{FB1}.

TRACK2 (Pin 12/Pin 9): Channel 2 Tracking Input. Tie the TRACK2 pin to a resistive divider connected to the output of channel 1 for either coincident or ratiometric output tracking. See the Soft-Start/Tracking application. TRACK2 comes with a 1µA pull-up current. An external capacitor can be added at this pin to provide soft-start. During startup or output short-circuit condition, if the potential at TRACK2 is less than 0.54V, current limit foldback is disabled. When channel 2 is powered down, this pin will be pulled low.

TRACK3 (Pin 13/Pin 10): Channel 3 Tracking Input. See TRACK2.

SENSE2$^-$ (Pin 14/Pin 11): The (–) Input to the Channel 2 Differential Current Comparator. See SENSE1$^-$.

SENSE2$^+$ (Pin 15/Pin 12): The (+) Input to the Channel 2 Differential Current Comparator. See SENSE1$^+$.

SENSE3$^-$ (Pin 16/Pin 13): The (–) Input to the Channel 3 Differential Current Comparator. See SENSE1$^-$.

SENSE3$^+$ (Pin 17/Pin 14): The (+) Input to the Channel 3 Differential Current Comparator. See SENSE1$^+$.

V_{CC} (Pin 18/Pin 15): Main Input Supply. All internal circuits except the output drivers are powered from this pin. V_{CC} should be connected to a low noise 5V power supply and should be bypassed to SGND with at least a 1µF capacitor in close proximity to the LTC3773.

PLLFLTR (Pin 19/Pin 16): Phase-Locked Loop Lowpass Filter. The phase-locked loop's lowpass filter is tied to this pin. Alternatively, when external frequency synchronizing is not used, this pin can be forced low, left floating or tied high to vary the frequency of the internal oscillator.

PIN FUNCTIONS (G/UHF)

PLLIN/FC (Pin 20/Pin 17): Synchronization Input to the Phase Detector and Forced Continuous Control Input. When floating, it sits around 1.6V, and the controller enters discontinuous mode operation at light load. Shorting this pin low or high for more than 20µs enables Burst Mode operation or forced continuous current mode operation, respectively. During frequency synchronization, the phase locked loop will force the controller to operate in continuous mode and the rising top gate signal of controller 1 to be synchronized with the rising edge of the PLLIN signal. When synchronization is not required, it is advisable to bypass the PLLIN/FC pin with a 1000pF capacitor to avoid noise coupling.

CLKOUT (Pin 18 UHF Only): CLK Output. Output clock signal available to synchronize other controller ICs for additional MOSFET controller stages/phases.

BG3 (Pin 21/Pin 19): Channel 3 Bottom Gate Drive. See BG1.

PGND (Pin 22/Pin 39): Driver's Power Ground. This pin connects directly to the sources of the bottom N-channel external MOSFETs and the (–) terminals of C_{IN}. The backside exposed pad (QFN) must be soldered to PCB ground.

V_{DR} (Pin 23/Pin 20): Driver Supply. Provides supply to the drivers for the bottom gates. Also used for charging the bootstrap capacitors. This pin needs to be very carefully and closely decoupled to the IC's PGND pin. If the V_{DR} potential is lower than V_{CC} potential by 1V, the drivers will be disabled.

BG2 (Pin 24/Pin 21): Channel 2 Bottom Gate Drive. See BG1.

BG1 (Pin 25/Pin 22): Channel 1 Bottom Gate Drive. Drives the gate of the bottom N-channel MOSFET between ground and V_{DR}.

SW3 (Pin 26/Pin 23): Channel 3 Switching Node. See SW1.

TG3 (Pin 27/Pin 24): Channel 3 Top Gate Drive. See TG1.

BOOST3 (Pin 28/Pin 25): Channel 3 Top Gate Driver Supply. See BOOST1.

BOOST2 (Pin 29/Pin 26): Channel 2 Top Gate Driver Supply. See BOOST1.

TG2 (Pin 30/Pin 27): Channel 2 Top Gate Drive. See TG1.

SW2 (Pin 31/Pin 28): Channel 2 Switching Node. See SW1.

SW1 (Pin 32/Pin 29): Channel 1 Switching Node. The (–) terminal of the bootstrap capacitor connects here. This pin swings from a Schottky diode (external) voltage drop below ground to V_{IN} (where V_{IN} is the external MOSFET supply rail).

TG1 (Pin 33/Pin 30): Channel 1 Top Gate Drive. The TG1 pin drives the top N-channel MOSFET with a voltage swing equal to V_{DR} superimposed on the switch node voltage SW.

BOOST1 (Pin 34/Pin 31): Channel 1 Top Gate Driver Supply. The (+) terminal of the bootstrap capacitor connects here. This pin swings from approximately V_{DR} up to $V_{IN} + V_{DR}$ (where V_{IN} is the external MOSFET supply rail).

PGOOD (Pin 35/Pin 32): Open Drain Power Good Output. This open-drain output is pulled low during shutdown or when any of the three output voltages has been outside the PGOOD tolerance window for more than 100µs.

PHASEMD (Pin 36/Pin 33): Phase Select Input. This pin controls the phase relationship between controller 1, controller 2, controller 3 and CLKOUT. When PHASEMD is floating, its value is around 1.6V, the three channels switch 120° out of phase, and CLKOUT synchronizes to the rising edge of TG1. When PHASEMD is grounded, TG1 leads CLKOUT by 60°. When PHASEMD is shorted to V_{CC}, TG1 leads TG2, TG3, and CLKOUT by 90°, 270° and 180°, respectively.

FUNCTIONAL DIAGRAM

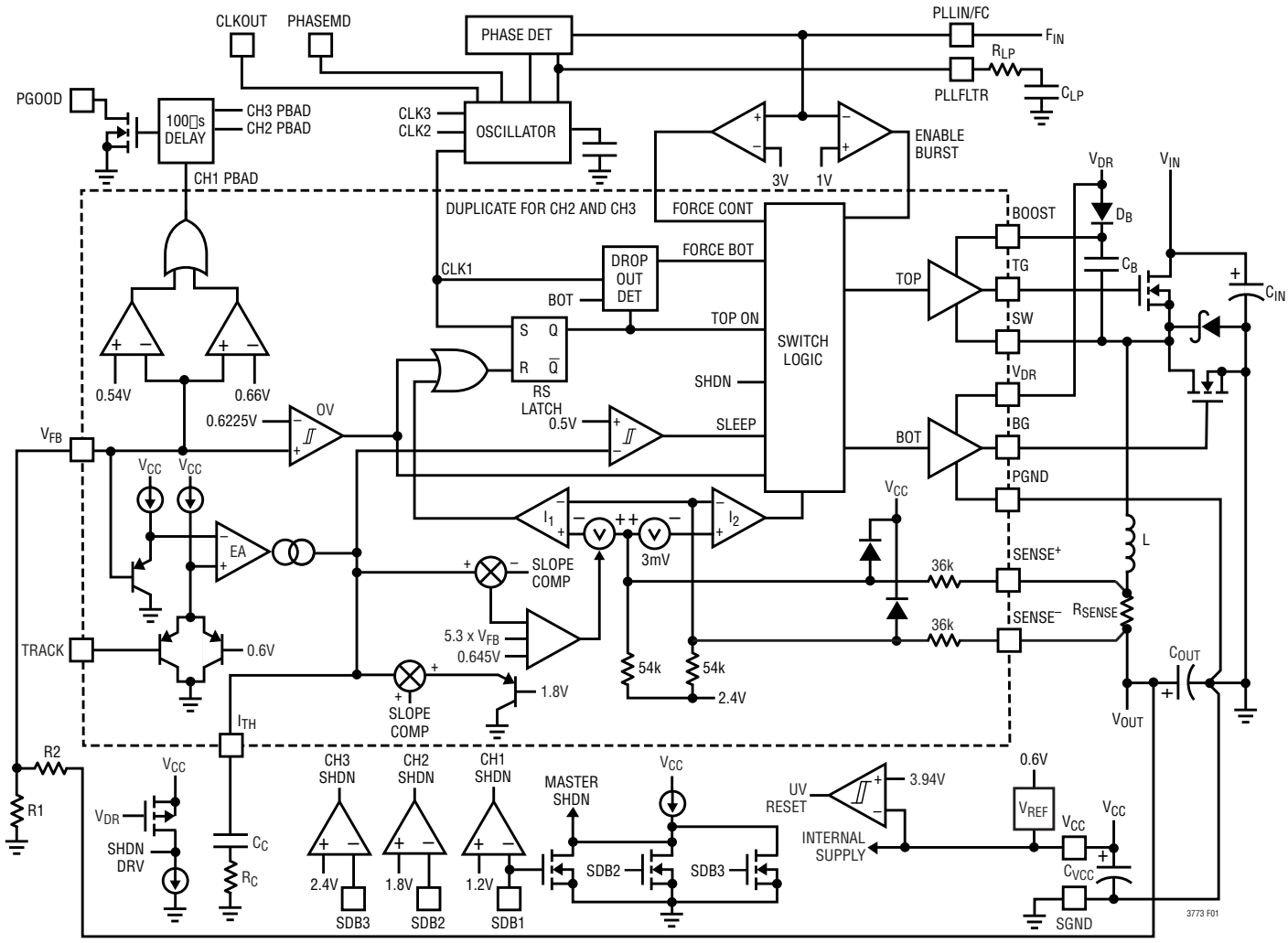


Figure 1. Functional Diagram

OPERATION (Refer to the Functional Diagram)

Main Control Loop

The LTC3773 uses a constant frequency, current mode step down architecture. During normal operation, each top MOSFET is turned on each cycle when the oscillator sets the RS latch, and turned off when the main current comparator, I_1, resets the RS latch. The peak inductor current at which I_1 resets the RS latch is controlled by the voltage on the I_{TH} pin, which is the output of the error amplifier EA. The error amplifier input pin, V_{FB}, receives the output voltage feedback signal from an external resistor divider. This feedback signal is compared to the internal 0.6V reference voltage by the EA. When the load current increases it causes a slight decrease in V_{FB} relative to the 0.6V reference, which in turn causes the I_{TH} voltage to increase until the average inductor current matches the new load current. While the top N-channel MOSFET is off, the bottom N-channel MOSFET is turned on until either the next cycle begins or the inductor current starts to reverse, as indicated by the current reversal comparator, I_2.

The top MOSFET drivers are biased from floating bootstrap capacitor C_B, which is normally recharged during each off cycle through an external Schottky diode. When V_{IN} decreases to a voltage close to V_{OUT}, however, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector counts the number of oscillator cycles that the bottom MOSFET remains off and periodically triggers a brief refresh pulse to recharge C_B.

Shutdown, Soft-Start and Tracking Startup

The main control loop is enabled by allowing the SDBn pin to go high. In the G package, SDB1, SDB2 and SDB3 are shorted together at the SDB pin. The power-up thresholds for channels 1, 2 and 3 are set at 1.2V, 1.8V and 2.4V respectively. By forcing the SDB1, SDB2 and SDB3 pins below 0.4V, the IC enters low current shutdown mode, and the chip draws less than 30µA. Releasing SDBn allows an internal 0.5µA current source to pull up the SDBn pin. If a resistive divider connected to V_{IN} drives the SDB pin, the controller will automatically start up when V_{IN} is fully powered up.

The start-up of V_{OUT} is controlled by the LTC3773's TRACK pin. An external capacitor at the TRACK pin provides the soft-start function. During soft-start, the error amplifier EA compares the feedback signal, V_{FB}, to the TRACK pin's potential (instead of the 0.6V reference), which rises linearly from 0V to 0.6V. This allows the output voltage to rise smoothly from 0V to its final value while maintaining control of the inductor current. When the potential at the TRACK pin approaches the 0.6V reference voltage, the control loop servos V_{FB} to the internal reference. The TRACK pin can also be used for power up/down tracking. A resistor divider on V_{OUT1} connected to the TRACK2/TRACK3 pin allows the startup of V_{OUT2}/V_{OUT3} to track that of V_{OUT1} (refer to the Soft-Start/Tracking section for more detail).

Low Current Operation

The PLLIN/FC pin is a multifunction pin: 1) an external clock input for PLL synchronization, and 2) a logic input to select between three modes of operation.

A) Continuous Current Operation: When the PLLIN/FC pin voltage is above 3V or driven by an external oscillator, the controller performs as a continuous, PWM current mode synchronous switching regulator. The top and bottom MOSFETs are alternately turned on to maintain the output voltage independent of direction of inductor current. This is the least efficient light load operating mode, but has lowest output ripple. The output can source or sink current in this mode. When sinking current while in forced continuous operation, the controller can cause current to flow back into the input supply filter capacitor. Be sure to use an input capacitor with enough capacitance to prevent the input voltage from boosting too high. See C_{IN} and C_{OUT} Selection in the Applications Information section. Certain applications must not allow continuous operation at startup with prebiased output or power down; this can be easily avoided by shorting the PGOOD output to the PLLIN/FC pin. The controller will be forced to operate in Burst Mode until all three outputs are within 10% of their nominal values.

B) Burst Mode Operation: When the PLLIN/FC pin voltage is below 1V and the regulated output voltage is within 10% of its nominal value, the controller behaves

OPERATION (Refer to the Functional Diagram)

as a Burst Mode switching regulator. Burst Mode operation clamps the minimum peak inductor current to approximately 20% of the current limit programmed by R_{SENSE}. As the load current goes down, the EA will reduce the voltage on the I_{TH} pin. When the I_{TH} voltage drops below 0.5V, the internal SLEEP signal goes high and both external MOSFETs are turned off.

In Burst Mode operation, the load current is supplied by the output capacitor. As the output voltage falls, the I_{TH} voltage rises. When the I_{TH} voltage reaches 0.55V, the SLEEP signal goes low and the controller resumes normal operation by turning on the external top MOSFET at the next cycle of the internal oscillator. During Burst Mode operation, the inductor current is not allowed to reverse.

C) Discontinuous Mode Operation: When the PLLIN/FC pin is floating, Burst Mode operation is disabled but the inductor current is not allowed to reverse. The 20% minimum inductor current clamp present in Burst Mode operation is removed, providing constant frequency discontinuous operation over the widest possible output current range. This constant frequency operation is not quite as efficient as Burst Mode operation, but provides a lower noise, constant frequency spectrum.

Frequency Synchronization

The selection of switching frequency is a trade off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

The phase-locked loop allows the internal oscillator to be synchronized to an external source using the PLLIN/FC pin. The output of the phase detector at the PLLFLTR pin is also the DC frequency control input of the oscillator, which operates over a 160kHz to 700kHz range corresponding to a voltage input from 0V to 2.5V. When locked, the PLL aligns the turn on of the controller 1 top MOSFET to the rising edge of the synchronizing signal.

When PLLIN/FC is not being driven by an external clock source, the PLLFLTR can be floated, tied to V_{CC} or SGND to select 400kHz, 560kHz or 220kHz switching frequency, respectively.

Power Good

The PGOOD pin is connected to the drain of an internal N-channel MOSFET. The MOSFET is turned on under shutdown state or if any regulator output voltage has been away from its nominal value by greater than 10% for more than 100µs. To shut off this MOSFET, all three regulator output voltages must be within the ±10% window for more than 100µs.

Short-Circuit Protection and Current Foldback

Upon start-up, the soft-start action at the TRACK pin limits the inrush current from the input power source; yet the controller provides the maximum rated output current to charge up the output capacitor as quickly as possible. If TRACK ramps above 0.54V but the output voltage is less than 70% of its nominal value, foldback current limiting is activated on the assumption that the output is in a severe overcurrent and/or short-circuit condition.

Output Overvoltage Protection

As a further protection, the overvoltage comparator (OV) guards against transient overshoots, as well as other more serious conditions that may overvoltage the output. When the feedback voltage on the V_{FB} pin has risen 3.75% above the reference voltage of 0.6V, the top gate is turned off and the bottom gate is turned on until the overvoltage is cleared.

Undervoltage Lockout

To prevent operation of the external MOSFETs below safe V_{CC} supply levels, an undervoltage lockout is incorporated in the LTC3773. When V_{CC} drops below 3.9V, the MOSFET drivers and all internal circuitry are turned off except for the undervoltage block and SDB input circuitry. If V_{DR} is lower than V_{CC} by more than 1V, the drivers are disabled.

APPLICATIONS INFORMATION

The basic application circuit is shown on the first page of this data sheet. External component selection is driven by the load requirement, and normally begins with the selection of an inductance value based upon the desired operating frequency, inductor current and output voltage ripple requirements. Once the inductors and operating frequency have been chosen, the current sensing resistors can be calculated. Next, the power MOSFETs and Schottky diodes are selected. Finally, C_{IN} and C_{OUT} are selected according to the required voltage ripple requirements. The circuit on the front page can be configured for operation up to a MOSFET supply voltage of 36V (limited by the external MOSFETs, V_{IN} capacitor voltage rating and possibly the minimum on-time).

Operating Frequency and Synchronization

The choice of operating frequency, f_{OSC}, is a trade-off between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses, both gate charge loss and transition loss. However, lower frequency operation requires more inductance for a given amount of ripple current. The internal oscillator for each of the LTC3773's controllers runs at a nominal 400kHz frequency when the PLLFLTR pin is left floating and the PLLIN/FC pin input is not switching. Pulling PLLFLTR to V_{CC} selects 560kHz operation; pulling PLLFLTR to SGND selects 220kHz operation. Alternatively, the LTC3773 will phase-lock to a clock signal applied to the PLLIN/FC pin with a frequency between 160kHz and 700kHz (see Phase-Locked Loop and Frequency Synchronization).

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET gate-charge losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered. The inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L decreases with higher inductance or frequency and increases with higher V_{IN} or V_{OUT}:

$$\Delta I_L = \frac{V_{OUT}}{(f)(L)}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is ΔI_L = 0.3 to 0.6 (I_{MAX}). Remember, the maximum ΔI_L occurs at the maximum input voltage. The inductor value also has an effect on low current operation. The transition to low current operation begins when the inductor current reaches zero while the bottom MOSFET is on. Burst Mode operation begins when the average inductor current required results in a peak current below 20% of the current limit determined by R_{SENSE}. Lower inductor values (higher ΔI_L) will cause this to occur at higher load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to decrease.

Inductor Core Selection

Once the inductance value is determined, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper (I^2R) losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so designers can concentrate on reducing I^2R loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and do not radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use

APPLICATIONS INFORMATION

mainly depends on the price vs size requirements and any radiated field/EMI requirements. New designs for high current surface mount inductors are available from numerous manufacturers, including Coiltronics, Vishay, TDK, Pulse, Panasonic, Vitec, Coilcraft, Toko and Sumida.

Power MOSFET and Schottky Diode Selection

At least two external power MOSFETs must be selected for each of the three output sections: One N-channel MOSFET for the top (main) switch and one or more N-channel MOSFET(s) for the bottom (synchronous) switch. The number, type and on-resistance of all MOSFETs selected take into account the voltage step-down ratio as well as the actual position (main or synchronous) in which the MOSFET will be used. A much smaller and much lower input capacitance MOSFET should be used for the top MOSFET in applications that have an output voltage that is less than 1/3 of the input voltage. In applications where $V_{IN} >> V_{OUT}$, the top MOSFETs' on-resistance is normally less important for overall efficiency than its input capacitance at operating frequencies above 300kHz. MOSFET manufacturers have designed special purpose devices that provide reasonably low on-resistance with significantly reduced input capacitance for the main switch application in switching regulators.

The peak-to-peak MOSFET gate drive levels are set by the driver supply voltage, V_{DR}, requiring the use of logic-level threshold MOSFETs in most applications. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; many of the logic-level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the on-resistance $R_{DS(ON)}$, input capacitance, input voltage and maximum output current. MOSFET input capacitance is a combination of several components but can be taken from the typical "gate charge" curve included on most data sheets as shown in Figure 2. The curve is generated by forcing a constant input current into the gate of a common source, current source loaded stage and then plotting the gate voltage versus time. The initial slope is the effect of the gate-to-source and the gate-to-drain capacitance. The flat portion of the curve is the result of the Miller multiplication effect of the drain-to-gate capacitance as the drain drops the voltage across the current source load. The upper sloping line is due to the drain-to-gate accumulation capacitance and the gate-to-source capacitance.

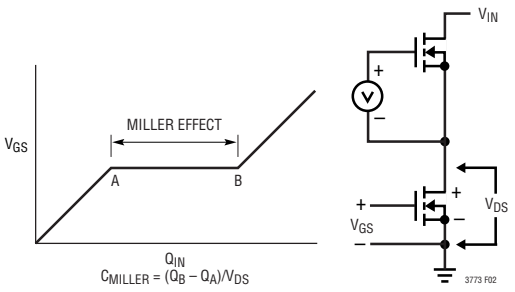


Figure 2. MOSFET Miller Capacitance

The Miller charge (the increase in coulombs on the horizontal axis from A to B while the curve is flat) is specified for a given V_{DS} drain voltage, but can be adjusted for different V_{DS} voltages by multiplying by the ratio of the application V_{DS} to the curve specified V_{DS} values. A way to estimate the C_{MILLER} term is to take the change in gate charge from points A and B on a manufacturers data sheet and divide by the stated V_{DS} voltage specified. C_{MILLER} is the most important selection criterion for determining the transition loss term in the top MOSFET but is not directly specified on MOSFET data sheets. C_{RSS} and C_{OS} are specified sometimes but definitions of these parameters are not included.

When the controller is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The power dissipation for the main and synchronous MOSFETs at maximum output current is given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}(I_{MAX}{}^2)(1+\delta)R_{DS(ON)} + V_{IN}{}^2\frac{I_{MAX}}{2}(R_{DR})(C_{MILLER})\bullet\left[\frac{1}{V_{DR}-V_{TH(IL)}}+\frac{1}{V_{TH(IL)}}\right](f)$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}(I_{MAX}{}^2)(1+\delta)R_{DS(ON)}$$

APPLICATIONS INFORMATION

where δ is the temperature dependency of $R_{DS(ON)}$, R_{DR} is the effective top driver resistance (approximately 2Ω at $V_{GS} = V_{MILLER}$), and V_{IN} is the drain potential and the change in drain potential in the particular application. $V_{TH(IL)}$ is the typical gate threshold voltage shown in the power MOSFET data sheet at the specified drain current. C_{MILLER} is the calculated capacitance using the gate charge curve from the MOSFET data sheet and the technique described above.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which peak at the highest input voltage. For $V_{IN} < 12V$, the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 12V$ the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

The term (1 + δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but δ = 0.005/°C can be used as an approximation for low voltage MOSFETs.

The Schottky diodes in Figure 1 conduct during the dead time between the conduction of the two large power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on, storing charge during the dead time and requiring a reverse recovery period which could cost as much as several percent in efficiency. A 2A to 8A Schottky is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition loss due to their larger junction capacitance.

C_{IN} and C_{OUT} Selection

The selection of C_{IN} is simplified by the 3-phase architecture and its impact on the worst-case RMS current drawn through the input network (battery/fuse/capacitor). It can be shown that the worst-case capacitor RMS current occurs when only one controller is operating. The controller with the highest $(V_{OUT})(I_{OUT})$ product needs to be used to determine the maximum RMS capacitor current requirement. Increasing the output current drawn from the other controller will actually decrease the input RMS ripple current from its maximum value. The out-of-phase technique typically reduces the input capacitor's RMS ripple current by a factor of 30% to 70% when compared to a single phase power supply solution.

The type of input capacitor, value and ESR rating have efficiency effects that need to be considered in the selection process. The capacitance value chosen should be sufficient to store adequate charge to keep high peak battery currents down. The ESR of the capacitor is important for capacitor power dissipation as well as overall battery efficiency. All the power (RMS ripple current • ESR) not only heats up the capacitor but wastes power from the battery.

Medium voltage (20V to 35V) ceramic, tantalum, OS-CON and switcher-rated electrolytic capacitors can be used as input capacitors, but each has drawbacks: ceramics have high voltage coefficients of capacitance and may have audible piezoelectric effects; tantalums need to be surge rated; OS-CONs suffer from higher inductance, larger case size and limited surface mount applicability; and electrolytics' higher ESR and dry out possibility require several to be used. Sanyo OS-CON SVP, SVPD series; Sanyo POSCAP TQC series or aluminum electrolytic capacitors from Panasonic WA series or Cornell Dubilier SPV series, in parallel with a couple of high performance ceramic capacitors, can be used as an effective means of achieving low ESR and large bulk capacitance. Multiphase systems allow the lowest amount of capacitance overall. As little as one 22µF or two to three 10µF ceramic capacitors are an ideal choice in 20W to 35W power supplies due to their extremely low ESR. Even though the capacitance at 20V is substantially below their rating at zero-bias, very low ESR loss makes ceramics an ideal candidate for highest efficiency battery operated systems.

In continuous mode, the source current of the top N-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current of one channel must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} \approx I_{OUT(MAX)} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

APPLICATIONS INFORMATION

This formula has a maximum value at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question.

The benefit of the LTC3773 multiphase clocking can be calculated by using the equation above for the highest power controller and then calculating the loss that would have resulted if all three channels switched on at the same time. The total RMS power lost is lower when triple controllers are operating due to the interleaving of current pulses through the input capacitor's ESR. This is why the input capacitance requirement calculated above for the worst-case controller is adequate for the triple controller design. Remember that input protection fuse resistance, battery resistance and PC board trace resistance losses are also reduced due to the reduced peak currents in a multiphase system. The overall benefit of a multiphase design will only be fully realized when the source impedance of the power supply/battery is included in the efficiency testing. The drains of the three top MOSFETs should be placed within 1cm of each other and share a common C_{IN}(s). Separating the drains and C_{IN} may produce undesirable voltage and current resonances at V_{IN}.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically once the ESR requirement is satisfied the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is determined by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{8 \bullet f \bullet C_{OUT}} \right)$$

Where f = operating frequency, C_{OUT} = output capacitance, and ΔI_L = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. With $\Delta I_L = 0.3 I_{OUT(MAX)}$ the output ripple will typically be less than 50mV at maximum V_{IN} assuming:

$$C_{OUT}\ Recommended\ ESR < 2R_{SENSE}$$

$$and\ C_{OUT} > \frac{1}{(8 \bullet f \bullet R_{SENSE})}$$

The first condition relates to the ripple current into the ESR of the output capacitance while the second term guarantees that the output capacitance does not significantly discharge during the operating frequency period due to ripple current. The choice of using smaller output capacitance increases the ripple voltage due to the discharging term but can be compensated for by using capacitors of very low ESR to maintain the ripple voltage at or below 50mV. The I_{TH} pin OPTI-LOOP compensation components can be optimized to provide stable, high performance transient response regardless of the output capacitors selected.

Manufacturers such as Sanyo, Panasonic and Cornell Dubilier should be considered for high performance through-hole capacitors. The OS-CON semiconductor electrolyte capacitor available from Sanyo has a good (ESR)(size) product. An additional ceramic capacitor in parallel with OS-CON capacitors is recommended to offset the effect of lead inductance.

In surface mount applications, multiple capacitors may have to be paralleled to meet the relevant ESR or transient current handling requirements. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. New special polymer surface mount capacitors offer very low ESR also but have much lower capacitive density per unit volume. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. Several excellent output capacitor choices are the Sanyo POSCAP TPD, TPE, TPF, AVX TPS, TPSV, the Kemet T510 series of surface mount tantalums, Kemet AO-CAPs or the Panasonic SP series of surface mount special polymer capacitors available in case heights ranging from 2mm to 4mm. Other capacitor types include Nichicon PL series and Sprague 595D series. Consult the manufacturers for other specific recommendations.

R_{SENSE} Selection for Output Current

Once the frequency and inductor have been chosen, R_{SENSE} is determined based on the required peak inductor current. The current comparator has a typical maximum threshold of $75mV/R_{SENSE}$ and an input common mode range of SGND to (1.1) • V_{CC}. The current comparator threshold sets the peak inductor current, yielding a maximum aver-

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age output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current, ΔI_L.

Allowing a margin for variations in the IC and external component values yields:

$$R_{SENSE} = \frac{55mV}{I_{MAX}}$$

The IC works well with values of R_{SENSE} from 0.002Ω to 0.1Ω.

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant frequency architectures by preventing subharmonic oscillations at duty cycles greater than 50%. It is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 40%. Normally, at the maximum duty cycle, with slope compensation, the maximum inductor peak current is reduced by more than 50%, reducing the maximum output current at high duty cycle operation. However, the LTC3773's slope compensation recovery is implemented to allow 70% rated inductor peak current at the maximum duty cycle.

V_{CC} and V_{DR} Power Supplies

Power for the top and bottom MOSFET drivers is derived from the V_{DR} pin; the internal controller circuitry is derived from the V_{CC} pin. Under typical operating conditions, the total current consumption at these two pins should be well below 100mA. Hence, V_{DR} and V_{CC} can be connected to an external auxiliary 5V power supply. If an auxiliary supply is not available, a simple zener diode and a darlington NPN buffer can be used to power these two pins as shown in Figure 3. To prevent switching noise from coupling to the sensitive analog control circuitry, V_{CC} should have a 1µF bypass capacitor, at least, close to the device. The BiCMOS process that allows the LTC3773 to include large on-chip MOSFET drivers also limits the maximum V_{DR} and V_{CC} voltage to 7V. This limits the practical maximum auxiliary supply to a loosely regulated 7V rail. If V_{CC} drops below 3.9V, LTC3773 goes into undervoltage lockout; if V_{DR} drops below V_{CC} by more than 1V, the driver outputs are disabled.

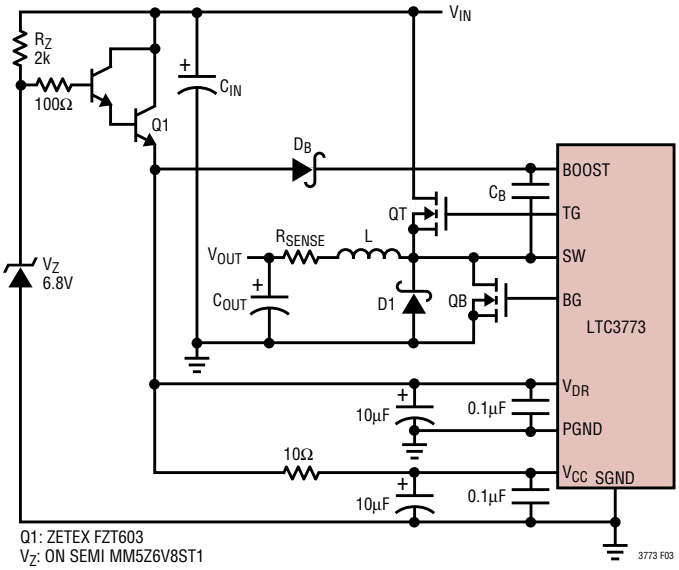

Figure 3. LTC3773 V_{CC} and V_{DR} Power Supplies

Topside MOSFET Driver Supply (C_B, D_B)

External bootstrap capacitors, C_B, connected to the BOOST pins, supply the gate drive voltages for the topside MOSFETs. Capacitor C_B in Figure 3 is charged though diode D_B from V_{DR} when the SW pin is low. When the topside MOSFETs turns on, the driver places the C_B voltage across the gate-source of the desired MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply ($V_{BOOST} = V_{DR} + V_{IN}$). The value of the boost capacitor C_B needs to be 30 to 100 times that of the total gate charge capacitance of the topside MOSFET(s) as specified on the manufacturer's data sheet. The reverse breakdown of D_B must be greater than $V_{IN(MAX)}$.

Regulator Output Voltage

The regulator output voltages are each set by an external feedback resistive divider carefully placed across the output capacitor. The resultant feedback signal is compared with the internal precision 0.6V voltage reference by the error amplifier. The output voltage is given by the equation:

$$V_{OUT} = 0.6V\left(1+\frac{R2}{R1}\right)$$

where R1 and R2 are defined in Figure 1.

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SENSE+/SENSE– Pins

The common mode input range of the current comparator sense pins is from 0V to (1.1)V_{CC}. Continuous linear operation is guaranteed throughout this range allowing output voltage setting from 0.6V to 7.7V, depending upon the voltage applied to V_{CC}. A differential NPN input stage is biased with internal resistors from an internal 2.4V source as shown in Figure 1. This requires that current either be sourced or sunk from the SENSE pins depending on the regulator output voltage. If the output voltage is below 2.4V, current will flow out of both SENSE pins to the main output. The output can be easily preloaded by the V_{OUT} resistive divider to compensate for the current comparator's negative input bias current. The maximum current flowing out of each pair of SENSE pins is:

$$I_{SENSE}^{+} + I_{SENSE}^{-} = 2 \bullet \frac{2.4V - V_{OUT}}{60k}$$

Since V_{FB} is servoed to the 0.6V reference voltage, we can choose R1 in Figure 1 to have a maximum value to absorb this current.

$$R1_{(MAX)} = 30k\left(\frac{0.6V}{2.4V - V_{OUT}}\right) \text{ for } V_{OUT} < 2.4V$$

Regulating an output voltage of 1.8V, the maximum value of R1 should be 30k. Note that for an output voltage above 2.4V, R1 has no maximum value necessary to absorb the sense currents; however, R1 is still bounded by the V_{FB} feedback current.

Power Up from Shutdown

If the SDB1, SDB2 and SDB3 pins are forced below 0.4V, the IC enters low current shutdown mode. Under this condition, most of the internal circuit blocks, including the reference, are disabled. The supply current drops to a typical value of 20µA. Disconnecting the external applied voltage source allows an internal 0.5µA current source to pull up the SDBn pin. Once the voltage at any of the SDB pins is above the shutdown threshold, the reference and the internal biasing circuit wake up. When the voltage at the SDBn pin goes above its power-up threshold, its driver starts to toggle. The power-up thresholds for channels 1, 2 and 3 are set at 1.2V, 1.8V and 2.4V respectively. Adding a small external capacitor larger than 100pF at the SDB pin reduces the slew rate at the node, permitting the internal circuit to settle before actual conversion begins.

LTC3773 can be easily configured to produce a sequential power up/down supply. By adding an external capacitor at the SDB pin; or by controlling the SDB input voltage, channel 1 will be powered up first, followed by channel 2 and sequentially channel 3. The channel turn on time delay is determined by the SDB capacitor value. Figure 4 shows the sequential power up/down configuration and its waveform. The capacitor at the TRACK pins control the individual channel power up slew rate.

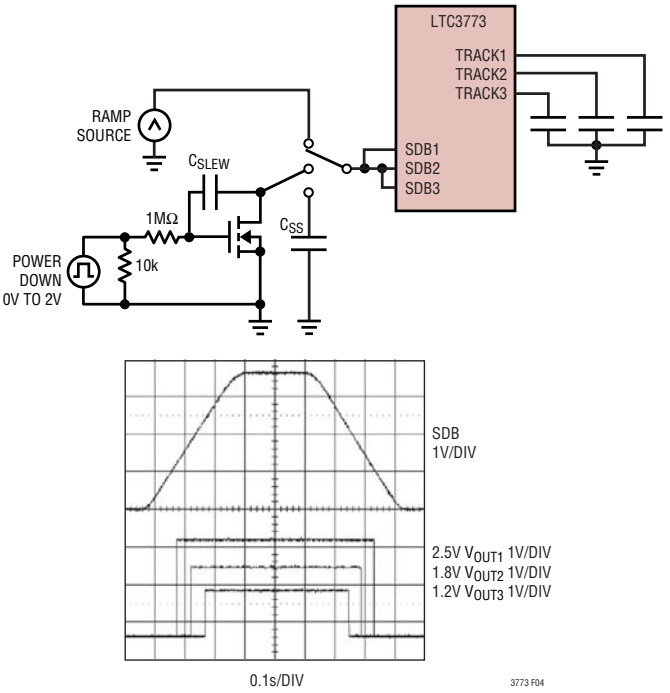

Figure 4. Sequential Power Up/Down

Soft-Start/Tracking

When the voltage on the TRACK pin is less than the internal 0.6V reference, the LTC3773 regulates the V_{FB} voltage to the TRACK pin voltage instead of 0.6V. After the soft-start/tracking cycle, the TRACK pin voltage must be higher than 0.8V; otherwise, the tracking circuit introduces offset in the error amplifier and the switcher output will be regulated to a slightly lower potential. If tracking is not required, a soft-start capacitor should be connected to the TRACK pin to regulate the output startup slew rate.

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An internal 1µA current source pull-up at the TRACK pin programs the output to take about 600ms/µF to reach its steady state value. The output voltage ramp down slew rate can be controlled by the external capacitor C_{SLEW} and the TRACK DOWN switch as shown in Figure 5a and 5b.

With a simple configuration, TRACK allows V_{OUT} start-up to track the master channel as shown qualitatively in Figures 5a and 5b. The LTC3773 can be configured for two different up/down tracking modes:coincident or ratiometric.

To implement the ratiometric tracking shown in Figure 5a, no extra divider is needed; simply connect the TRACK2 and TRACK3 pins to the TRACK1 pin. Do not connect TRACK to the V_{FB} pin. With a ratiometric configuration, the LTC3773 produces three different output slew rates. Because each channel's slew rate is proportional to its corresponding output voltage, the three output voltages reach their steady-state values at about the same time. If any of the channel SDB pins are asserted, its TRACK pin will be internally pulled low and all channels will be disabled.

To implement coincident tracking, connect extra resistor dividers to the output of channel 1. These resistor dividers are selected to be the same as the V_{FB} dividers across the outputs of channels 2 and 3. TRACK2 and TRACK3 are connected to these extra resistor dividers as shown in Figure 5b. In this tracking scheme, V_{OUT1} must be set higher than V_{OUT2} and V_{OUT3}. The coincident configuration produces the same slew rate at the three outputs, so that the lowest output voltage channel reaches its steady state first.

The TRACK pin 1µA internal pull-up current performs the soft-start action, but in tracking mode it introduces an error term in the resistive divider. To minimize this error, build the resistive divider with smaller value resistors, or

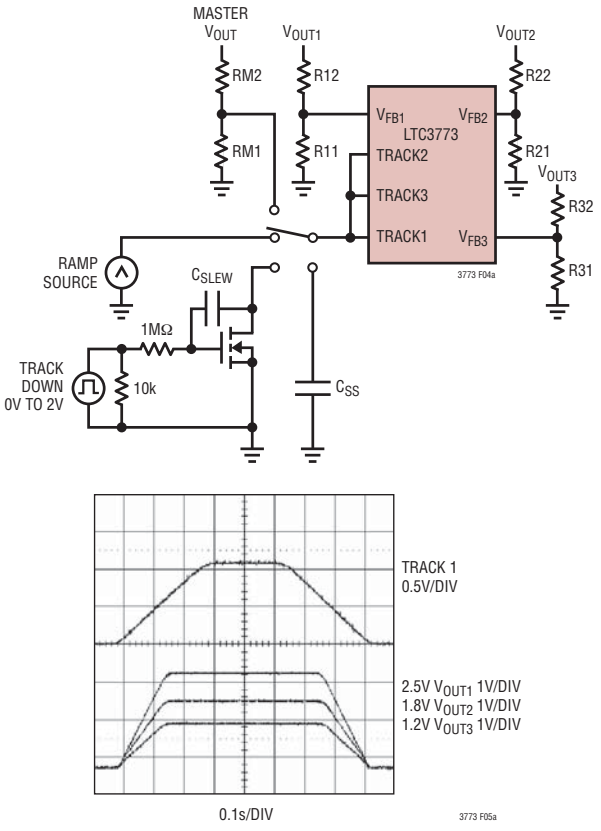

Figure 5a. Ratiometric Tracking. TRACK1 Functions as a Soft-Start Pin; V_{OUT2} and V_{OUT3} Track V_{OUT1} with Ratiometric Start-Up Slew Rate

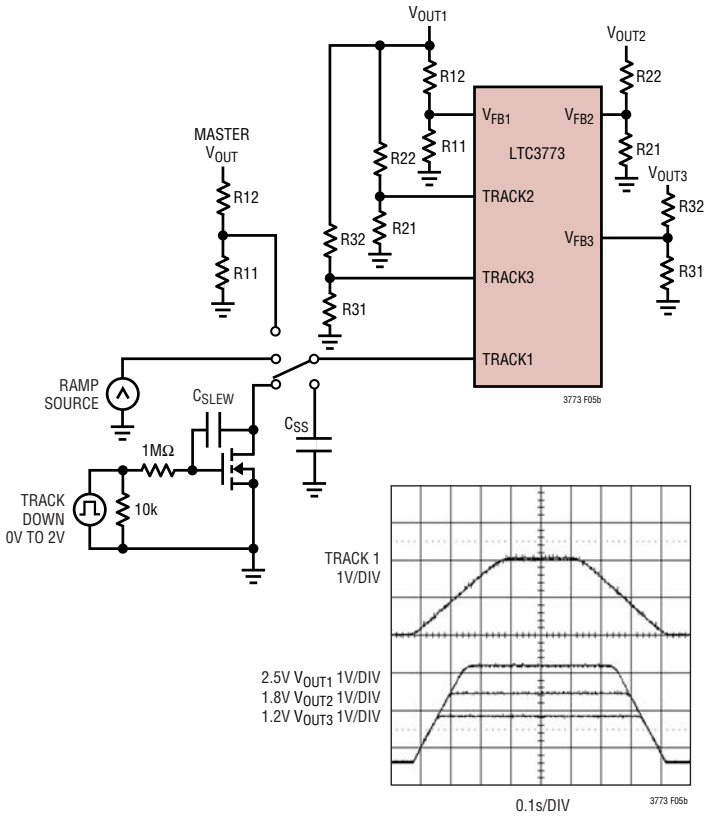

Figure 5b. Coincident Tracking. TRACK1 Functions as a Soft-Start Pin; V_{OUT2} and V_{OUT3} Track V_{OUT1} with the Same Start-Up Slew Rate

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add an extra tracking resistive divider. When the tracking resistive divider input is grounded, the pull-up current flowing through the network could produce a small unwanted offset at the TRACK pin, forcing the controller to create an unwanted low voltage supply at the regulator output. To compensate for this error, the LTC3773 introduces a 30mV offset in the tracking circuit, which disables the driver until the potential at the TRACK pin is above 30mV. The magnitude of this offset diminishes as the potential at the TRACK pin approaches 100mV, allowing accurate tracking after startup.

Fault Conditions: Current Limit and Current Foldback

The LTC3773 current comparator has a maximum sense voltage of 75mV resulting in a maximum MOSFET current of $75mV/R_{SENSE}$. The maximum value of current limit generally occurs with the largest V_{IN} at the highest ambient temperature, conditions that cause the highest power dissipation in the top MOSFET.

The LTC3773 includes current foldback to help further limit load current when the output is shorted to ground. If the potential at the TRACK pin is above 0.54V and the V_{FB} voltage falls below 70% of its nominal level, then the maximum sense voltage is progressively lowered from 75mV to 15mV. Under short-circuit conditions with very low duty cycles, the LTC3773 will begin cycle skipping in order to limit the short-circuit current. In this situation the bottom MOSFET will be dissipating most of the power but less than in normal operation. The short-circuit ripple current is determined by the minimum on-time, $t_{ON(MIN)}$, of the LTC3773 (less than 200ns), the input voltage and inductor value:

$$\Delta I_{L(SC)} = t_{ON(MIN)} \left(\frac{V_{IN}}{L} \right)$$

The resulting short-circuit current is:

$$I_{SC} = \frac{15mV}{R_{SENSE}} - \frac{1}{2} \Delta I_{L(SC)}$$

Disable Current Foldback at Start-Up

At start-up, if the potential at the TRACK pin is lower than 0.54V, the LTC3773 current comparator threshold voltage stays at 75mV and the regulator current limit remains at its rated value. This feature allows the LTC3773 to power the core and I/O of low voltage FPGAs.

When power is first applied to an FPGA, the device can draw current several times its normal operating current. This power-on surge current is due to the programmable nature of FPGAs. When the FPGA powers up, before initialization, the RAM cells are briefly in a random state. This results in contention at the interconnect and significant power dissipation. The duration of the power-on surge current is typically quite brief but can cause problems for power supply designs. LTC3773 views currents that are outside the normal operation range as possible short-circuits. Disabling the current foldback at startup allows the regulator to provides a higher surge current to meet the FPGA's requirement. Nevertheless, when calculating the current sense resistor value for FPGA power supply applications, the computed output current value must be higher than the power-on surge current to allow a proper startup.

Fault Conditions: Overvoltage Protection

A comparator monitors the output for overvoltage conditions. The comparator (OV) detects overvoltage faults greater than 3.75% above the nominal output voltage. When this condition is sensed, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared. The bottom MOSFET remains on continuously for as long as the OV condition persists. If V_{OUT} returns to a safe level, normal operation automatically resumes.

Note that under extreme power-up conditions, e.g. with high input voltage, a small inductor and a small soft-start capacitor, once the OV comparator trips, the output voltage might continue to charge above the rated value until the energy in the inductor is depleted. The peak of the overshoot might be higher than the rated voltage of the output capacitors.

Phase-Locked Loop and Frequency Synchronization

The LTC3773 has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (VCO) and a phase detector. This allows the turn-on of the external N channel

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MOSFET of controller 1 to be locked to the rising edge of an external clock signal applied to the PLLIN/FC pin. The turn-on of controller 2's/3's external N-channel MOSFET and CLKOUT signal are controlled by the PHASEMD pin as showed in Table 1. Note that when PHASEMD is forced high, controller 2 and controller 3 outputs can be connected in parallel to produce a higher output power voltage source.

Table 1. Phase Relationship between the PLLIN/FC Pin vs Controller 1, 2, 3 Top Gate and CLKOUT Pin

PHASEMD	CH1	CH2	CH3	CLKOUT
GND	0 Deg	120 Deg	240 Deg	60 Deg
Floating	0 Deg	120 Deg	240 Deg	0 Deg
V_{CC}	0 Deg	90 Deg	270 Deg	180 Deg

The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock. A simplified Phase-Locked Loop Block Diagram is shown in Figure 6a. The output of the phase detector is a pair of complementary current sources that charge or discharge the external filter network connected to the PLLFLTR pin. The relationship between the voltage on the PLLFLTR pin and operating frequency, when there is a clock signal applied to PLLIN/FC, is shown in Figure 6b and specified in the Electrical Characteristics table. Note that the LTC3773 can only be synchronized to an external clock whose frequency is within range of the LTC3773's internal VCO, which is nominally 160kHz to 700Hz. This is guaranteed, over temperature and variations, to be between 200kHz and 540kHz.

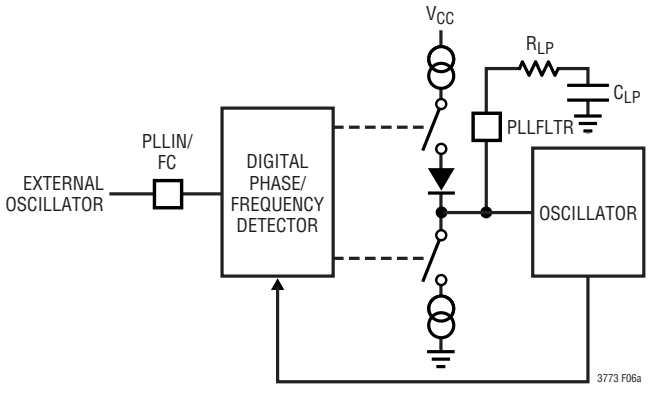

Figure 6a. Phase-Locked Loop Block Diagram

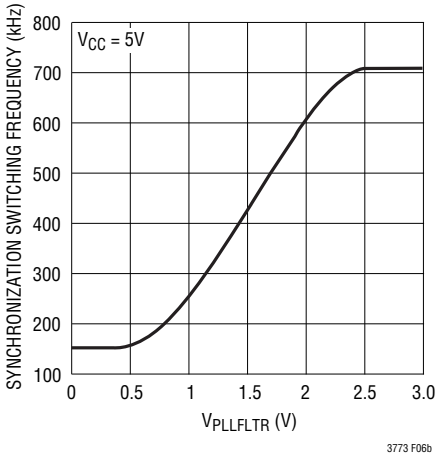

Figure 6b. Relationship Between Oscillator Frequency and Voltage at the PLLFLTR Pin When Synchronizing to an External Clock

If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sourced continuously from the phase detector output, pulling up the PLLFLTR pin. When the external clock frequency is less than f_{OSC}, current is sunk continuously, pulling down the PLLFLTR pin. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage on the PLLFLTR pin is adjusted until the phase and frequency of the oscillators are identical. At the stable operating point, the phase detector has high impedance and the filter capacitor C_{LP} holds the voltage.

The loop filter components, C_{LP} and R_{LP}, smooth out the current pulses from the phase detector and provide a stable input to the voltage-controlled oscillator. The filter components C_{LP} and R_{LP} determine how fast the loop acquires lock. Typically R_{LP} = 10k and C_{LP} is 0.01µF to 0.1µF. The external clock (on the PLLIN/FC pin) input threshold is typically 1V. Table 2 summarizes the different states in which the PLLIN/FC and PLLFLTR pins can be used.

Table 2. PLLFLTR Pin Voltage vs Switching Frequency

PLLFLTR	PLLIN/FC	FREQUENCY
GND	DC Voltage	220kHz
Floating	DC Voltage	400kHz
V_{CC}	DC Voltage	560kHz
RC Loop Filter	Clock Signal	Phase-Locked to External Clock

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The LTC3773 can be configured to operate at any switching frequency within the synchronization range. Figure 7 shows a simple circuit to achieve this. The resistive divider at the PLLFLTR pin programs the LTC3773 switching frequency according to the transfer curve of Figure 6b. By connecting the PLLIN/FC pin to the BG1 or the CLKOUT (UHF package only) node, the pre-set frequency selection is disengaged and the PLLFLTR pin potential determines the switching frequency.

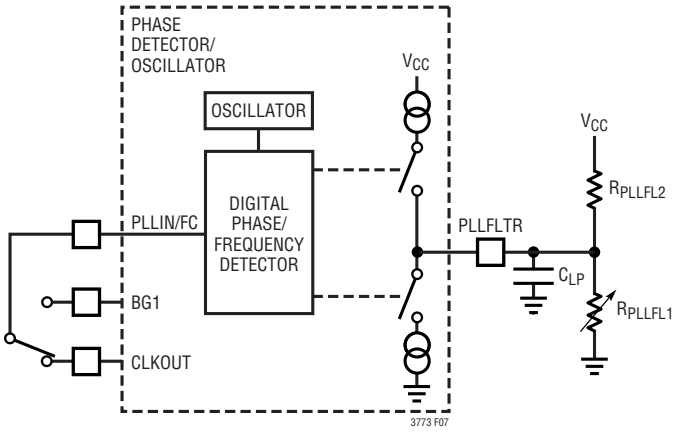

Figure 7. Fixed Frequency Adjustment

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the IC is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge of the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN}(f)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the IC will begin to skip every other cycle, resulting in half-frequency operation. The output voltage will continue to be regulated, but the ripple current and ripple voltage will increase.

The minimum on-time for the IC is generally about 130ns. However, as the peak sense voltage decreases, the minimum on-time gradually increases. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

If an application can operate close to the minimum on-time limit, an inductor must be chosen that is low enough in value to provide sufficient ripple amplitude to meet the minimum on-time requirement. As a general rule, keep the inductor ripple current for each channel equal to or greater than 30% of $I_{OUT(MAX)}$ at $V_{IN(MAX)}$.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%Efficiency = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD} \bullet ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. The availability of the I_{TH} pin not only allows optimization of control loop behavior, but also provides a DC coupled and AC filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin.

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The I_{TH} series R_C-C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly to maximize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be decided upon because the various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 80% of full load current having a rise time of <2µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. The initial output voltage step, resulting from the step change in output current, may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the I_{TH} pin signal which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Application Note 76.

Automotive Considerations: Plugging into the Cigarette Lighter

As battery-powered devices go mobile, there is a natural interest in plugging into the cigarette lighter in order to conserve or even recharge battery packs during operation. But before you connect, be advised: you are plugging into the supply from hell. The main battery line in an automobile is the source of a number of nasty potential transients, including load dump, reverse battery and double battery.

Load dump is the result of a loose battery cable. When the cable breaks connection, the field collapse in the alternator can cause a positive spike as high as 60V which takes several hundred milliseconds to decay. Reverse battery is just what it says, while double battery is a consequence of tow-truck operators finding that a 24V jump start cranks cold engines faster than 12V.

The network shown in Figure 8 is the most straightforward approach to protect a DC/DC converter from the ravages of an automotive battery line. The series diode prevents current from flowing during reverse battery, while the transient suppressor clamps the input voltage during load dump. Note that the transient suppressor should not conduct during double-battery operation, but must still clamp the input voltage below breakdown of the converter. Although the IC has a maximum input voltage of 36V on the SW pins, most applications will be limited to 30V by the MOSFET B_{VDSS}.

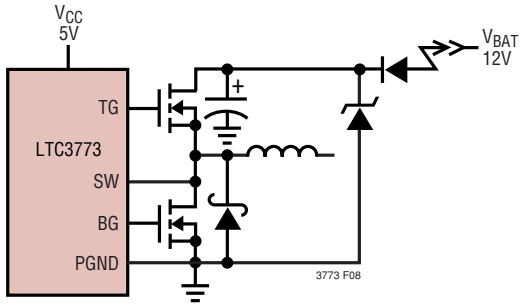

Figure 8. Automotive Application Protection

Design Example

As a design example for one channel, assume V_{IN} = 12V (nominal), V_{IN} = 22V(max), V_{OUT} = 1.8V, I_{MAX} = 15A, and f = 220kHz.

The inductance value is chosen first based on a 30% ripple current assumption. The highest value of ripple current occurs at the maximum input voltage. Short the PLLFLTR pin to ground to program for 220kHz operation. The minimum inductance for 30% ripple current is:

$$L = \frac{V_{OUT}}{(f)(\Delta I_L)}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

$$= \frac{1.8V}{(220k)(30\%)(15A)}\left(1-\frac{1.8V}{22V}\right) = 1.67\mu H$$

Using L = 1.5µH, a commonly available value results in 30% ripple current. The peak inductor current will be the maximum DC value plus one half the ripple current, or 17.3A. Increasing the ripple current will also help ensure

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that the minimum on-time of 130ns is not violated. The minimum on-time occurs at maximum V_{IN}:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)}f} = \frac{1.8V}{22V(220kHz)} = 372ns$$

The R_{SENSE} resistor value can be calculated by using the maximum current sense voltage specification with a conservative maximum sense current threshold of 55mV:

$$R_{SENSE} \leq \frac{55mV}{17.3A} \approx 3.2m\Omega$$

Use a commonly available 0.003Ω sense resistor.

Since the output voltage is below 2.4V the output resistive divider will need to be sized to not only set the output voltage but also to absorb the SENSE pin's specified input current.

$$R1_{(MAX)} = 30k\left(\frac{0.6V}{2.4V - V_{OUT}}\right)$$

$$= 30k\left(\frac{0.6V}{2.4V - 1.8V}\right) = 30k$$

Choosing 1% resistors; R1 = 10k and R2 = 20k yields an output voltage of 1.8V.

The power dissipation on the top side MOSFET can be easily estimated. Choosing a Renesas HAT2168H MOSFET results in: $R_{DS(ON)}$ = 13.5mΩ, C_{MILLER} = 6nC/25V = 240pF. At maximum input voltage with T (estimated) = 50°C:

$$P_{MAIN} = \left\{\frac{1.8V}{22V}(15)^2\left[1+(0.005)(50°C-25°C)\right]\right.$$

$$\left.(13.5m\Omega)\right\} + \left\{(22V)^2\left(\frac{15A}{2}\right)(2\Omega)(240pF)\right.$$

$$\left.\left[\frac{1}{5-1.8}+\frac{1}{1.8}\right](220kHz)\right\} = 0.612W$$

Using a Renesas HAT2165H as a bottom MOSFET, the worst-case power dissipation by the synchronous MOSFET under normal operating conditions at elevated ambient temperature and an estimated 50°C junction temperature rise is:

$$P_{SYNC} = \frac{22V - 1.8V}{22V}(15)^2(1.125)(5.3m\Omega) = 1.23W$$

A short-circuit to ground will result in a folded back current of

$$I_{SC} = \frac{15mV}{0.003\Omega} - \frac{1}{2}\left(\frac{130ns(22V)}{1.5\mu H}\right) = 4.05A$$

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. These items are also illustrated graphically in the layout diagram of Figure 10. Check the following in the PC layout:

1. Are the top N-channel MOSFETs located within 1cm of each other with a common drain connection at C_{IN}? Do not attempt to split the input decoupling for the three channels as it can cause a large resonant loop.
2. Are the signal and power grounds kept separate? Keep the SGND at one end of a printed circuit path thus preventing MOSFET currents from traveling under the IC. The SGND pin should be used to hook up all control circuitry on one side of the IC. The combined LTC3773 SGND pin and the ground return of C_{VCC} must return to the combined C_{OUT} (–) terminals. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor by placing the capacitors next to each other and away from the charge pump circuitry. The path formed by the top N-channel MOSFET, Schottky diode and the C_{IN} capacitor should have short leads and PC trace lengths. The power ground returns to the sources of the bottom N-channel MOSFETs, anodes of the Schottky diodes and (–) plates of C_{IN}, which should have as short lead lengths as possible.
3. The V_{CC} decoupling capacitor should be placed immediately adjacent to the IC between the V_{CC} pin and SGND. A 1µF ceramic capacitor of the X7R type is small enough to fit very close to the IC to minimize the ill effects of the large current pulses drawn to drive the bottom MOSFETs. An additional 4.7µF to 10µF of ceramic, tantalum or other very low ESR capacitance is recommended in order to keep the internal IC supply quiet.
4. Do the LTC3773 V_{FB} resistive dividers connect to the (+) terminals of C_{OUT}? The resistive divider must be con-

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nected between the (+) terminal of C_{OUT} and SGND and a small decoupling capacitor should be placed across this divider; as close as possible to the LTC3773 SGND pin and away from any high current or high frequency switching nodes.

5. Are the SENSE$^-$ and SENSE$^+$ printed circuit traces for each channel routed together with minimum PC trace spacing? The filter capacitors between SENSE$^+$ and SENSE$^-$ for each channel should be as close as possible to the pins of the IC. Connect the SENSE$^-$ and SENSE$^+$ pins to the pads of the sense resistor as illustrated in Figure 9.
6. Keep the switching nodes, SW, BOOST and TG away from sensitive small-signal nodes (SENSE$^+$, SENSE$^-$, V_{FB}, I_{TH}). Ideally the SW, BOOST and TG printed circuit traces should be routed away and separated from the IC and the "quiet" side of the IC. Separate the high dV/dt printed circuit traces from sensitive small-signal nodes with ground traces or ground planes.
7. Use a low impedance source such as a logic gate to drive the PLLIN pin and keep the lead as short as possible.
8. Minimize trace impedances of TG, BG and SW nets. TG and SW must be routed in parallel with minimum distance.

Figure 10 illustrates all branch currents in a three-phase switching regulator. It becomes very clear after studying the current waveforms why it is critical to keep the high switching current paths to a small physical size. High electric and magnetic fields will radiate from these "loops" just as radio stations transmit signals. The output capacitor ground should return to the negative terminal of the input capacitor and not share a common ground path with any switched current paths. The left half of the circuit gives rise to the "noise" generated by a switching regulator. The ground terminations of the synchronous MOSFETs and Schottky diodes should return to the bottom plate(s) of the input capacitor(s) with a short isolated PC trace since very high switched currents are present. A separate isolated path from the bottom plate(s) of the input and output capacitor(s) should be used to tie in the IC power ground pin (PGND). This technique keeps inherent signals generated by high current pulses taking alternate current paths that have finite impedances during the total period of the switching regulator. External OPTI-LOOP compensation allows overcompensation for PC layouts which are not optimized but this is not the recommended design procedure.

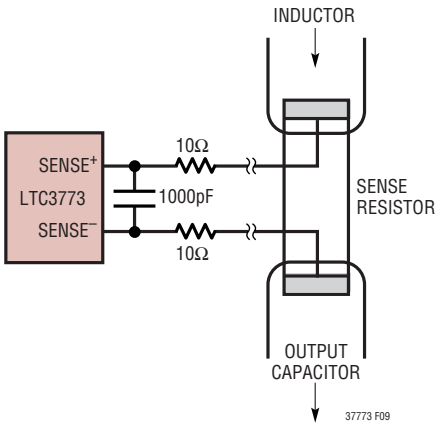

Figure 9. Kelvin Sensing R_{SENSE}

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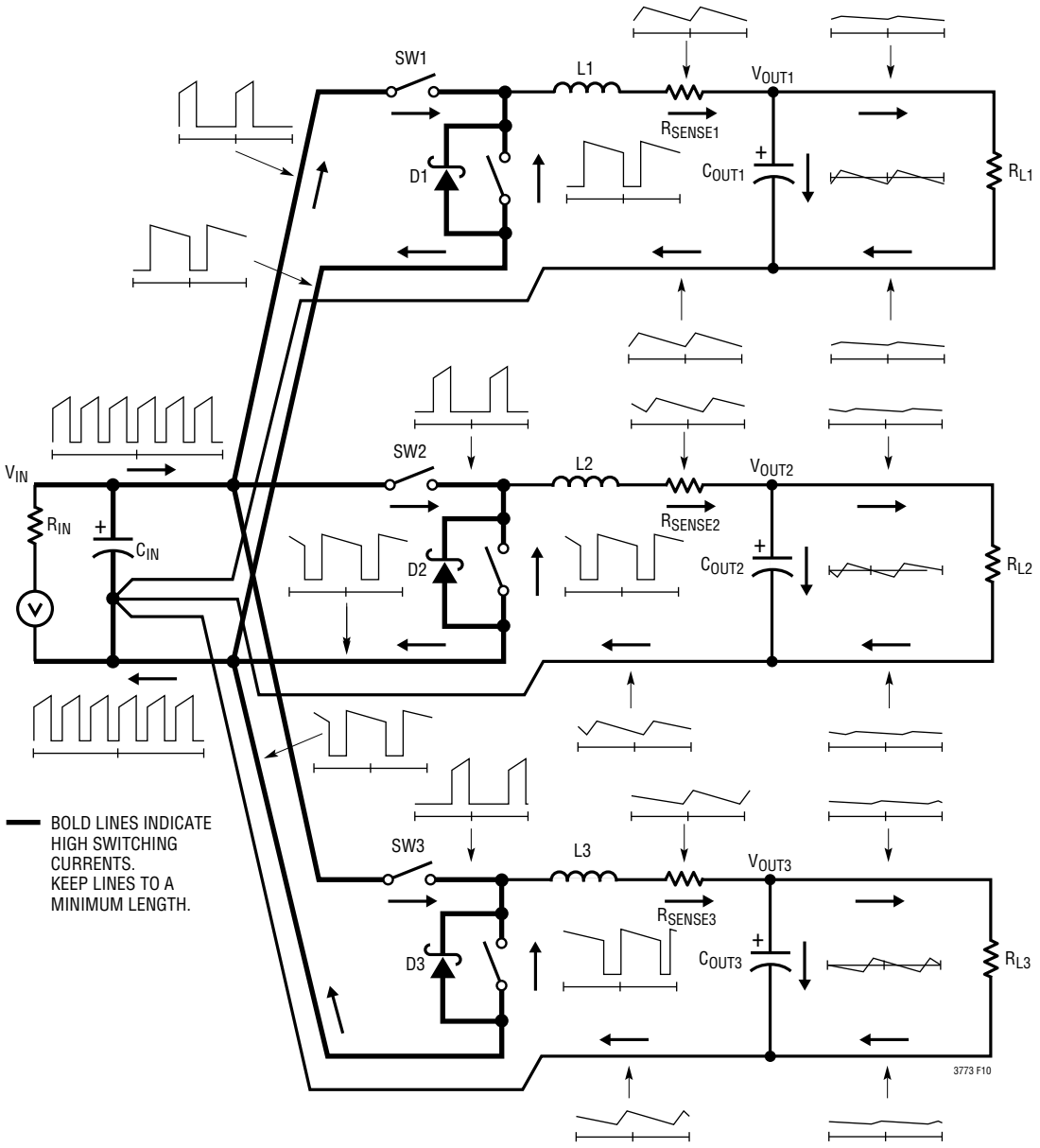

Figure 10. Branch Current Waveforms

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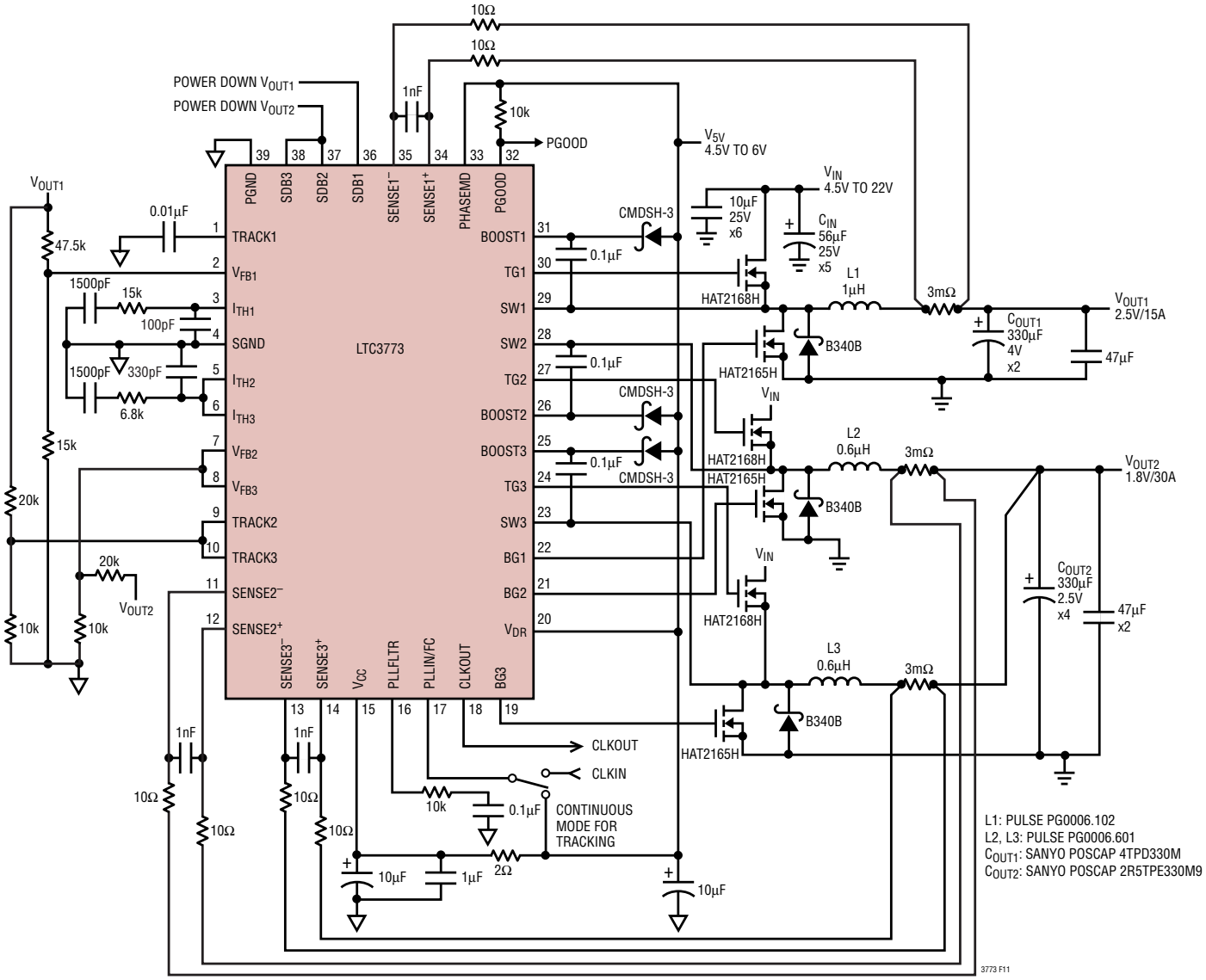
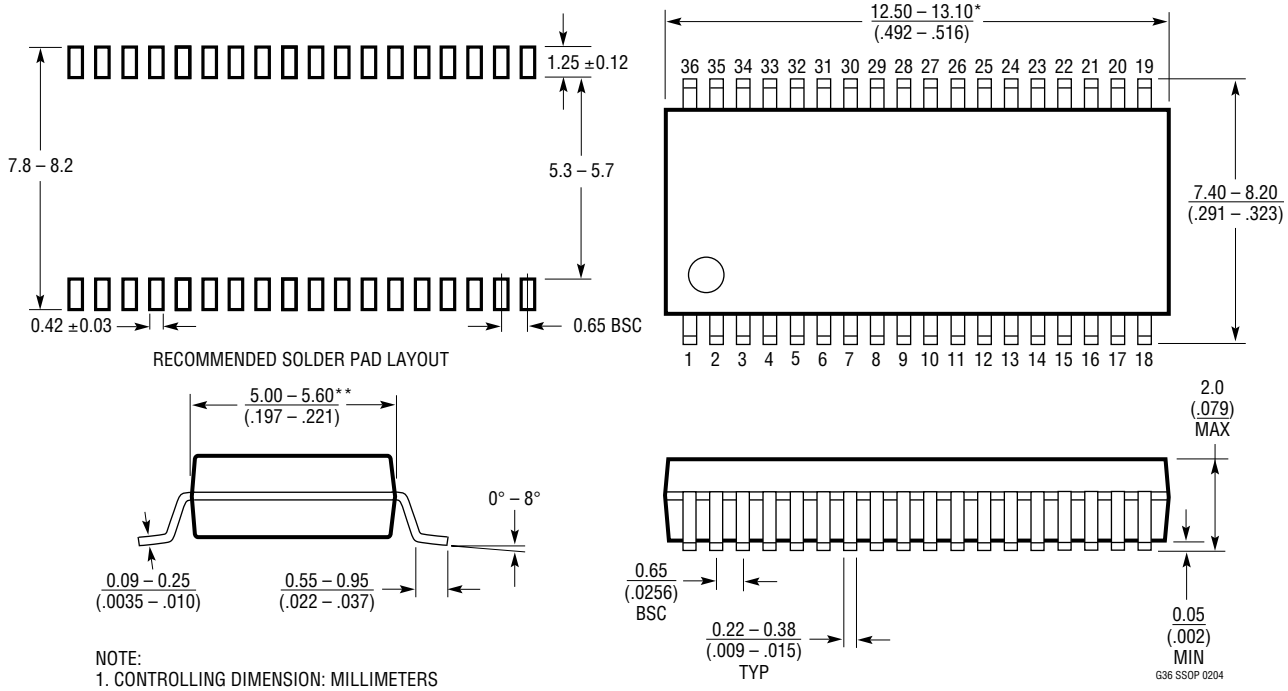


Figure 11. 3-Phase, Dual Output with Coincident Output Tracking Function

PACKAGE DESCRIPTION

G Package
36-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



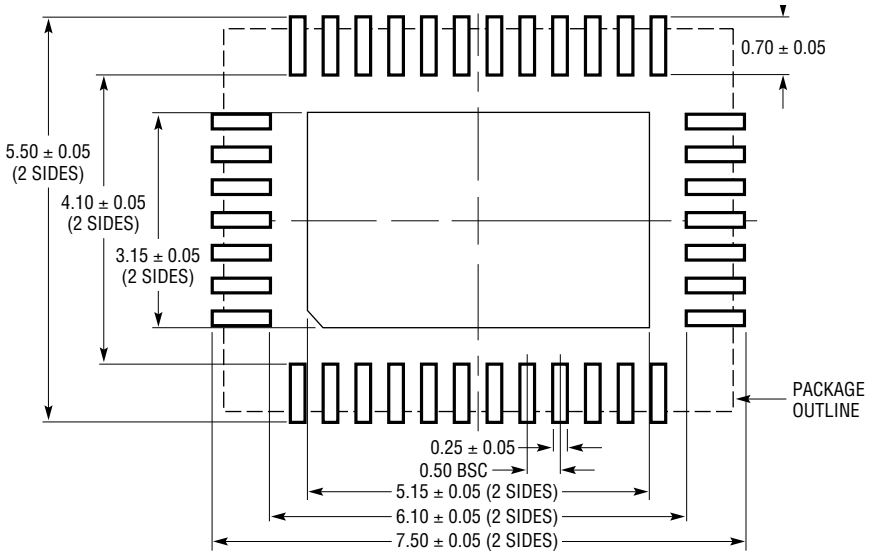
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE

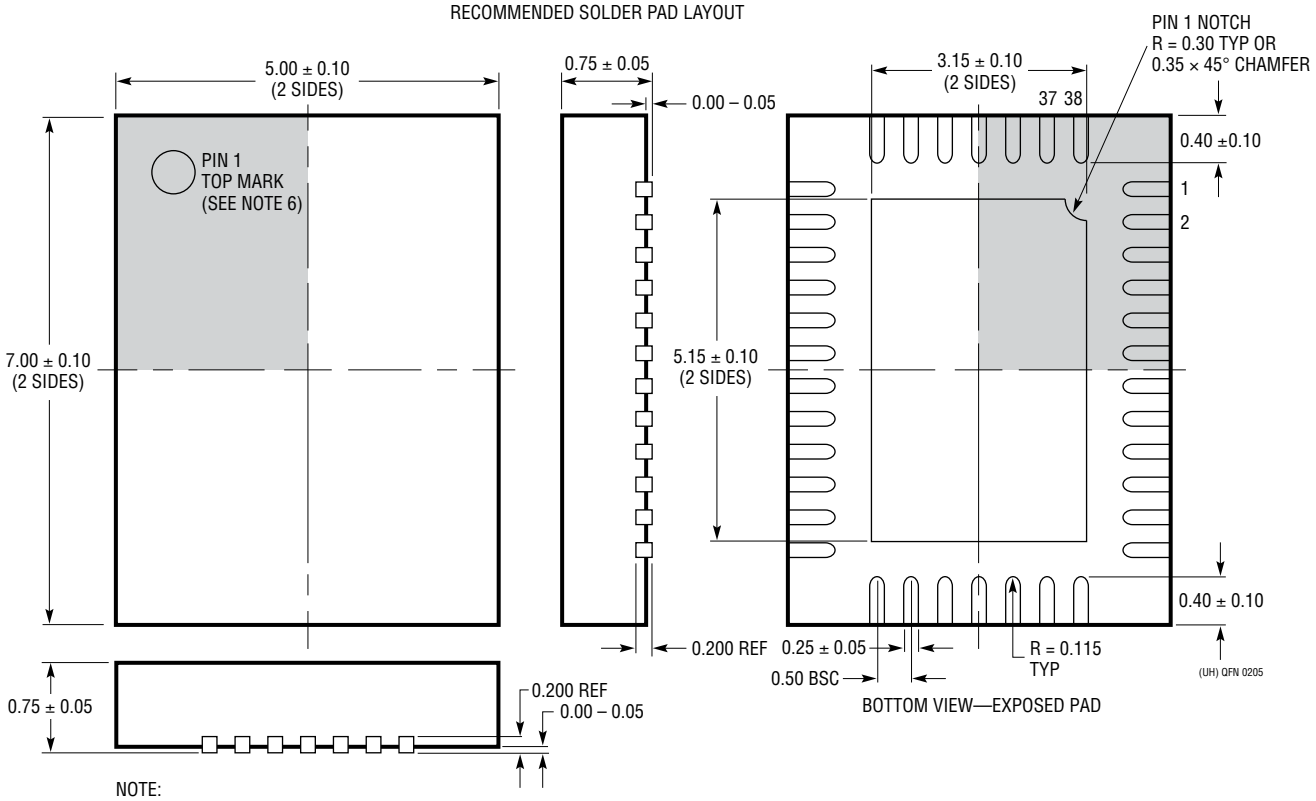
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

PACKAGE DESCRIPTION

UHF Package
38-Lead Plastic QFN (5mm × 7mm)
(Reference LTC DWG # 05-08-1701)



RECOMMENDED SOLDER PAD LAYOUT



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE M0-220 VARIATION WHKD
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

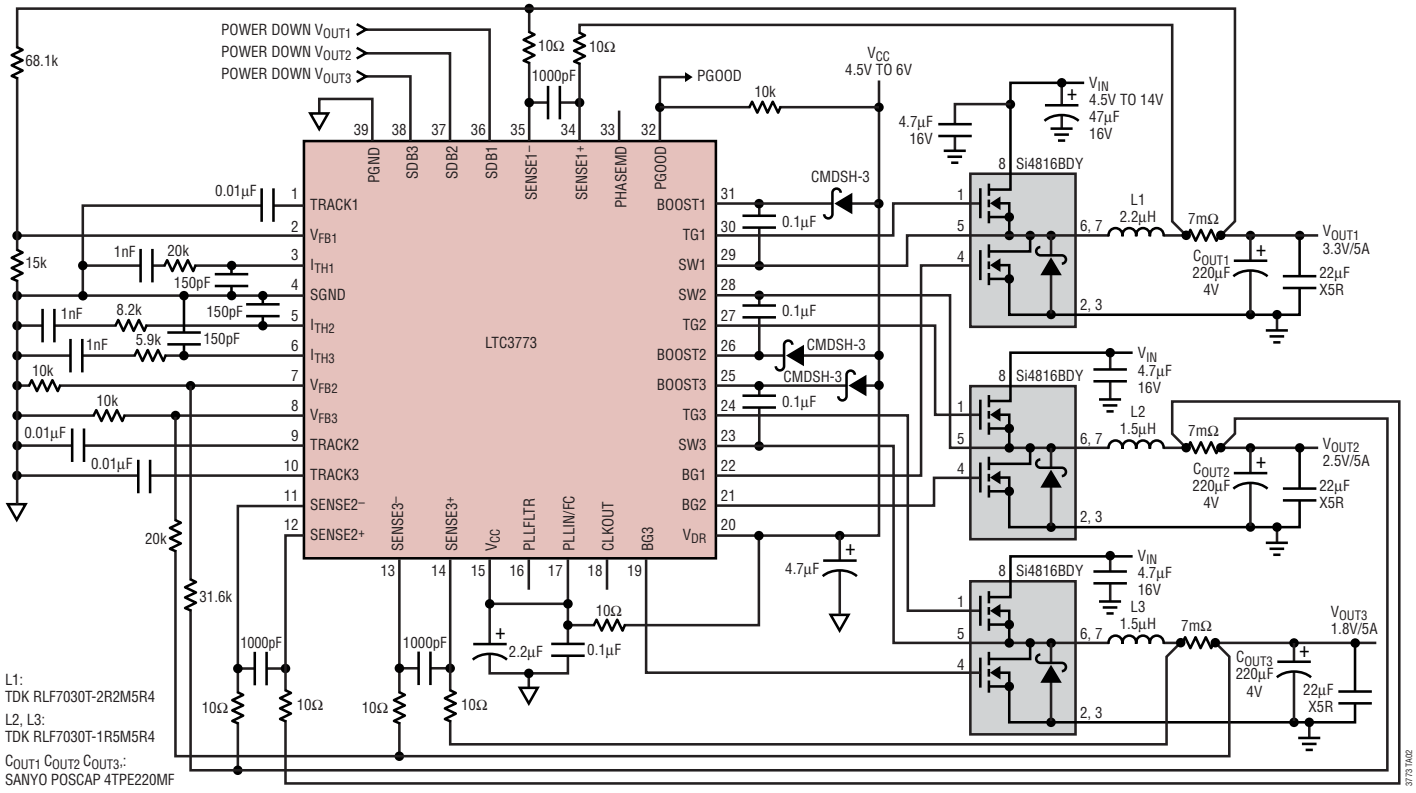


Figure 12. High Efficiency, Small Footprint Triple Output Step-Down Converter

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3407-2	Dual Synchronous, 800mA, 2.25MHz Step-Down Monolithic DC/DC Regulator	V_{IN}: 2.5V to 5.5V, V_{OUT}: 0.6V to 5V, 100% Maximum Duty Cycle
LTC3417A	Dual Synchronous Step-Down Monolithic 1.5A/1A	V_{IN}: 2.25V to 5.5V, V_{OUT}: 0.8V to 5V, 100% Maximum Duty Cycle
LTC3703	High Input Synchronous Step-Down Controller	$V_{IN} \leq 100V$
LTC3708	No R_{SENSE}™, Dual, 2-Phase Synchronous Step-Down Controller with Output Tracking	Very Low Duty Factor Operation, Programmable Output Voltage Voltage Up/Down Tracking
LTC3727	Dual Output 2-Phase Current Mode Synchronous DC/DC Step-Down Switching Regulator Controller	V_{IN}: 4V to 36V, V_{OUT}: 0.8V to 14V, 99% Maximum Duty Cycle, Selectable Burst Mode Operation
LTC3728	Dual PolyPhase® Synchronous Step-Down Switching Regulator	Dual Output, Current Mode
LTC3729	20A to 200A, 500kHz PolyPhase Synchronous Controller	Expandable from 2-Phase, Uses All Surface Mount Components, V_{IN} up to 36V
LTC3731	3- to 12-Phase Step-Down Synchronous Controller	Single Output, 60A to 240A Output Current, $0.6V \leq V_{OUT} \leq 6V$, $4.5V \leq V_{IN} \leq 32V$
LTC3778	Wide Operating Range, No R_{SENSE} Step-Down Controller	Single Channel, Separate V_{ON} Programming
LTC3802	Dual PolyPhase Voltage Mode Synchronous Step-Down Switching Regulator with Output Tracking	Very Low Duty Factor Operation, Programmable Output Voltage Up/Down Tracking, V_{IN} Up to 30V
LTC3827	Low I_Q, Dual, 2-Phase Synchronous Step-Down Controller	Low 80µA I_Q, $0.8V \leq V_{OUT} \leq 10V$, $4V \leq V_{IN} \leq 36V$

No R_{SENSE} is a trademark of Linear Technology Corporation. PolyPhase is a registered trademark of Linear Technology Corporation.

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