Rev 2; 8/04

DALLAS SEMICONDUCTOR MAXIM

CPU Supervisor with Nonvolatile Memory and Programmable I/O

DS4510

General Description

The DS4510 is a CPU supervisor with integrated 64-byte EEPROM memory and four programmable, nonvolatile (NV) I/O pins. It is configured with an industry-standard I²C™ interface using either fast-mode (400kbps) or standard-mode (100kbps) communication. The I/O pins can be used as general-purpose I²C-to-parallel I/O expander with unlimited read/write capability. EEPROM registers allow the power-on value of the I/O pins to be adjusted to keep track of the system's state through power cycles, and the CPU supervisor's timer can be adjusted between 125ms and 1000ms to meet most any application need.

Features

- **Accurate 5%, 10%, or 15% 5V Power-Supply Monitoring**
- **Programmable Reset Timer Maintains Reset After V_{CC} Returns to an In-Tolerance Condition**
- **Four Programmable, NV, Digital I/O Pins with Selectable Internal Pullup Resistor**
- **64 Bytes of User EEPROM**
- **Reduces Need for Discrete Components**
- **I²C-Compatible Serial Interface**
- **10-Pin µSOP Package**

Applications

RAM-Based FPGA Bank Switching for Multiple Profiles

Industrial Controls

Cellular Telephones

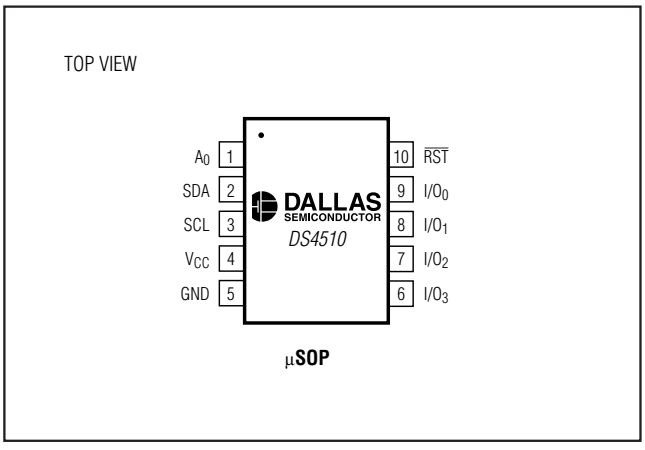
PC Peripherals

PDAs

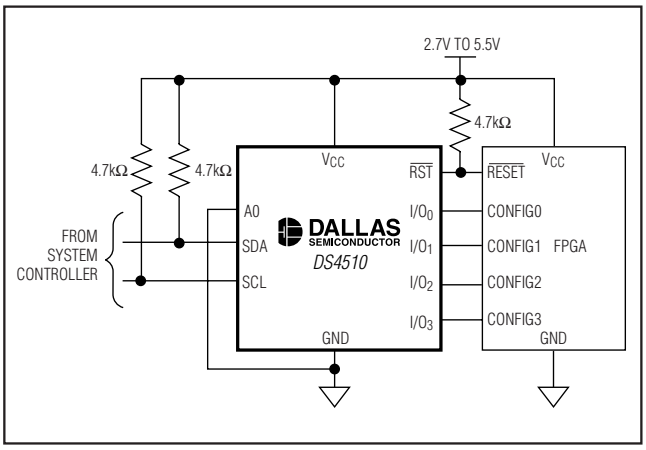
Ordering Information

PART	V_{CC} TRIP POINT	TEMP RANGE	PIN-PACKAGE
DS4510U-5	5%	-40°C to +85°C	10 µSOP
DS4510U-10	10%	-40°C to +85°C	10 µSOP
DS4510U-15	15%	-40°C to +85°C	10 µSOP
DS4510U-5/T&R	5%	-40°C to +85°C	10 µSOP
DS4510U-10/T&R	10%	-40°C to +85°C	10 µSOP
DS4510U-15/T&R	15%	-40°C to +85°C	10 µSOP

Pin Configuration



Typical Operating Circuit



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CPU Supervisor with Nonvolatile Memory and Programmable I/O

ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{CC}, SDA, and SCL Pins Relative to Ground .....-0.5V to +6.0V
Voltage Range on A_0, I/O_0, I/O_1, I/O_2, I/O_3 Relative to Ground .....-0.5V to V_{CC} + 0.5V, not to exceed +6.0V.
Operating Temperature Range .....-40°C to +85°C
EEPROM Programming Temperature .....0°C to +70°C
Storage Temperature Range .....-55°C to +125°C
Soldering Temperature .....See IPC/JEDEC J-STD-020A Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	(Notes 1)	2.7		5.5	V
Input Logic 1	V_{IH}	(Note 2)	0.7 x V_{CC}		V_{CC} + 0.3	V
Input Logic 0	V_{IL}		-0.3		+0.3 x V_{CC}	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7V to 5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Trip Point	V_{CCTP}	DS4510U-5	4.5	4.625	4.75	V
		DS4510U-10	4.25	4.375	4.49	
		DS4510U-15	4.0	4.125	4.24	
Standby Current	I_{STBY}	V_{CC} = 5.0V (Note 3)		50	75	µA
Input Leakage	I_L		-1.0		+1.0	µA
SDA Low-Level Output Voltage	V_{OL}	3mA sink current			0.4	V
		6mA sink current			0.6	
I/O_X Low-Level Output Voltage	V_{OLIOX}	4mA sink current			0.4	V
$\overline{RST}$ Pin Low-Level Output	$V_{OL\overline{RST}}$	10mA sink current (Note 4)			0.4	V
I/O_X Pullup Resistors	R_P		4.0	5.0	6.5	kΩ
I/O Capacitance	$C_{I/O}$	(Note 5)			10	pF

CPU SUPERVISOR AC ELECTRICAL CHARACTERISTICS (See Figure 1)

(V_{CC} = 2.7V to 5.5V, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{RST}$ Active Time	$t_{\overline{RST}}$	TD1= 0, TD0 = 0	112	125	138	ms
		TD1= 0, TD0 = 1	225	250	275	
		TD1= 1, TD0 = 0	450	500	550	
		TD1= 1, TD0 = 1	900	1000	1100	
V_{CC} Detect to $\overline{RST}$	t_{RPU}	TD1= 0, TD0 = 0	112	125	138	ms
		TD1= 0, TD0 = 1	225	250	275	
		TD1= 1, TD0 = 0	450	500	550	
		TD1= 1, TD0 = 1	900	1000	1100	
V_{CC} Fail to $\overline{RST}$	t_{RPD}			4	10	µs

AC ELECTRICAL CHARACTERISTICS (See Figure 5)

(V_{CC} = 2.7V to 5.5V, T_A = -40°C to +85°C, timing referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 6)	0		400	kHz
Bus Free Time Between Stop and Start Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) Start Condition	$t_{HD:STA}$		0.6			µs
Low Period of SCL	t_{LOW}		1.3			µs
High Period of SCL	t_{HIGH}		0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Start Setup time	$t_{SU:STA}$		0.6			µs
SDA and SCL Rise Time	t_R	(Note 7)	20 + 0.1C_B		300	ns
SDA and SCL Fall Time	t_F	(Note 7)	20 + 0.1C_B		300	ns
Stop Setup Time	$t_{SU:STO}$		0.6			µs
SDA and SCL Capacitive Loading	C_B	(Note 7)			400	pF
EEPROM Write Time	t_W	(Note 7)		10	20	ms

CPU Supervisor with Nonvolatile Memory and Programmable I/O

NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = 2.7V to 5.5V, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Writes		+70°C (Note 5)	50,000			

Note 1: All voltages referenced to ground.

Note 2: The DS4510 does not obstruct the SDA and SCL lines if V_{CC} is switched off, as long as the voltages applied to these inputs do not violate their min and max input voltage levels.

Note 3: I_{STBY} specified with V_{CC} equal to 5.0V, and control port-logic pins are driven to ground or V_{CC} for the corresponding inactive state (SDA = SCL = V_{CC}), does not include pullup resistor current.

Note 4: See *Typical Operating Characteristics* for the $\overline{RST}$ output voltage vs. supply voltage.

Note 5: This parameter is guaranteed by design.

Note 6: I^2C interface timing shown for is for fast-mode (400kHz) operation. This device is also backward compatible with I^2C standard-mode timing.

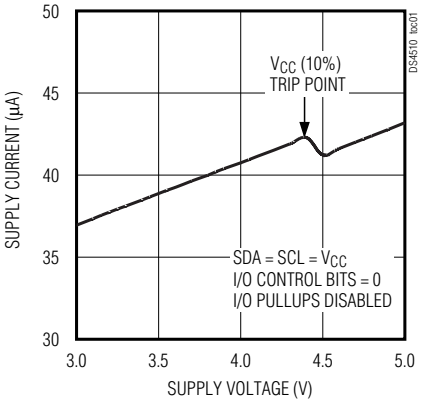
Note 7: C_B—total capacitance of one bus line in picofarads.

Note 8: EEPROM write time applies to all the EEPROM memory and SEEPROM memory when $\overline{SEE}$ = 0. The EEPROM write time begins at the occurrence of a stop condition.

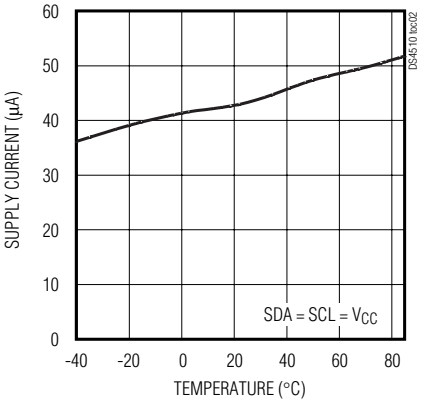
Typical Operating Characteristics

(V_{CC} = +5.0V, T_A = +25°C, unless otherwise noted.)

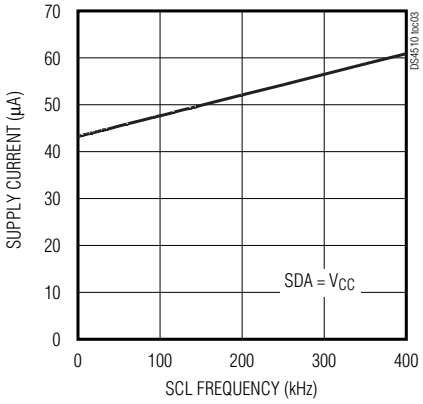
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



SUPPLY CURRENT vs. SCL FREQUENCY

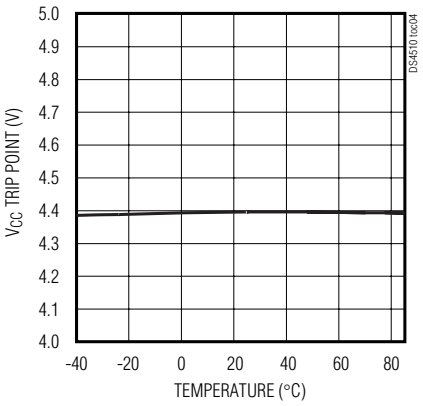


CPU Supervisor with Nonvolatile Memory and Programmable I/O

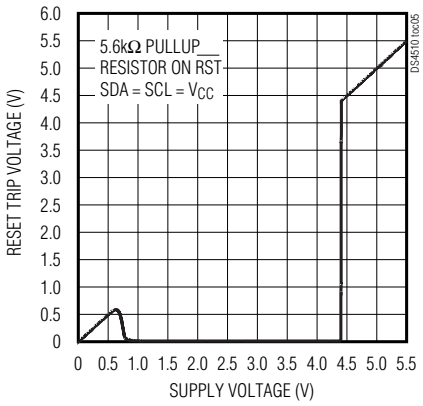
Typical Operating Characteristics (continued)

(V_{CC} = +5.0V, T_A = +25°C, unless otherwise noted.)

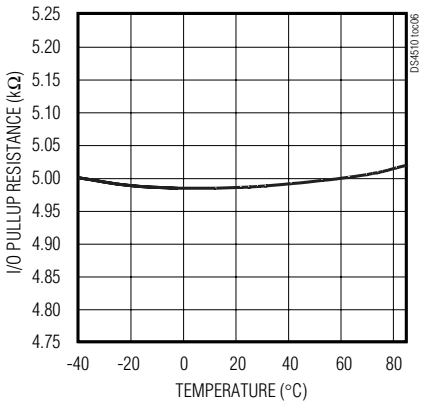
V_{CC} TRIP POINT vs. TEMPERATURE



$\overline{RST}$ OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



I/O PULLUP RESISTANCE vs. TEMPERATURE

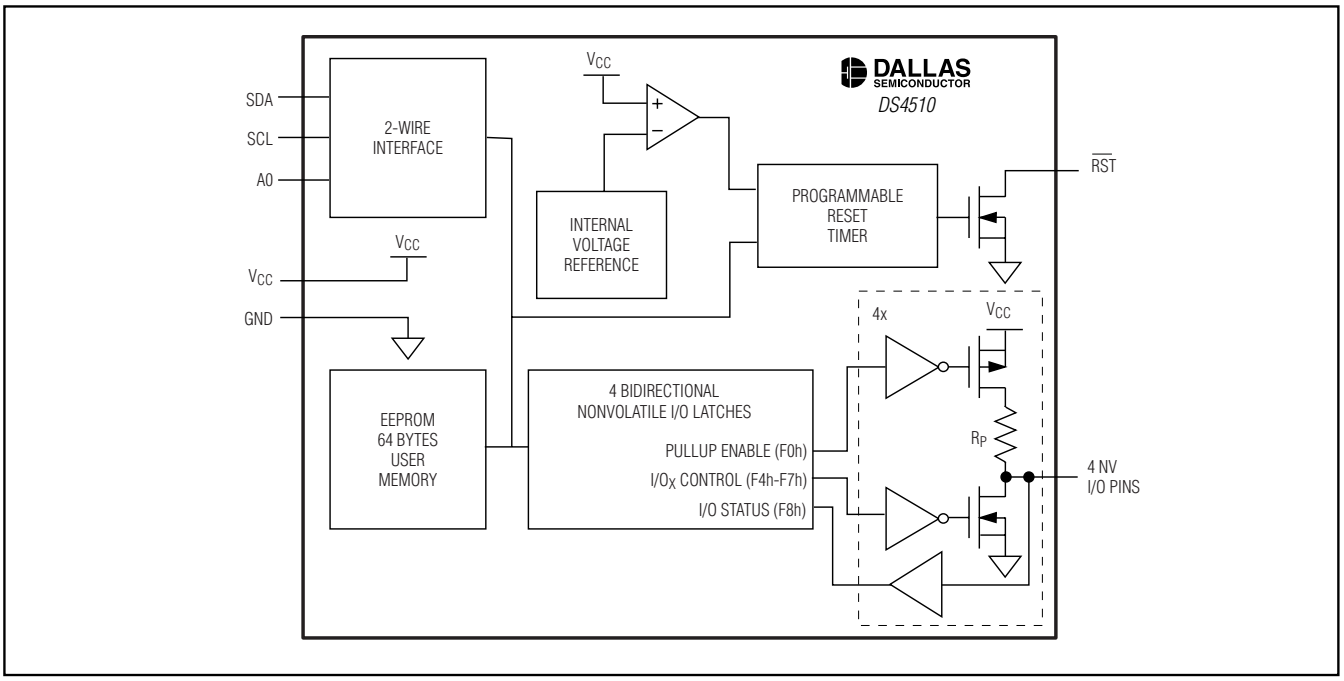


Pin Description

PIN	NAME	FUNCTION
1	A_0	I^2C Address Input. This input pin determines the chip address of the device. A_0 = 0 sets the slave address to 1010000b, A_0 = 1 sets the slave address to 1010001b.
2	SDA	Serial Data Input/Output. Bidirectional I^2C data pin.
3	SCL	Serial Clock Input. I^2C clock input.
4	V_{CC}	Power Input
5	GND	Ground
6	I/O3	Input/Output 3. I^2C accessible bidirectional I/O pin.
7	I/O2	Input/Output 2. I^2C accessible bidirectional I/O pin.
8	I/O1	Input/Output 1. I^2C accessible bidirectional I/O pin.
9	I/O0	Input/Output 0. I^2C accessible bidirectional I/O pin.
10	$\overline{RST}$	Active-Low Reset Output. Open-drain CPU supervisor reset output.

CPU Supervisor with Nonvolatile Memory and Programmable I/O

Functional Diagram



Detailed Description

The DS4510 contains a CPU supervisor, four programmable I/O pins, and a 64-byte EEPROM memory. All functions are configurable or controllable through an industry-standard I²C-compatible bus. DS4510 NV registers that are likely to require frequent modification are implemented using SRAM-shadowed EEPROM (SEEPROM) memory. This memory is configurable to act as volatile SRAM or NV EEPROM by adjusting the $\overline{SEE}$ bit in the Config register. Configuring the SEEPROM as SRAM eliminates the EEPROM write time and allows infinite write cycles to these registers. Configuring the registers as EEPROM allows the application to change the power-on values that are recalled during power-up.

Programmable CPU Supervisor

The timeout period is adjusted by writing the reset delay register (SEEPROM). The delay for each setting is shown in the *CPU Supervisor AC Electrical Characteristics*. If the $\overline{SEE}$ bit is set, changes are written to SRAM. On power-up the last value written to the EEPROM is recalled. The I²C bus is also used to activate the $\overline{RST}$ by setting the SWRST bit in the Config register. This bit automatically returns to zero after the timeout period. The Config register also contains the ready, trip point, and reset status bits. The ready bit determines if the power-on reset level of the DS4510 is surpassed by V_{CC}. The trip point bit determines if V_{CC} is above V_{CCTP}, and the reset status bit is set if $\overline{RST}$ is in its active state.

Note: The $\overline{RST}$ pin is an open-drain output, therefore an external pullup resistor must be used to realize high logic levels.

Programmable NV Digital I/O Pins

Each programmable I/O_X pin contains an input, open-collector output, and a selectable internal pullup resistor. The DS4510 stores changes to the I/O_X pin in SEEPROM memory. Using the SEEPROM as SRAM is conducive to applications such as I/O expansion that generally require fast access times and frequent modification of the I/O_X pin. Configuring the SEEPROM to behave as EEPROM allows the modification of the power-on state of the I/O_X pin. During power-up the I/O_X pins are high impedance until V_{CC} exceeds 2.0V (typically), which is when the last value programmed is recalled from EEPROM. On power-down, the I/O_X state is maintained until V_{CC} drops below 1.9V (typically).

The internal pullups for each I/O_X pin are controlled by the pullup-enable register (F0h). Similarly, the individual I/O_X control registers (F4h to F7h) adjust the pulldown

transistors. Read the I/O status register (F8h) to determine the logic levels present at the I/O pins.

User Memory

Three types of memory are present in the DS4510 (EEPROM, SEEPROM, and SRAM). The main user memory is 64 bytes of EEPROM starting at address 00h. This memory is not SRAM shadowed, so all writes to these locations result in EEPROM write cycles regardless of the state of the $\overline{SEE}$ bit. Additional memory for storing application data includes 6 bytes of SRAM (FAh–FFh), and 2 bytes of SEEPROM (F2h, F3h). Refer to the register memory map (Figure 3) for register addresses and memory types. Figure 4 shows the bit names for the memory-mapped I/O bytes and their factory default values.

The higher-order bits of the I/O registers that are not used, such as the four most significant bits of the pullup-enable byte (address F0h), can be used as additional memory. It is the responsibility of the application to ensure that writes to these bytes do not adversely affect bits controlling special functions of the DS4510.

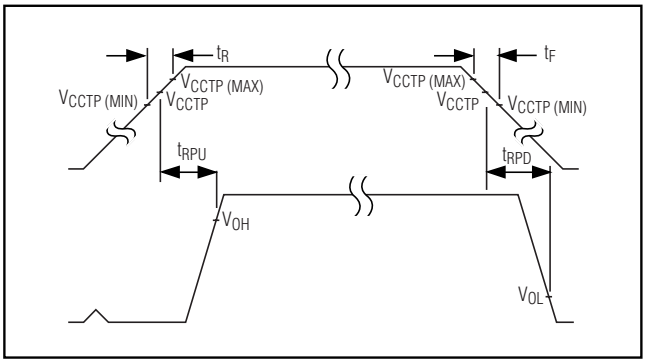


Figure 1. CPU Supervisor Power-Up and Power-Down Timing

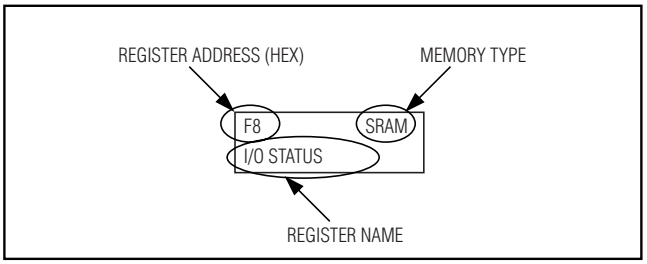


Figure 2. How to Read the Memory Map

00 EE USER BYTE	01 EE USER BYTE	02 EE User byte	03 EE USER BYTE	04 EE USER BYTE	05 EE USER BYTE	06 EE USER BYTE	07 EE USER BYTE
08 EE USER BYTE	09 EE USER BYTE	0A EE USER BYTE	0B EE USER BYTE	0C EE USER BYTE	0D EE USER BYTE	0E EE USER BYTE	0F EE USER BYTE
10 EE USER BYTE	11 EE USER BYTE	12 EE USER BYTE	13 EE USER BYTE	14 EE USER BYTE	15 EE USER BYTE	16 EE USER BYTE	17 EE USER BYTE
18 EE USER BYTE	19 EE USER BYTE	1A EE USER BYTE	1B EE USER BYTE	1C EE USER BYTE	1D EE USER BYTE	1E EE USER BYTE	1F EE USER BYTE
20 EE USER BYTE	21 EE USER BYTE	22 EE USER BYTE	23 EE USER BYTE	24 EE USER BYTE	25 EE USER BYTE	26 EE USER BYTE	27 EE USER BYTE
28 EE USER BYTE	29 EE USER BYTE	2A EE USER BYTE	2B EE USER BYTE	2C EE USER BYTE	2D EE USER BYTE	2E EE USER BYTE	2F EE USER BYTE
30 EE USER BYTE	31 EE USER BYTE	32 EE USER BYTE	33 EE USER BYTE	34 EE USER BYTE	35 EE USER BYTE	36 EE USER BYTE	37 EE USER BYTE
38 EE USER BYTE	39 EE USER BYTE	3A EE USER BYTE	3B EE USER BYTE	3C EE USER BYTE	3D EE USER BYTE	3E EE USER BYTE	3F EE USER BYTE
40	41	42	43	44	45	46	47
RESERVED							
E8	E9	EA	EB	EC	ED	EE	EF
F0 SEE *PULLUP ENABLE*	F1 SEE *RESET DELAY*	F2 SEE *USER BYTE*	F3 SEE *USER BYTE*	F4 SEE *I/O_3 CONTROL*	F5 SEE *I/O_2 CONTROL*	F6 SEE *I/O_1 CONTROL*	F7 SEE *I/O_0 CONTROL*
F8 SRAM *I/O STATUS*	F9 SRAM *CONFIG*	FA SRAM USER BYTE	FB SRAM USER BYTE	FC SRAM USER BYTE	FD SRAM USER BYTE	FE SRAM USER BYTE	FF SRAM USER BYTE

*ITALICIZED BYTES HAVE BIT DESCRPTIONS, REFER TO FIGURE 3.

Figure 3. Register Memory Map

REGISTER NAME	REGISTER LOCATION (HEX)	REGISTER BIT NAMES								FACTORY OR POWER-ON DEFAULT (BIN)
		Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
User EEPROM	00-3F	EE	EE	EE	EE	EE	EE	EE	EE	00000000
Reserved	40-EF	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Pullup Enable	F0	SEE	SEE	SEE	SEE	I/O3 pullup	I/O2 pullup	I/O1 pullup	I/O0 pullup	00000000
$\overline{RST}$ Delay	F1	SEE	SEE	SEE	SEE	SEE	SEE	TD1	TD0	00000011
User SEE	F2	SEE	SEE	SEE	SEE	SEE	SEE	SEE	SEE	00000000
User SEE	F3	SEE	SEE	SEE	SEE	SEE	SEE	SEE	SEE	00000000
I/O3 Control	F4	SEE	SEE	SEE	SEE	SEE	SEE	SEE	I/O3	00000001
I/O2 Control	F5	SEE	SEE	SEE	SEE	SEE	SEE	SEE	I/O2	00000001
I/O1 Control	F6	SEE	SEE	SEE	SEE	SEE	SEE	SEE	I/O1	00000001
I/O0 Control	F7	SEE	SEE	SEE	SEE	SEE	SEE	SEE	I/O0	00000001
I/O Status	F8	0	0	0	0	I/O3 Status	I/O2 Status	I/O1 Status	I/O0 Status	n/a
Config	F9	$\overline{ready}$	trip point	reset status	$\overline{SEE}$	SWRST	0	0	0	XXX00000
User SRAM	FA-FF	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM	SRAM	00000000

Figure 4. Register Bit Names

I²C Definitions

The following terminology is commonly used to describe I²C data transfers.

Master Device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses, start, and stop conditions.

Slave Devices: Slave devices send and receive data at the master's request.

Bus Idle or Not Busy: Time between stop and start conditions when both SDA and SCL are inactive and in their logic-high states. When the bus is idle it often initiates a low-power mode for slave devices.

Start Condition: A start condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a start condition. See the timing diagram for applicable timing.

Stop Condition: A stop condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a stop condition. See the *I²C Timing Diagram* for applicable timing.

Repeated Start Condition: The master can use a repeated start condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated starts are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated start condition is issued identically to a normal start condition. See the *I²C Timing Diagram* for applicable timing.

Bit Write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL (see Figure 5) plus the setup and hold-time requirements. Data is shifted into the device during the rising edge of the SCL.

Bit Read: At the end a write operation, the master must release the SDA bus line for the proper amount of setup

Table 1. Register Definitions

REGISTER LOCATION (HEX)	REGISTER NAME	FUNCTION
00 to 3F	User EEPROM	64 bytes of EEPROM memory.
40 to EF	Reserved	These memory locations are reserved for future products.
F0	Pullup Enable	The four least significant bits of this register each enable/disable one of the internal pullup resistors. Set the bit to enable the pullup, clear it to disable the pullup.
F1	$\overline{RST}$ Delay	The two LSBs of this register (TD1 and TD0) select the reset delay ($t_{\overline{RST}}$) as shown in the *CPU Supervisor AC Timing Characteristics*.
F2 to F3	User SEEPROM	SRAM Shadowed EEPROM user byte.
F4 to F7	I/O_X Control	Clearing the LSB of the register enables the I/O_X pulldown transistor; setting the bit disables the pulldown transistor.
F8	I/O Status	This register reflects the logic level of the I/O_X pins. The upper four bits of this register always read zero.
F9	Config	This register contains 5 bits that read and control the behavior of the part as follows:
	Bit Name	*Bit Function*
	$\overline{ready}$	Reads zero when V_{CC} is above the DS4510's power-on reset voltage.
	Trip Point	Reads one when V_{CC} below V_{CCTP}.
	Reset Status	Reads one when the $\overline{RST}$ pin is active.
	$\overline{SEE}$	When zero, writes to the SEEPROM registers behave like EEPROM. When one, writes to the SEEPROM registers behave like SRAM.
	SWRST	Setting this bit activates the $\overline{RST}$ output. This bit automatically returns to zero during the $\overline{RST}$ active time.
FA to FF	User SRAM	6 bytes of SRAM memory

time (see Figure 5) before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses, including when it is reading bits from the slave.

Acknowledgement (ACK and NACK): An Acknowledgement (ACK) or Not Acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during the 9th bit. A device performs a NACK by transmitting a one during the 9th bit. Timing (Figure 5) for the ACK and NACK is identical to all other bit writes. An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or as an indication that the device is not receiving data.

Byte Write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgement from the slave to the master. The 8 bits transmitted by the master are done according to the bit-write definition and the acknowledgement is read using the bit-read definition.

Byte Read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit-read definition above, and the master transmits an ACK using the bit-write definition to receive additional data bytes. The master must NACK the last byte read to terminate communication so the slave will return control of SDA to the master.

Slave Address and the R/$\overline{W}$ Bit: Each slave on the I^2C bus responds to a slave addressing byte sent immediately following a start condition. The slave address byte contains the slave address and the R/$\overline{W}$ bit. The slave address (see Figure 6) is the most significant 7 bits and the R/$\overline{W}$ bit is the least significant bit.

The DS4510's slave address is $101000A_0$ (binary), where A_0 is the value of the A_0 address pin. The

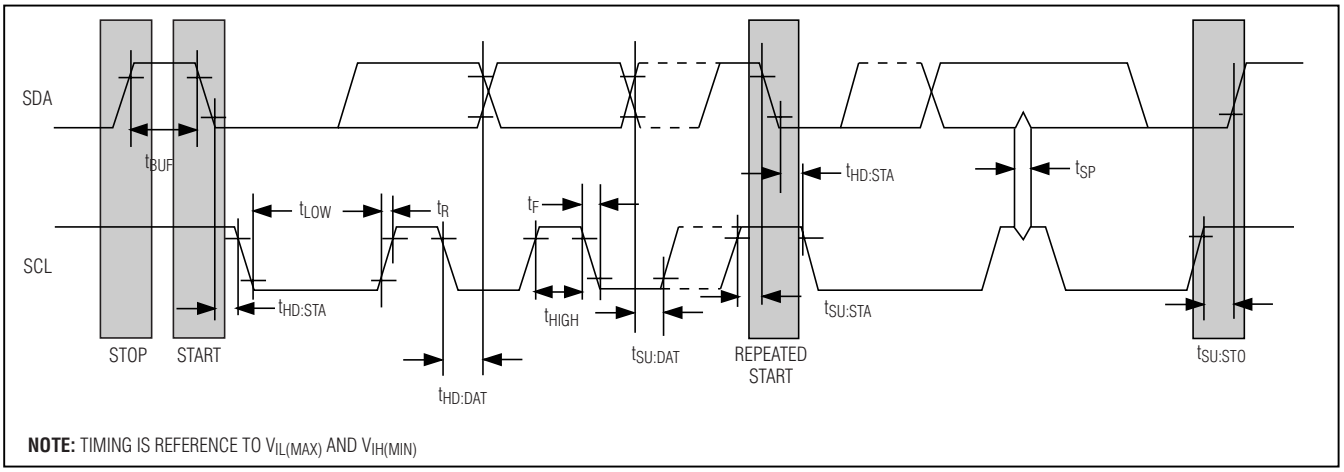


Figure 5. I²C Timing Diagram

address pin allows for the DS4510 to respond to one of two slave addresses (1010000X, or 1010001X). If the R/$\overline{W}$ bit is zero, the master writes data to the slave. If the R/$\overline{W}$ is one, the master reads data from the slave.

Memory Address: During an I²C write operation, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte (R/$\overline{W}$ = 0).

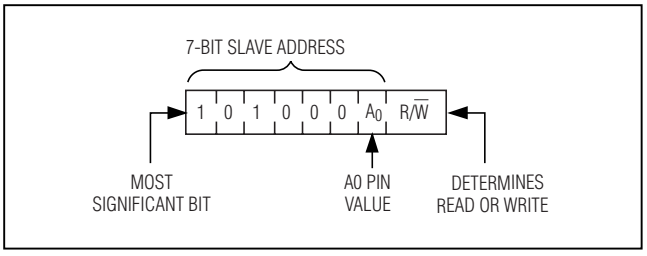


Figure 6. DS4510's Slave Address and the R/$\overline{W}$ Bit

I²C Communications

Writing a Single Byte to a Slave: The master must generate a start condition, write the slave address (R/$\overline{W}$= 0), write the memory address, write the byte of data and generate a stop condition. Remember the master must read the slave's acknowledgement during all byte write operations.

Writing a Multiple Bytes to a Slave: To write multiple bytes to a slave the master generates a start condition, writes the slave address (R/$\overline{W}$ = 0), writes the memory address, writes up to 8 data bytes, and generates a stop condition.

The DS4510 can write 1 to 8 bytes (one page or row) with a single write transaction. This is internally controlled by an address counter that allows data to be written to consecutive addresses without transmitting a memory address before each data byte is sent. The address counter limits the write to one 8-byte page (one row of the memory table, see Figure 3). Attempts to write to additional pages of memory without sending a stop condition between pages results in the address counter wrapping around to the beginning of the present row.

Example: A 3-byte write starts at address 06h and writes three data bytes (11h, 22h, and 33h) to three "consecutive" addresses. The result would be addresses 06h and 07h would contain 11h and 22h, respectively, and the third data byte, 33h, would be written to address 00h.

To prevent address wrapping from occurring, the master must send a stop condition at the end of the page, then wait for the bus-free or EEPROM-write time to elapse. The master may then generate a new start con-

dition, write the slave address (R/$\overline{W}$ = 0), and the first memory address of the next page before continuing to write data.

Acknowledge Polling: Any time an EEPROM page is written, the DS4510 requires the EEPROM write time (t_W) after the stop condition to write the contents of the page to EEPROM. During the EEPROM write time, the DS4510 does not acknowledge its slave address because it is busy. It is possible to take advantage of that phenomenon by repeated addressing the DS4510, which allows the next page to be written as soon as the DS4510 is ready to receive the data. The alternative to acknowledge polling is to wait for maximum period of t_W to elapse before attempting to write again to the DS4510.

EEPROM Write Cycles: When EEPROM writes occur, the DS4510 writes the whole EEPROM memory page even if only a single byte on the page was modified. Writes that do not modify all 8 bytes on the page are allowed and do not corrupt the remaining bytes of memory on the same page. Because the whole page is written, bytes on the page that were not modified during the transaction are still subject to a write cycle. This can result in a whole page being worn out over time by writing a single byte repeatedly. Writing a page one byte at a time wears the EEPROM out eight times faster than writing the entire page at once. The DS4510's EEPROM memory is guaranteed to handle 50,000 write cycles at +70°C. Writing to SEEPROM memory with $\overline{SEE}$ = 1 does not count as an EEPROM write cycle when evaluating the EEPROM's estimated lifetime.

Reading a Single Byte from a Slave: Unlike the write operation that uses the memory address byte to define where the data is to be written, the read operation occurs at the present value of the memory address counter. To read a single byte from the slave the master generates a start condition, writes the slave address with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a stop condition.

Manipulating the Address Counter for Reads: A dummy write cycle can be used to force the address counter to a particular value. To do this the master generates a start condition, writes the slave address (R/$\overline{W}$ = 0), writes the memory address where it desires to read, generates a repeated start condition, writes the slave address (R/$\overline{W}$ = 1), reads data with ACK or NACK as applicable, and generates a stop condition.

See Figure 7 for a read example using the repeated start condition dummy write cycle.

Reading Multiple Bytes from a Slave: The read operation can be used to read multiple bytes with a single transfer. When reading bytes from the slave, the master simply ACKs the data byte if it desires to read another byte before terminating the transaction. After the master reads the last byte it NACKs to indicate the end of the transfer and generates a stop condition. This can be done with or without modifying the address counter's location before the read cycle. The DS4510 does not wrap on page boundaries during read operations, but the counter rolls from its upper-most memory address FFh to 00h if the last memory location is read during the read transaction.

Example: The entire memory contents of the DS4510 can be read with a single transfer starting at address F0h that reads 80 bytes of data. Addresses F0h to FFh are read sequentially, the address counter rolls to 00h, and then addresses 00h to 3Fh can be read sequentially. This allows the entire memory contents to be read in a single operation without reading the undefined contents of the reserved area of the memory.

Application Information

Advantages of Using the $\overline{SEE}$ Bit to Disable EEPROM Writes

The $\overline{SEE}$ bit allows EEPROM writes to be disabled for the SRAM-shadowed EEPROM bytes, allowing the SRAM of SEE registers to change without writing the EEPROM to the same value. This prevents write operations from changing the power-on value of the I/O pins, reduces the number of EEPROM write cycles, and speeds up I/O operations because the DS4510 does not require an internally timed EEPROM write cycle to complete the operation.

Power-Supply Decoupling

To achieve the best results when using the DS4510, decouple the power supply with a 0.01µF or a 0.1µF capacitor. Use high-quality, ceramic, surface-mount capacitors, and mount the capacitors as close as possible to the V_{CC} and GND pins of the DS4510 to minimize lead inductance.

SDA and SCL Pullup Resistors

SDA is an open-collector output on the DS4510 that requires a pullup resistor to realize high logic levels. Because the DS4510 does not utilize clock cycle stretching, a master using either an open-collector output with a pullup resistor or a normal output driver can be utilized for SCL. Pullup resistor values should be chosen to ensure that the rise and fall times listed in the *AC Electrical Characteristics* are within specification.

CPU Supervisor with Nonvolatile Memory and Programmable I/O

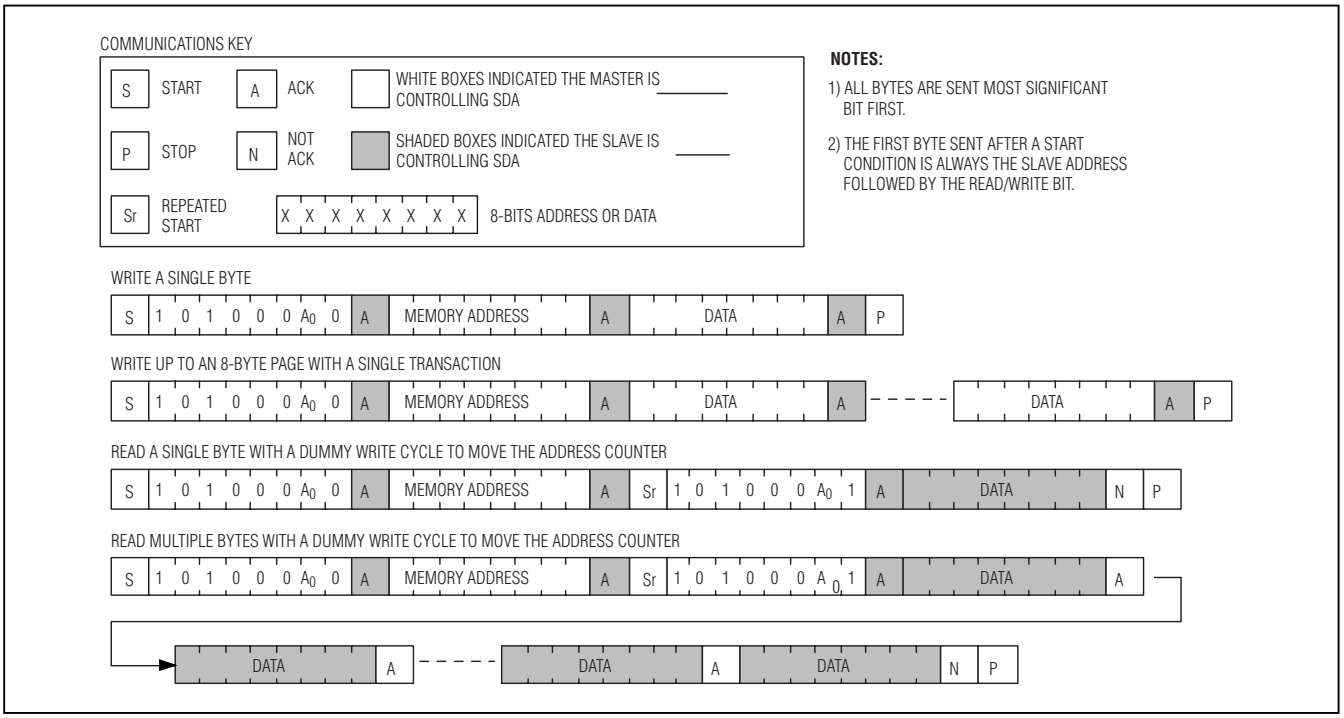


Figure 7. I²C Communications Examples

Chip Topology

TRANSISTOR COUNT: 16559

SUBSTRATE CONNECTED TO GROUND

Package Information

For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo.**