MC28R36M Datasheet

CENTELLAX

Clock Recovery Unit (CRU) Module

Features

- 27.9 - 36.0 Gb/s Data Rates
- High Input Sensitivity
- Low Jitter Output Clock
- Low Power Consumption
- Single -3.3V Power Supply

Description

The MC28R36M is a Clock Recovery Unit (CRU) using Silicon Germanium (SiGe) process technology. The module accepts input data rates at 27.95 Gb/s with an input sensitivity greater than 50mVppk. The data input is AC coupled and terminated with a 50 ohm resistor to minimize reflections. The half-rate recovered clock is AC-coupled at ECL compatible levels.

Applications

The MC28R36M can be used to extract low jitter clock for 100 GE applications operating at transmission speeds of 27.95 Gb/s. Broadband test systems will benefit from the low power dissipation, precision connectors and excellent signal quality. The MC28R36M also locks to half-rate data to cover 16 Gb/s Fibre Channel (16 GFC).

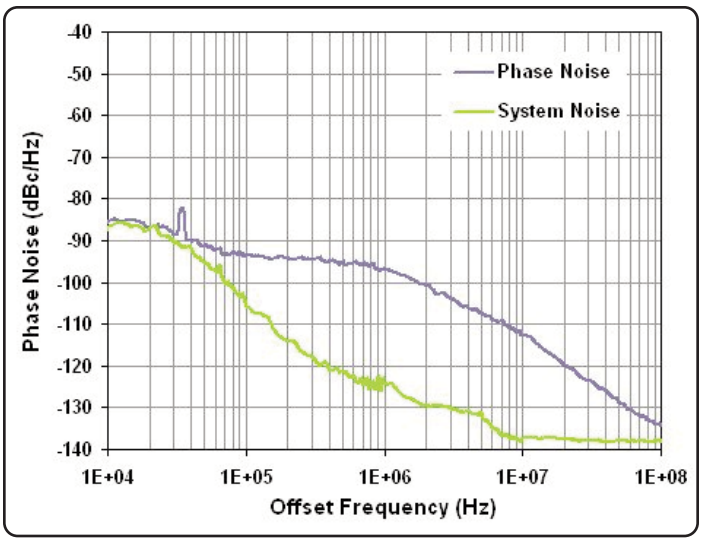
Operating Conditions

Parameter	Minimum	Typical	Maximum	Units
Vee	-3.6	-3.3	-3.0	V

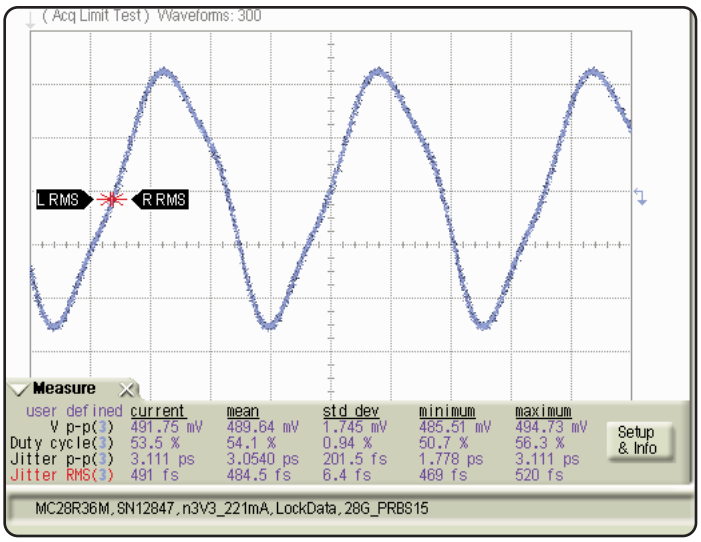
Key Specifications @ 25°C

Vee= -3.3V, Iee = 220mA, Zo = 50 Ω

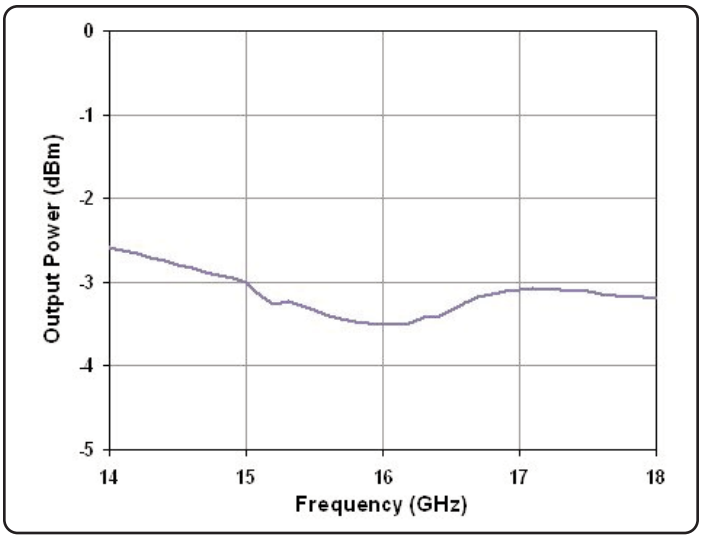
Parameter	Minimum	Typical	Maximum	Units
Data Input				
Bit Rate	27.9	-	36.0	Gb/s
Amplitude	50	-	1400	mVpp
Reference Clock Input				
Frequency	6.975	-	9.0	GHz
Amplitude	50	-	1400	mVpp
Clock Output				
Frequency	13.95	-	18.0	GHz
Amplitude	300	-	600	mVpp
Jitter RMS	-	0.4	0.6	psec
Jitter Pk-Pk	-	3	6	psec



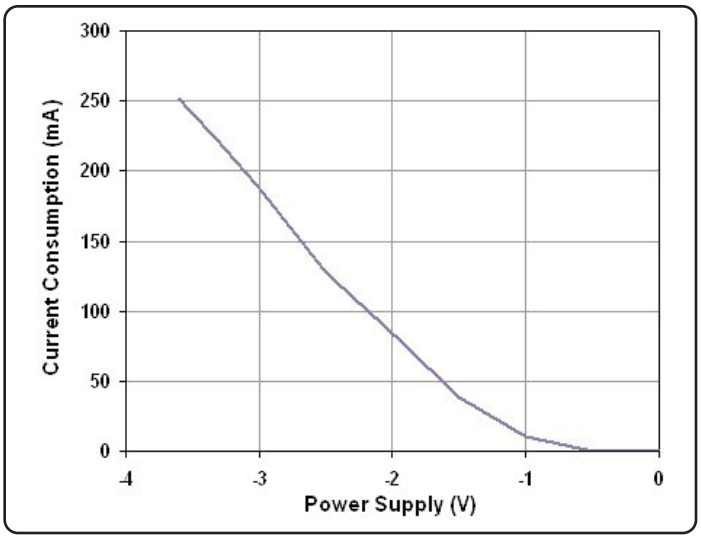
Phase Noise of CKO at 14.0 GHz
Locked to 2e15, 28.0 Gb/s data



14.0 GHz Clock Output
Locked to 2e15, 28.0 Gb/s data



Output Power vs Frequency

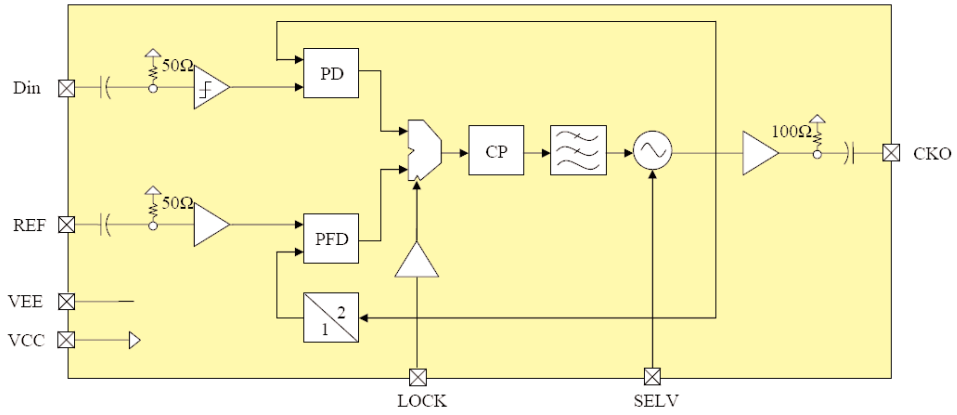


Total Current Consumption vs Power Supply Level

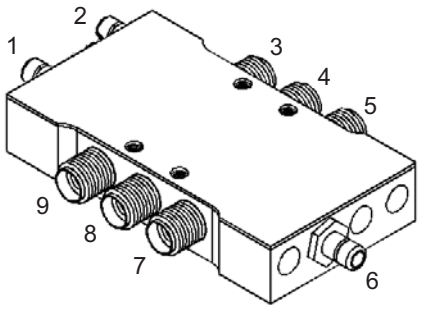
Absolute Maximum Ratings

Parameter	Value	Unit
Supply Voltage (VEE)	-3.8	V
Ref Power (REF)	+10	dBm
DC Voltage Level (Din,REF,CKO)	+/-1	V
Operating Temperature	0 to 70	ºC
Storage Temperature	-85 to 125	ºC

Functional Block Diagram



Module Outline



Pin Description

Name	Pin	Description	Note	Connector
LOCK	1	Reference Input Selector	Internal PLL Reference Selector Between Input Data and Reference Clock	SMB
SELV	2	Frequency Range Selector	Selects Between Two VCOs for Lower/Upper Band	SMB
CKO	5	Half-Rate Clock Output	Single Ended Output	2.9mm(K)
VEE	6	Negative Supply Voltage	Center Pin -3.3V, Shield/Case is ground	SMB
REF	7	Reference Clock Input	Positive Differential Input	2.9mm(K)
DIN	9	Data Input	Single Ended Input	2.9mm(K)
NC	3,4,8	No Connect		

LOCK Logic

Parameters	State	Min	Typ	Max	Unit
Low (default)	Reference Clock	-	-3.3	-	V
High	Data	-	0	-	V

SELV Logic

Parameters	State	Min	Typ	Max	Unit
Low (default)	27.9 - 32.0 Gb/s	-	-3.3	-	V
High	32.0 - 36.0 Gb/s	-	0	-	V

Application Note

Clock Recovery

The MC28R36M has two loops with two separate inputs -- one for training the loop to the right frequency, and the other for phase locking the loop to the actual data. Refer to page 3 for block diagram. The part requires a 1/4 rate clock for training the CRU. Once the loop is trained, the input should be switched over to the data input by setting the LOCK pin (pin 1) High (or 0V).

Clock Recovery Procedure

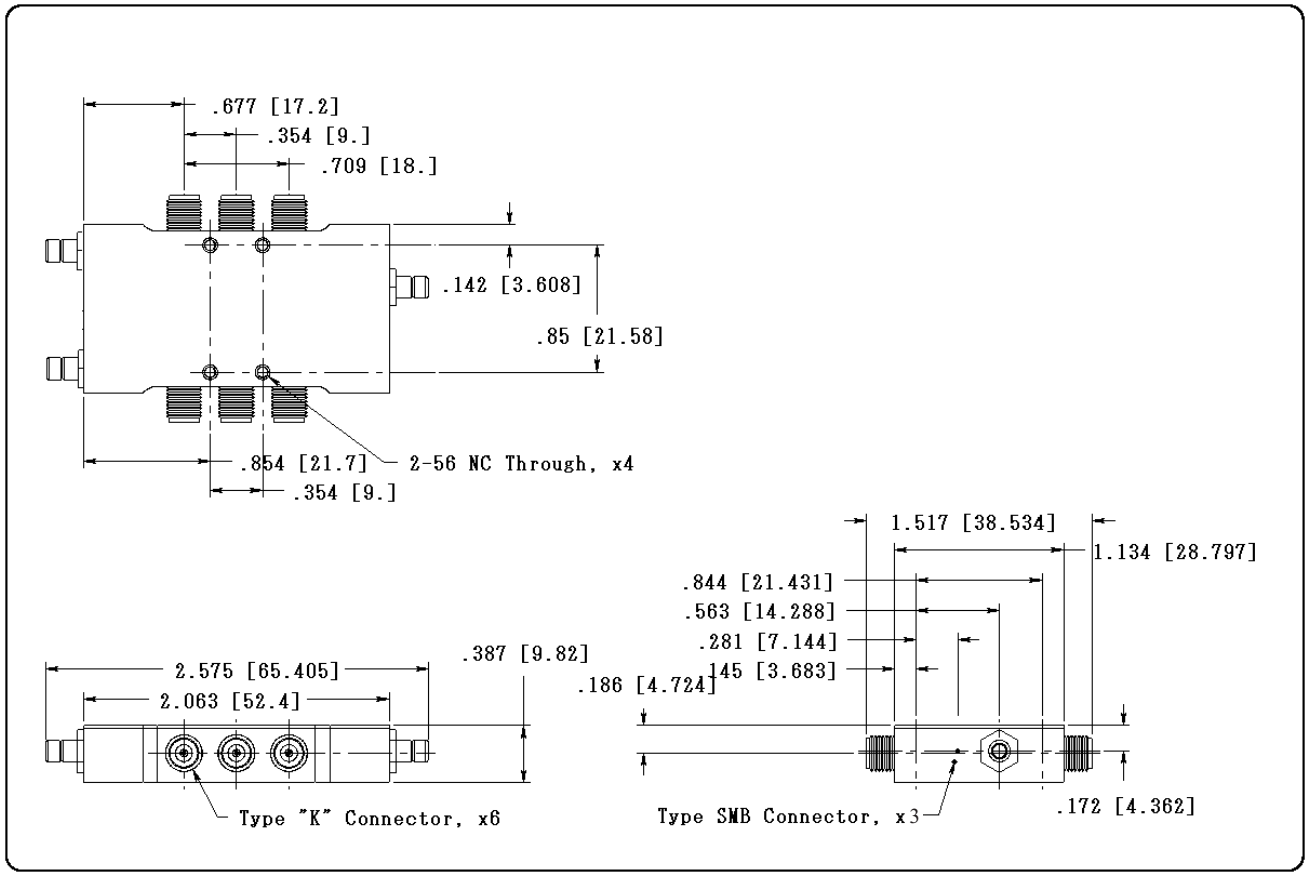
1. Connect both data and reference inputs to the device. The reference clock should be 1/4 of the data rate. For example, if data rate is 27.95 Gbps, then reference clock is 6.9875 GHz (sine or square). Make sure that the LOCK pin (pin 1) is set to Low, or -3.3V, or left open (it defaults to logic state Low).

2. Monitor the output frequency to see if the loop has locked to the desired frequency, which should be half-rate. For this example, the loop is locked if CKO is 13.975 GHz.

3. Once the loop is locked (i.e. trained), switch the LOCK pin to High, or 0V, to lock onto the data input.

**The MC28R36M may also be trained using 1/8 or 1/16 of the data rate as the reference clock input; however, the VCO capture range will be reduced.*

Packaging Information



All measurements in inches (mm)