MCS7781

USB to IrDA Port

Features

- Low-power CMOS design
- Powered from USB port
- Single 12 MHz crystal
- IrDA data rates from 2.4 Kbps to 115.2 kbps in SIR mode
- Supports MIR (Medium IR) at 1.152 Mbps
- Supports FIR (Fast IR) mode with data rate of 4 Mbps
- Uses standard IrDA transceivers
- USB Specification 1.1 compliant
- Supports all USB standard commands
- Full compliance to IrDA 1.4
- Internal Power-On Reset
- On-Chip Regulator
- EEPROM Interface
- Re-configurable Vendor-Specific parameters (Vendor-ID, Product-ID, Release #)
- Support for 4 string descriptors (Language-ID, Manufacturer-ID, Product Name, Serial Number)
- 28-pin SSOP package

Applications

- Add-on IrDA dongle
- Cell Phones
- Embedded Applications

Application Note

- AN-7781

Evaluation Board

- MCS7781-EVB

IrReady

IrDA Reference Product

"IrReady Qualified"
in Demo Adapters
Customer boards require IrDA qualification

General Description

The MCS7781 controller provides bridging between the Universal Serial Bus (USB) and an IrDA wireless data communication port. This device contains all the necessary logic to communicate with the host computer via the USB bus.

MCS7781 contains an on-chip regulator & operates in bus-powered mode. MCS7781 has a reduced frequency (12MHz) crystal oscillator. MCS7781 also has an optional EEPROM Interface.

This combination of features allows significant cost savings in system designs, along with straight forward implementation of IrDA port functionality into PC peripherals using the host's USB port.

Ordering Information		
Commercial Grade (0 °C to +70 °C)		
MCS7781CS-GR	28-SSOP	RoHS

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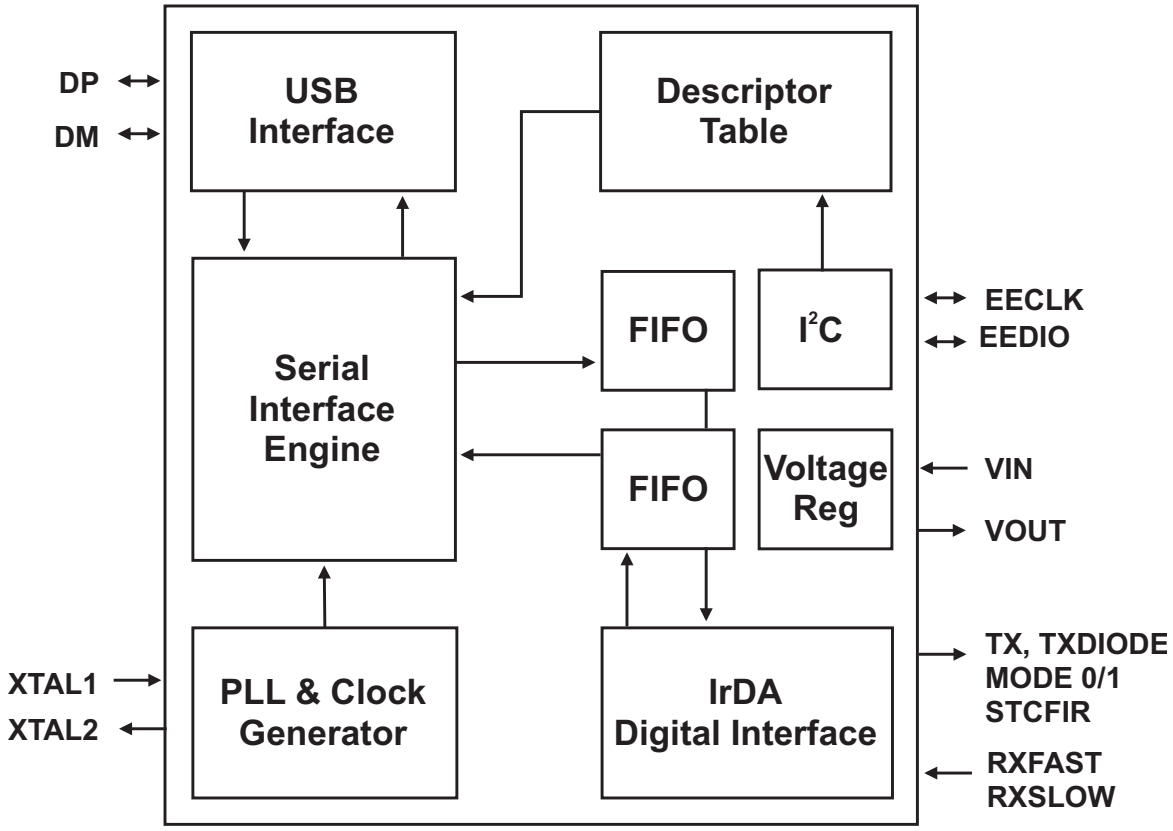
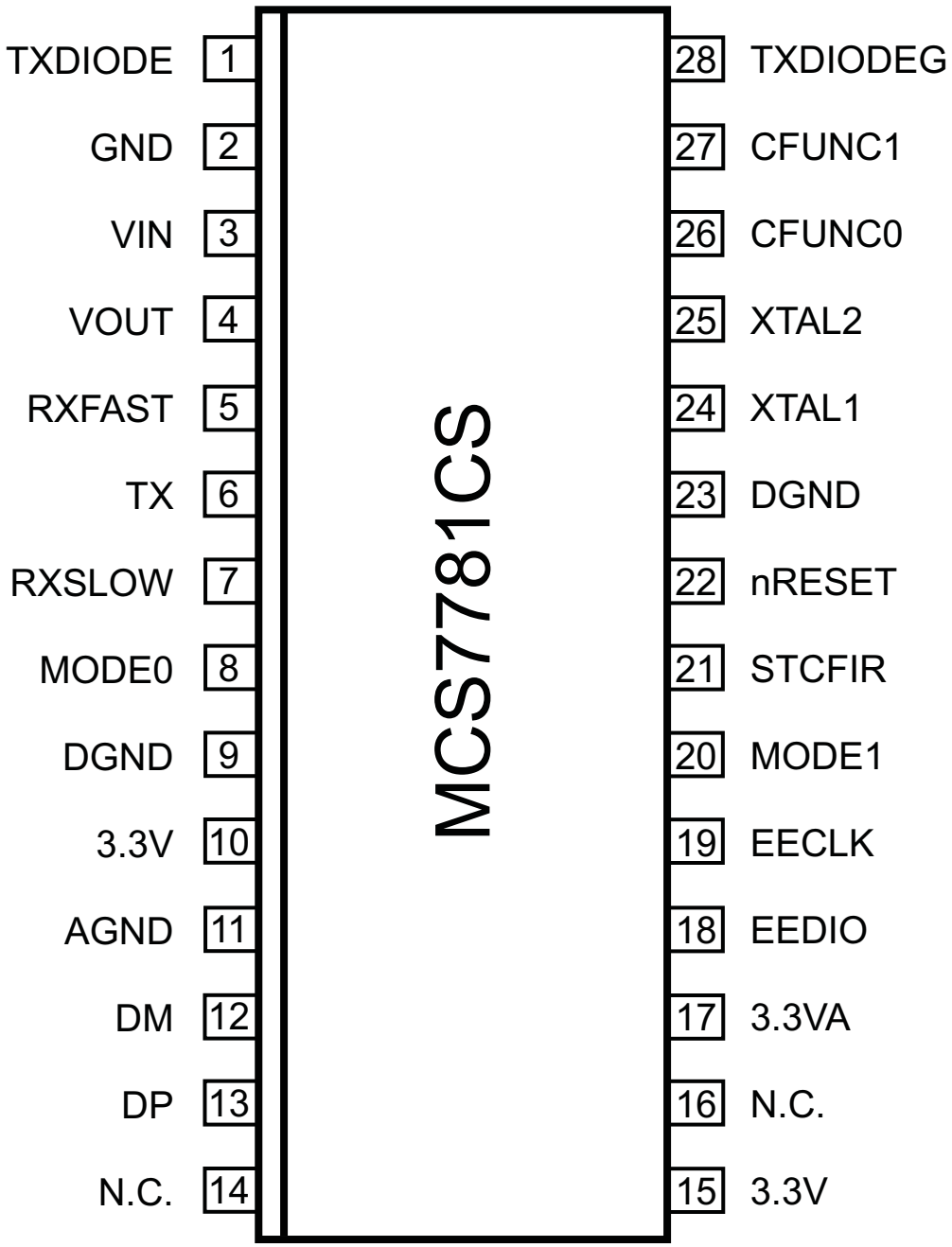
Block Diagram



Pinout Diagram



Pin Assignments

Name	Pin	Type	Description
TXDIODE	1	O	Optional Transmit LED driver output
VIN	3	PWR	Main Power Input (5V). Connect to USB VBUS or local 5V Supply
VOUT	4	PWR	3.3V, Voltage Regulator Output. All 3.3V supply pins need to be connected to this pin
RXFAST	5	I	Receive data from IR module (Fast)
TX	6	O	Transmit Data output to IR module
RXSLOW	7	I	Receive data from IR module (Slow)
MODE0	8	O	Mode control to IR module
DM	12	I/O	USB interface Negative Data
DP	13	I/O	USB interface Positive Data
EEDIO	18	I/O	External EEPROM Data IN / OUT (I^2C format)
EECLK	19	I/O	External EEPROM Clock (I^2C format)
MODE1	20	O	Mode control to IR module
STCFIR	21	O	Static FIR select
nRESET	22	I	Master Reset, active low
XTAL1	24	I	12 MHz crystal/clock input
XTAL2	25	O	12 MHz crystal/clock output
CFUNC0	26	I	Internal mode control (Internal pull-up). Should be left open
CFUNC1	27	I	Internal mode control (Internal pull-up). Should be left open
TXDIODEG	28	PWR	Optional LED driver output GND
5VA	17	PWR	USB transceiver power supply
5V	10, 15	PWR	USB transceiver power supply
AGND	23	PWR	USB transceiver power supply ground
DGND	2, 9, 11	PWR	Digital Power supply ground

Functional Description

The MCS7781 consists of two major functional blocks, the USB Controller and the Digital IR Transceiver. The USB Controller provides Control, Bulk-In, and Bulk-Out endpoints to the USB host. The Digital IR Transceiver consists of transmit and receive interfaces that connect to an analog IR front end.

This USB/IrDA Bridge Controller has full interface capability to connect between a USB bus, and an IrDA compatible infrared transceiver device.

USB Interface

The USB Device Controller implements the USB protocol engine. It has one configuration with a single interface. Two Bulk end-points, with maximum packet size of 64 Bytes, are used for data transfers. The MCS7781 uses a vendor specific implementation of IR configuration and control. Two vendor specific requests are defined for this purpose, 1. Write Word, and 2. Read Word. The vendor specific requests are piped through the control endpoint.

"Write Word" is a 2 phase transaction which can be used to write a single 16-bit register. The setup phase of this command supplies both the index and data value to be written into the register. There is no data phase in this transfer.

"Read Word" requests are used to read the register contents of MCS7781. It allows reading one 16-bit register at a time. The setup phase specifies the register address to be read, and the data is returned in data phase.

Digital IR Transceiver

The Digital IR Transceiver is responsible for driving the transmit diode and receiving the digital input from an analog IR front end. The primary components are the transmit modulator, the receive demodulator, the FIFO, the analog transmit section, and the register array.

By programming the registers in the register array, the device's operation is determined. Various registers are used to specify operations such as the modulation scheme, the BAUD Rate, the current frame size in the FIFO, the RX input selection, etc.

In steady state transmit operation, the USB controller is filling the FIFO with data while the Digital IR Transceiver is emptying it via the transmit modulator. In steady state receive operation, the USB controller is emptying the FIFO while the RX demodulator is filling the FIFO.

IR FRAMING

Framing involves adding wrappers around the payload received from NDIS to make a valid IR frame. MCS7781 uses a custom framing style to achieve low gate counts. The hardware and software together play a role in making SIR, MIR, and FIR frames.

Mode Register
Offset: 0x00

Name	Bit	Access	Default	Description
FIR *	0	R/W	0	1 = Puts the device in fast infrared mode (4 MHz). 0 = When cleared, puts the device in SIR/MIR mode based on Baud Rate register.
SIR *	1	R/W	0	1 = The SIR pulse width of 1.6 uS is used. 0 = The SIR pulse used is 3/16th of bit time.
BBTG	2	R/W	1	1 = Enables back to back transmission with no inter-packet gap. *Invalid in SIR mode.*
ASK *	3	R/W	0	1 = Puts the device in ASK mode. 0 = Device not in ASK mode.
PARITY *	4	R/W	0	1 = Odd parity to be used by ASK. 0 = Even parity is used
RATE *	[7:5]	R/W	0x01	BAUD Rate selector.
PLLPWD	8	R/W	1	1 = Enable power down feature of the PLL 0 = Power down feature of the PLL disabled.
DRIVER	9	R/W	0	1 = State after initialization. 0 = State after Reset.
DTD	10	R/W	1	1 = Device determines the transfer direction automatically. 0 = The direction is controlled by software by writing a 1 (TX) or 0 (RX) in DIR bit of this register
DIR	11	R/W	0	*This bit controls the direction of transfer.* 1 = Transmit 0 = Receive *This bit is valid only when AUTO = 0.* *Software should check the CHGDIR bit before writing to this bit.*
SIPEN	12	R/W	1	1 = Enables the automatic generation of SIP pulse from the hardware. 0 = Disables the auto SIP generation. SIP is generated by software through vendor specific commands.
SENDSIP	13	R/W	0	On detecting a transition from low to high on this bit, the device generates a SIP.
CHGDIR	14	R	1	1 = Software is allowed to change the transfer direction by writing to DIR bit. 0 = Direction change is not allowed. Software polls until this bit goes high before changing the direction.
RESET	15	R/W	1	0 = Resets the bridge and IR TOP modules. *This bit self clearing.*

* Changes to these bits require resetting the IR System

The “Rate” field (bits[7:5]) allow selecting the desired BAUD Rate for data transfers. This table shows the data rates available.

Rate Field	BAUD Selected
0	2.4 Kbps
1	9.6 Kbps
2	19.2 Kbps
3	38.4 Kbps
4	57.6 Kbps
5	115.2 Kbps
6	0.576 Mbps
7	1.152 Mbps

Framing Register
Offset: 0x01

Name	Bit	Access	Default	Description
STAL *	[7:0]	R/W	0x00	*The six least significant bits indicate the number of STAs.* Bit-7 = 1, The 6 LSBs are used as the number of STAs. Bit-7 = 0, Uses the values hard coded in the design.
IPG *	[15:8]	R/W	0x00	*Inter packet gap* *Specified in terms of number of bit times (MIR)* *or chip time (FIR).* Bit-15 = 1, The 6 LSBs are used as the inter packet gap. Bit-15 = 0, Uses the values hard coded in the design.

* Changes to these bits require resetting the IR System

XCVR Register
Offset: 0x02

Name	Bit	Access	Default	Description
MODE0	0	R/W	0	The usage varies with the transceiver make and is reflected in the transceiver truth table.
STFIR	1	R/W	0	The usage varies with the transceiver make and is reflected in the transceiver truth table.
XCVR	2	R/W	0	1 = Puts the transceiver in configuration mode. 0 = Puts the transceiver in data transfer mode.
RXFAST	3	R/W	0	1 = Causes the device to use RXFAST as the input pin for receive from transceiver. 0 = Causes the device to use RXSLOW as the receive signal.
TXCUR	[6:4]	R/W	000	These bits control the current supplied to the TX-LED.
MODE1	7	R/W	0	The usage varies with the transceiver make and is reflected in the transceiver truth table.
SMODE0	8	R/W	1	Value of MODE0 to put the device into shut down. Varies with transceiver make.
SMODE1	9	R/W	0	Value of MODE1 to put the device into shut down. Varies with transceiver make.
INVTX	10	R/W	0	1 = Inverts the data bits sent to the transceiver. 0 = The transmit line works as an active high signal.
INVRX	11	R/W		1 = RXD line from transceiver is treated as an active low signal. 0 = RXD line from transceiver is treated as an active high signal.
EEDATA	[15:12]	R	0000	Loaded from the EEPROM.

This table shows the usage of XCVR Register for various Transceivers.

Vendor	Code	Dynamic Configuration			
		MODE0	MODE1	STC_FIR	Latched From
Vishay TDFU6614	0	1->0	0	0	TXD
Vishay TDFU6102	0	1->0	0	0	TXD
SHARP GP2W100YP	1	1->0	0	1	TXD
Agilent 3602/3600	2	Can switch pins dynamically. There is no latching mechanism			

SIP Resister
Offset: 0x03

Name	Bit	Access	Default	Description
SIPON	[6:0]	R/W	0x4C	*Pulse width of the SIP.* Specified as number of 48 MHz clocks.
SIPOFF	[15:7]	R/W	0x154	*The SIP low time.* Specified as number of 48 MHz clocks.

MINRXPW Register
Offset: 0x04

Name	Bit	Access	Default	Description
MNRXW	[15:0]	R/W	0x00	*Minimum pulse width of the signal to be received.* 0 = device uses the hard coded values. X (non zero) = device uses the value specified in this register.

TXPW Register
Offset: 0x05

Name	Bit	Access	Default	Description
TXPW	[15:0]	R/W	0x00	*Pulse width of the signal transmitted.* 0 = device uses the hard coded values X (non zero) = device uses the value specified in this register.

RFIFO2
Offset: 0x06

Name	Bit	Access	Default	Description
TIMEOT	[7:0]	R/W	0x0A	*Timeout specified in terms of 50 mS. Used in SIR mode to abort a receive if idle for a long period specified by this register.* N => N*50 mS timeout.
TRSHD	[14:8]	R/W	0x40	FIFO Threshold
CLRFF	15	R/W	0	1 = Clear FIFO pointers 0 = FIFO pointers not cleared *This bit is self clearing*

RESV Register
Offset: 0x07

Name	Bit	Access	Default	Description
RESV	[15:2]	R/W	0x0A	Reserved
IRINRX	1	R	0	1 = Indicates that receive is in progress 0 = Indicates that receive is not in progress
IRINTX	0	R	0	1 = Indicates that transmit is in progress 0 = Indicates that transmit is not in progress

Electrical Characteristics

Absolute Maximum Ratings

Supply Voltage	6.0 V
Voltage at any pin	GND – 0.3V to VCC + 0.3V
Operating Temperature	0 °C to +70 °C
Storage Temperature	-65 °C to +150 °C
Package Dissipation	500 mW
ESD	±2000 V
Latch up	220 mA

DC Electrical Specification

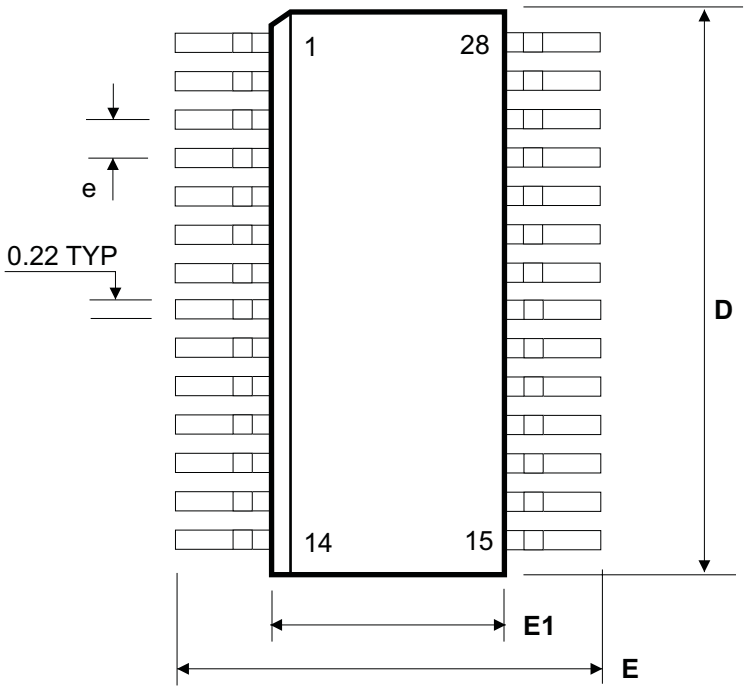
Temp = 0 °C to +70 °C, Vcc = 3.3 – 5.0 V ± 10% unless otherwise specified.

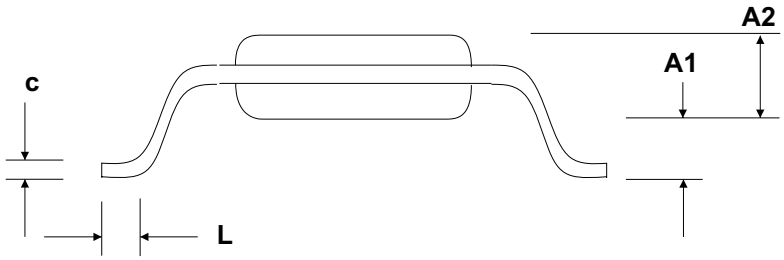
Symbol	Parameter	Min	Max	Unit	Condition
5V	5V Supply	4.5	5.5	V	Voltage Regulator Input
3.3V	Supply Voltage	3.0	3.6	V	
$Vclk_L$	Clock Input (low level)	-0.5	0.6	V	External
Vck_H	Clock Input (high level)	2.4	Vcc	V	External
Vi_L	Input (low level)		1.08	V	CMOS
Vi_H	Input (high level)	2.1		V	CMOS
Vo_L	Output (low level)		0.4	V	Io_L = 6 mA
Vo_H	Output (high level)	1.85		V	Io_H = 6 mA
Ii_L	Input Leakage Current	-10	+10	µA	
Icc	Operating Current	7.5	14	mA	From 3.3V Supply
Icc	Operating Current		22	mA	From 5V Supply
Cp	Input Pin Capacitance	5	7	pF	

AC Electrical Specification

Temp = 0 °C to +70 °C, Vcc = 3.3V ± 10% unless otherwise specified.

Symbol	Parameter	Min	Max	Unit	Condition
F_{CLKA}	USB Clock Frequency	12	12	MHz	±50 PPM





28-Pin SSOP
Package Dimensions

SYMBOL	MILLIMETERS			INCHES		
	MIN	TYP	MAX	MIN	TYP	MAX
A1	0.05		0.21	0.020		0.08
A2	1.65		1.80	0.650		0.708
C			0.25			
e		0.65			0.026	
D	10.00		10.4	3.93		4.09
E	7.4	7.8	8.2			
E1	5.2		5.4	2.05		2.12
L	0.55	0.75	0.95			

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Revision History

Revision	Changes	Date
1.0	Initial Release	Feb-2004
2.0	Updated to new Layout Format	26-May-2006
2.1	Corrected Electrical Specs, Certifications, Pin Descriptions	31-May-2006