

Dual N-Channel 30-V Power MOSFET

GENERAL DESCRIPTION

The LT4936 is the Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

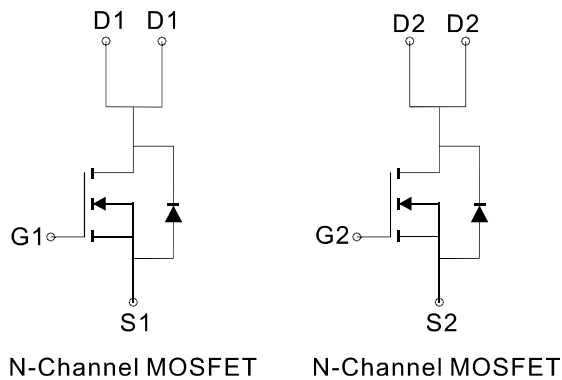
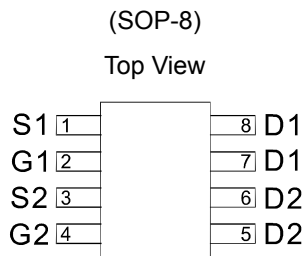
FEATURES

- $R_{DS(ON)} \leq 36m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 45m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management
- DC/DC Converter
- LCD TV & Monitor Display inverter
- CCFL inverter

PIN CONFIGURATION



Absolute Maximum Ratings ($T_A=25^\circ C$ Unless Otherwise Noted)

Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DSS}	30		V
Gate-Source Voltage		V_{GSS}	± 20		V
Continuous Drain Current (T _J =150°C)	$T_A=25^\circ C$	I_D	6.6	5.1	A
	$T_A=70^\circ C$		5.1	4	
Pulsed Drain Current		I_{DM}	30		A
Continuous Source Current (Diode Conduction)		I_S	1.7	0.9	A
Maximum Power Dissipation	$T_A=25^\circ C$	P_D	2.5	1.5	W
	$T_A=70^\circ C$		1.5	0.9	
Operating Junction Temperature		T_J	-55 to 150		°C
Storage Temperature Range		T_{stg}	-55 to 150		°C
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	50	82	°C/W
Thermal Resistance-Junction to Case*		$R_{\theta JC}$	50		°C/W

*The device mounted on 1in² FR4 board with 2 oz copper

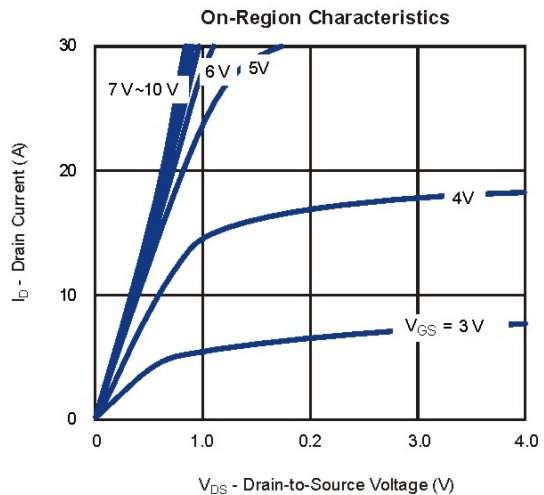
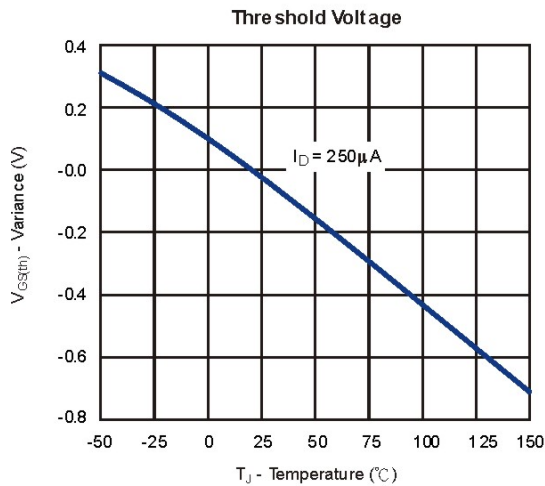
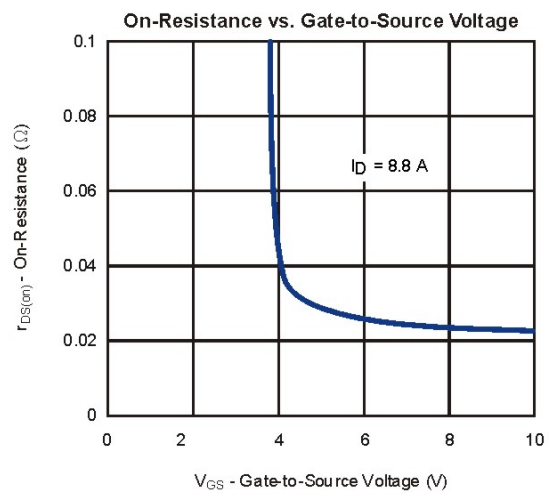
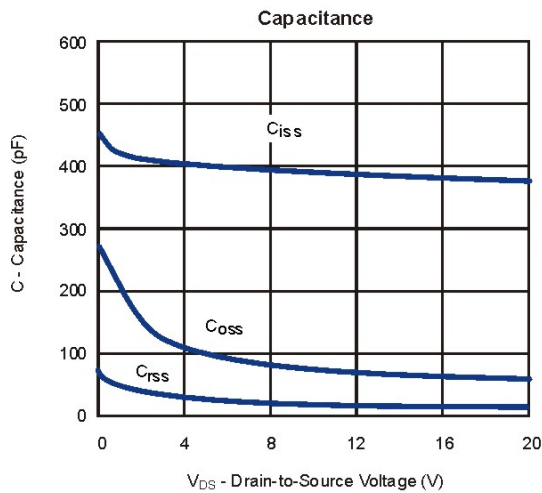
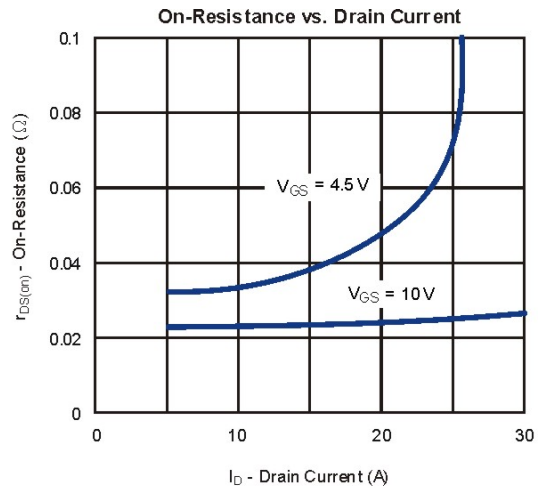
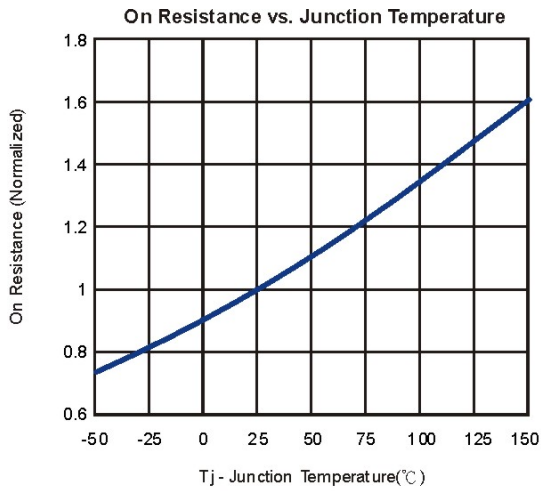
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Electrical Characteristics ($T_A=25^\circ\text{C}$ Unless Otherwise Specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
STATIC						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\ \mu A$	30			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\ \mu A$	1.0	1.4	3.0	V
I_{GSS}	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=30V, V_{GS}=0V$			1	μA
		$V_{DS}=30V, V_{GS}=0V$			5	
		$T_J=55^\circ\text{C}$				
$I_{D(ON)}$	On-State Drain Current ^a	$V_{DS}\geq 5V, V_{GS}=10V$	20			A
$R_{DS(ON)}$	Drain-Source On-Resistance ^a	$V_{GS}=10V, I_D=5.9A$		23	36	m Ω
		$V_{GS}=4.5V, I_D=4.9A$		34	45	
V_{SD}	Diode Forward Voltage	$I_S=1.7A, V_{GS}=0V$		0.8	1.2	V
DYNAMIC						
R_g	Gate resistance	$V_{GS}=0V, V_{DS}=0V, f=1\text{MHz}$		0.8		Ω
C_{iss}	Input capacitance	$V_{DS}=15V, V_{GS}=0V, f=1.0\text{MHz}$		380	450	pF
C_{oss}	Output Capacitance			68		
C_{rss}	Reverse Transfer Capacitance			18		
Q_g	Total Gate Charge	$V_{DS}=15V, V_{GS}=10V, I_D=5.9A$		13	20	nC
Q_{gs}	Gate-Source Charge			3.5		
Q_{gd}	Gate-Drain Charge			3		
$t_{d(on)}$	Turn-On Delay Time	$V_{DD}=15V, R_L=15\ \Omega$ $I_D=1.0A, V_{GEN}=10V$ $R_G=6\ \Omega$		9	12	ns
t_r	Turn-On Rise Time			14	18	
$t_{d(off)}$	Turn-Off Delay Time			32	42	
t_f	Turn-Off Fall time			5	8	

 Notes: a. Pulse test; pulse width $\leq 300\ \mu s$, duty cycle $\leq 2\%$

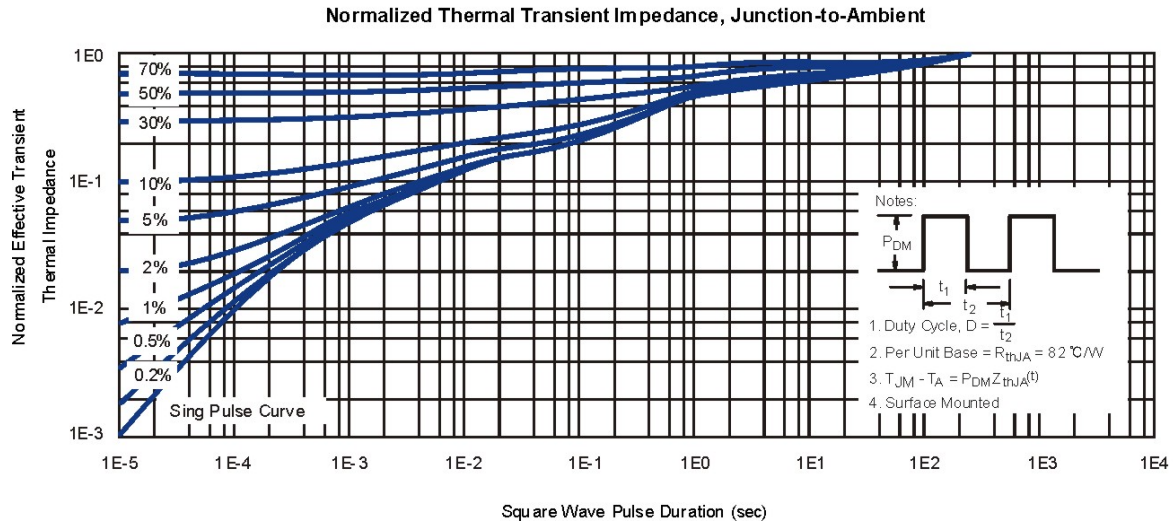
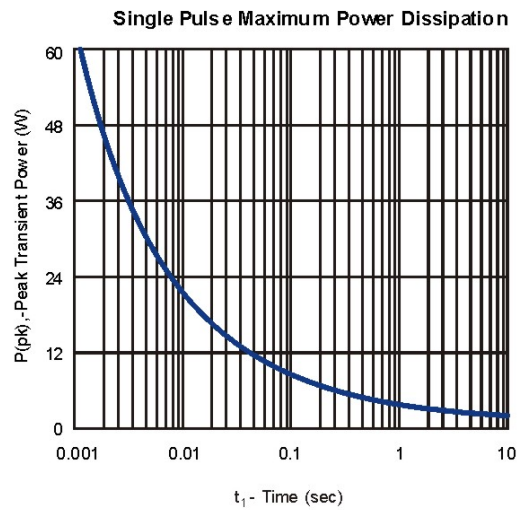
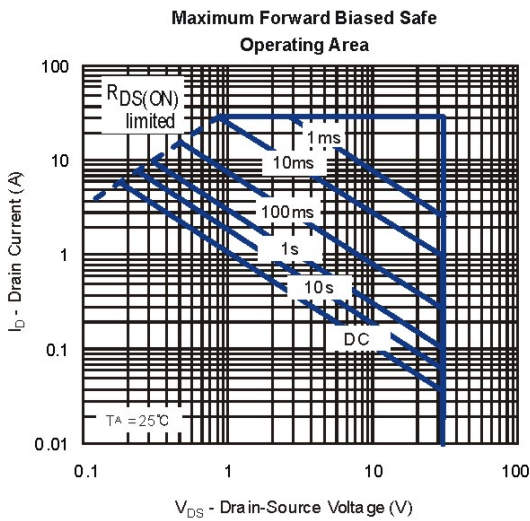
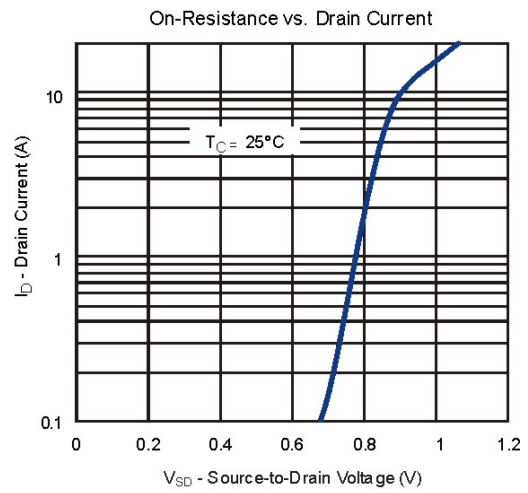
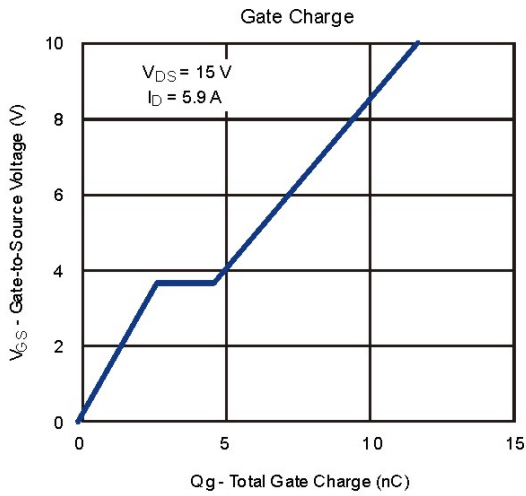
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Typical Characteristics (T_J = 25°C Noted)



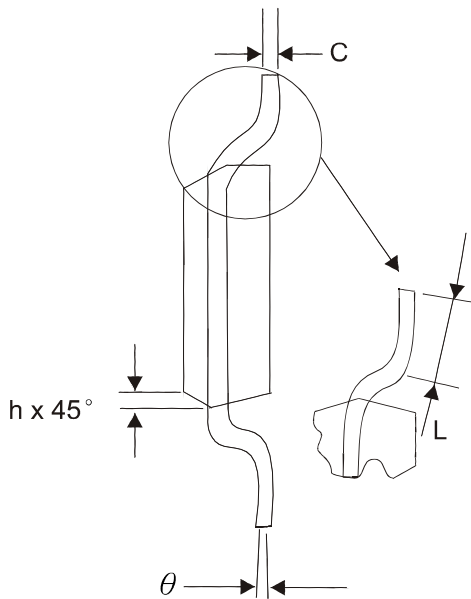
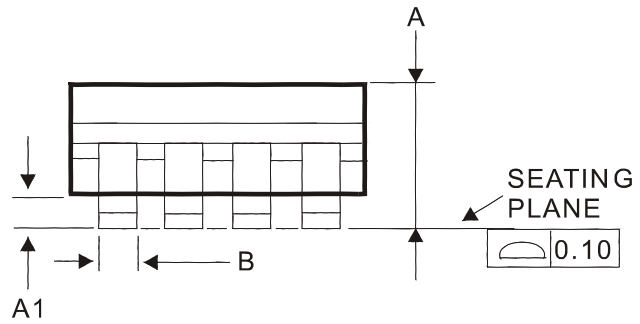
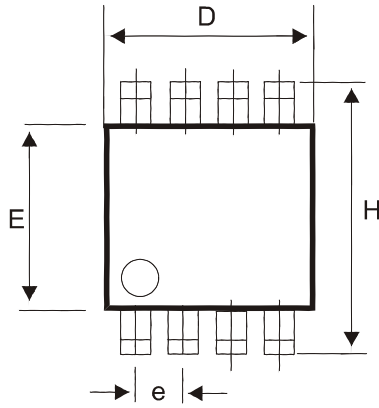
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SOP-8 Package Outline



DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°