Dual N-Channel 30-V Power MOSFET

GENERAL DESCRIPTION

The LT4920C is the N-Channel logic enhancement mode power field effect transistors, using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on state resistance.

These devices are particularly suited for low voltage application such as cellular phone, notebook computer power management and other battery powered circuits, and low in-line power loss that are needed in a very small outline surface mount package.

FEATURES

- 30V/6.9A, $R_{DS(ON)}$=35 mΩ@VGS=10V
- 30V/5.8A, $R_{DS(ON)}$=45 mΩ@VGS=4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

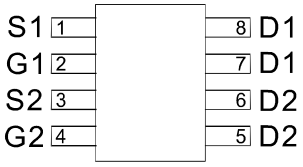
APPLICATIONS

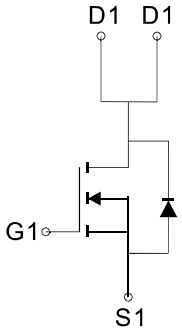
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION

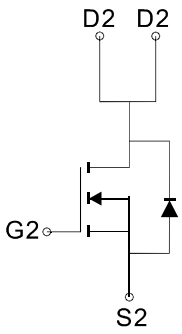
(SOP-8)

Top View





N-Channel MOSFET



N-Channel MOSFET

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Limit		Unit
Drain-Source Voltage		V_{DSS}	30		V
Gate-Source Voltage		V_{GSS}	±20		V
Continuous Drain Current(tJ=150℃)	T_A=25℃	I_D	6.9		A
	T_A=70℃		5.5		
Pulsed Drain Current		I_{DM}	30		A
Continuous Source Current (Diode Conduction)		I_S	1.7		A
Maximum Power Dissipation	T_A=25℃	P_D	2		W
	T_A=70℃		1.3		
Operating Junction Temperature		T_J	-55 to 150		℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	T≦10 sec	50	℃/W
			Steady State	80	
Thermal Resistance-Junction to Case		$R_{\theta JC}$	50		℃/W

The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1	1.4	3	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	μA
		V_{DS}=30V, V_{GS}=0V T_J=55℃			25	
$I_{D(ON)}$	On-State Drain Current[a]	V_{DS}≧5V, V_{GS}=10V	20			A
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=10V, I_D= 6.9A		26	35	mΩ
		V_{GS}=4.5V, I_D= 5.8A		36	45	
G_{FS}	Forward Transconductance	V_{DS}=15V, I_D=6.9A		25		S
V_{SD}	Diode Forward Voltage	I_S=1.7A, V_{GS}=0V		0.75	1.2	V
DYNAMIC[b]						
Qg	Total Gate Charge	V_{DS}=15V, V_{GS}=10V, I_D=6.9A		11.5	15	nC
Qgs	Gate-Source Charge			2.7		
Qgd	Gate-Drain Charge			2.3		
Ciss	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHz		350	450	pF
Coss	Output Capacitance			65		
Crss	Reverse Transfer Capacitance			16		
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=15V, R_L =15Ω I_D=1A, V_{GEN}=10V R_G=6Ω		9	12	ns
tr	Turn-On Rise Time			10	23	
$t_{d(off)}$	Turn-Off Delay Time			32	40	
tf	Turn-Off Fall Time			3.5	5	
t_{rr}	Surce-Drain Reverse Recovery Time	I_F=1.7A, di/dt=100A/μs		50	90	ns

Notes

a. pulse test:pulse width≦ 300us, duty cycle≦ 2%,Guaranteed by design, not subject to production testing.

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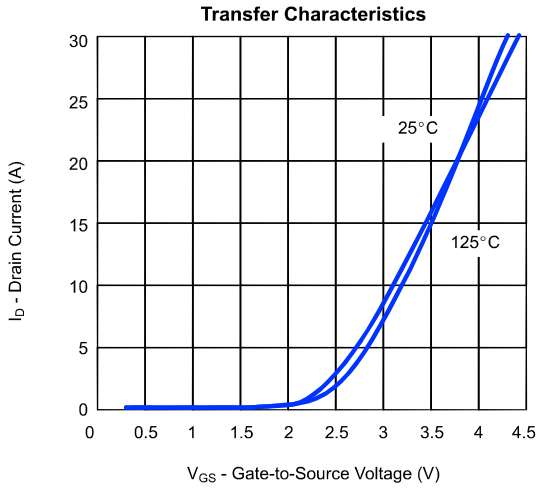
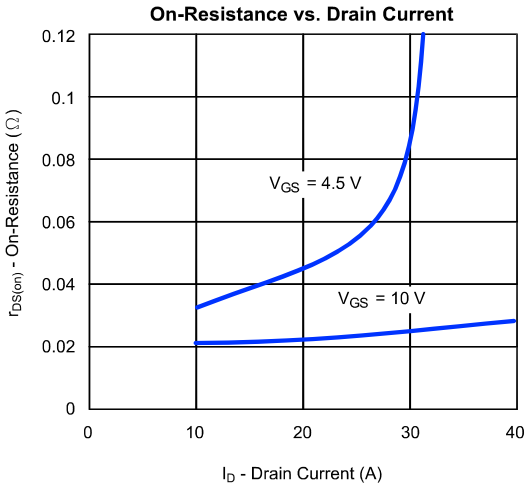
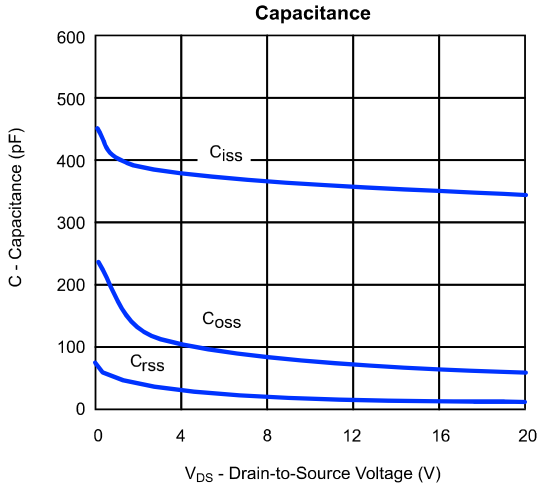
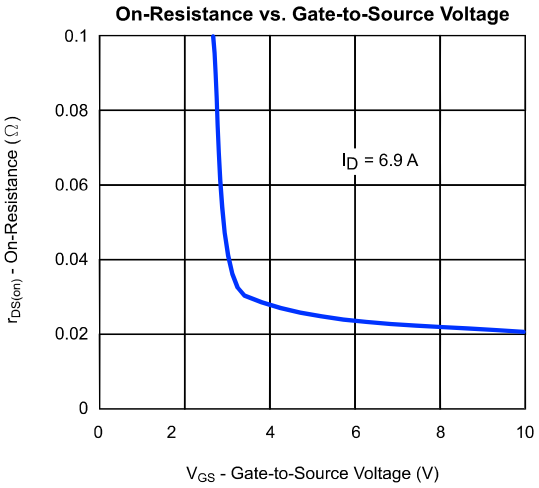
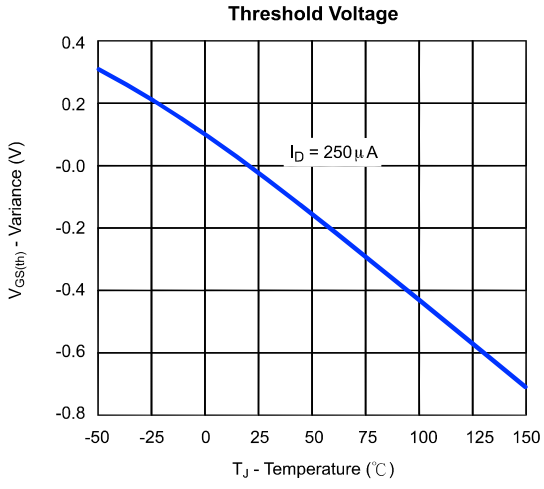
Typical Characteristics (T_J =25℃ Noted)

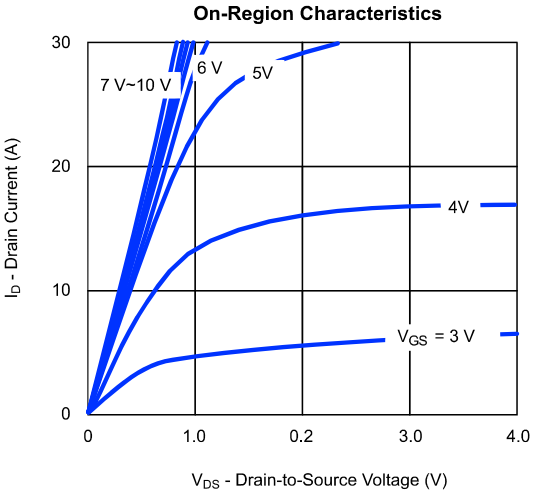












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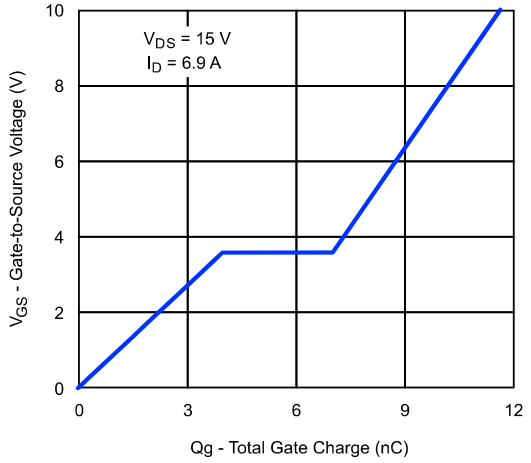
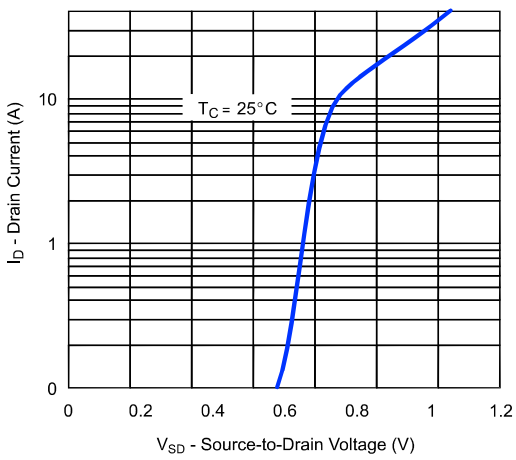
Typical Characteristics (T_J =25℃ Noted)

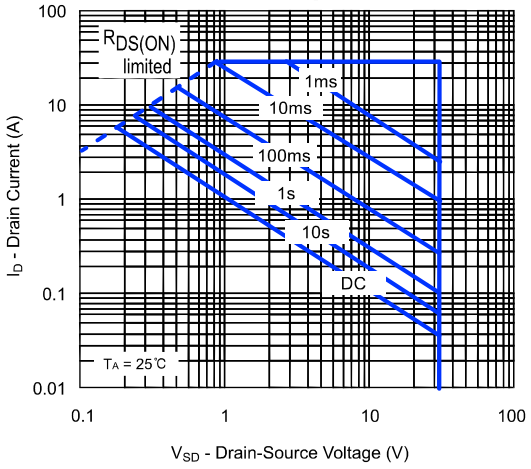
Gate Charge



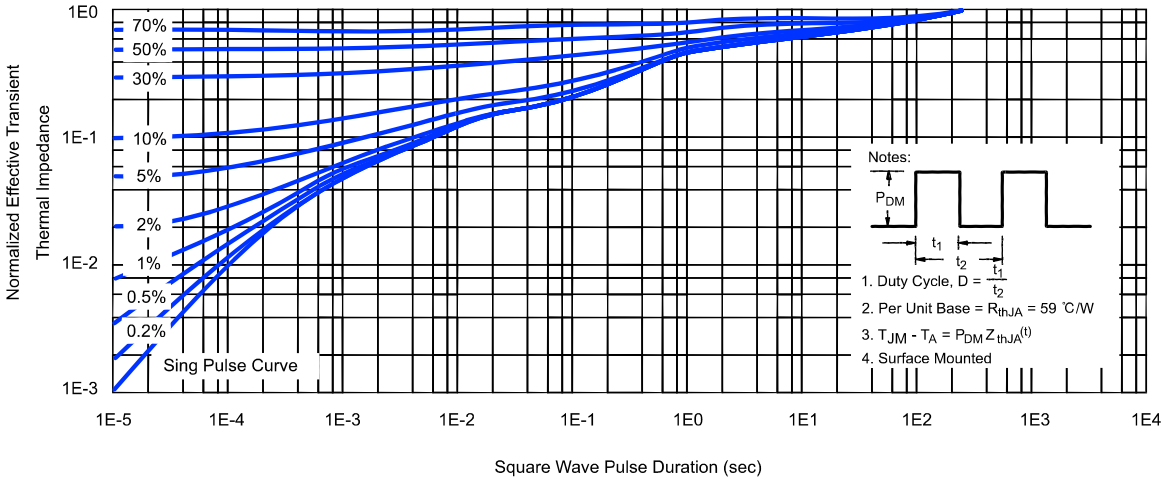
On-Resistance vs. Drain Current



Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



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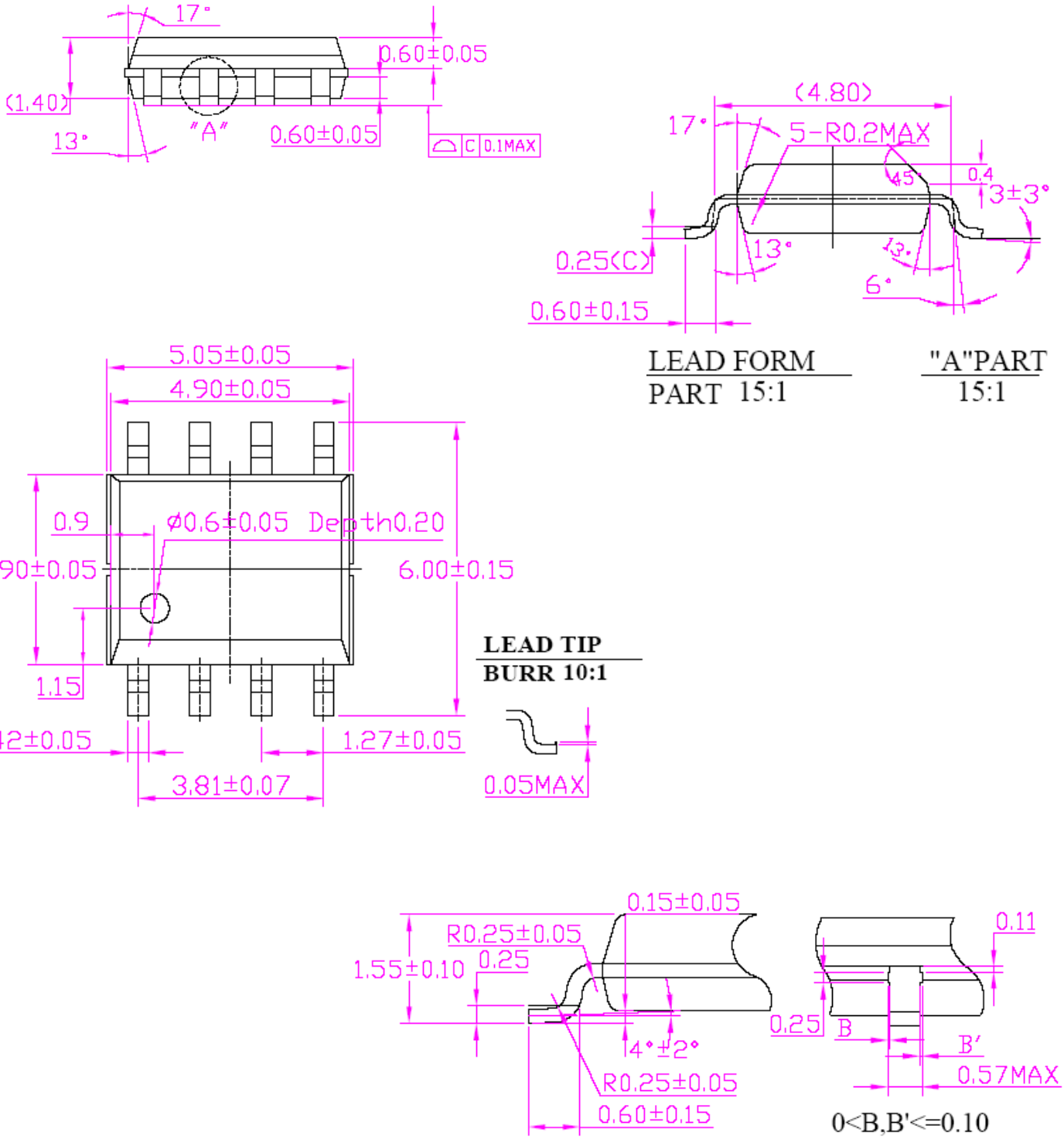
SOP-8 Package Outline



NOTES:

1. PKG ALL SURFACES ARE Ra0.8-1.2um.

2. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total(both sides) .