

**N- and P-Channel 30-V Power MOSFET**

**GENERAL DESCRIPTION**

The LT4542 is the N- and P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

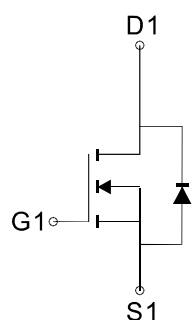
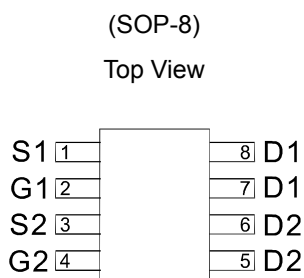
**FEATURES**

- $R_{DS(ON)} \leq 25m\Omega @ V_{GS}=10V$  (N-Ch)
- $R_{DS(ON)} \leq 40m\Omega @ V_{GS}=4.5V$  (N-Ch)
- $R_{DS(ON)} \leq 35m\Omega @ V_{GS}=-10V$  (P-Ch)
- $R_{DS(ON)} \leq 58m\Omega @ V_{GS}=-4.5V$  (P-Ch)
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

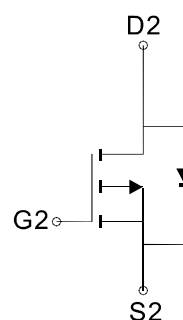
**APPLICATIONS**

- Power Management
- DC/DC Converter
- LCD TV & Monitor Display inverter
- CCFL inverter
- LCD Display inverter

**PIN CONFIGURATION**



N-Channel MOSFET



P-Channel MOSFET

**Absolute Maximum Ratings ( $T_A=25^\circ C$  Unless Otherwise Noted)**

Parameter	Symbol	N-Channel		P-Channel		Unit	
		10 secs	Steady State	10 secs	Steady State		
Drain-Source Voltage	$V_{DSS}$	30		-30		V	
Gate-Source Voltage	$V_{GSS}$	$\pm 20$		$\pm 20$			
Continuous Drain Current ( $t_J=150^\circ C$ )	$I_D$	$T_A=25^\circ C$	8	6.3	-6.9	-5.4	A
		$T_A=70^\circ C$	6.4	5	-5.5	-4.3	
Pulsed Drain Current	$I_{DM}$	30		-30		W	
Maximum Power Dissipation	$P_D$	$T_A=25^\circ C$	2.6	1.6	2.7		1.6
		$T_A=70^\circ C$	1.67	1	1.7	1	
Operating Junction Temperature	$T_J$	-55 to 150				$^\circ C$	
Thermal Resistance-Junction to Ambient *	$R_{\theta JA}$	48	78	46	77	$^\circ C/W$	
Thermal Resistance-Junction to Case *	$R_{\theta JC}$	50		48		$^\circ C/W$	

\*The device mounted on 1in2 FR4 board with 2 oz copper

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**Electrical Characteristics** ( $T_A=25^\circ\text{C}$  Unless Otherwise Specified)

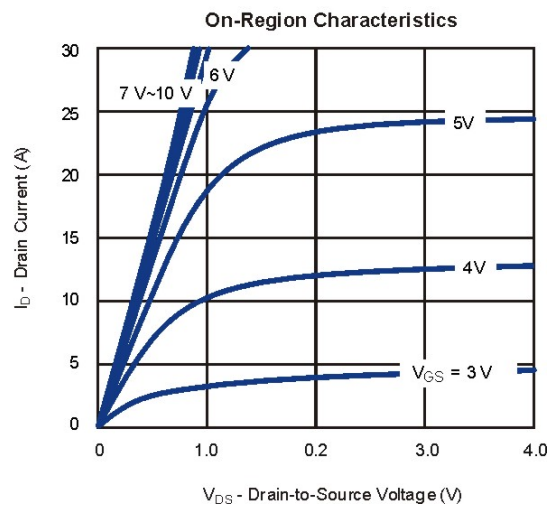
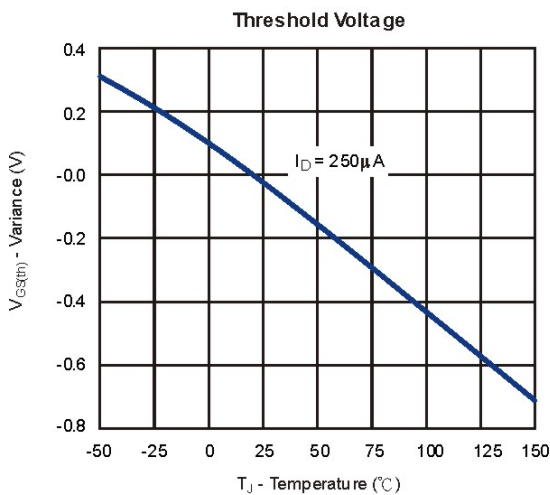
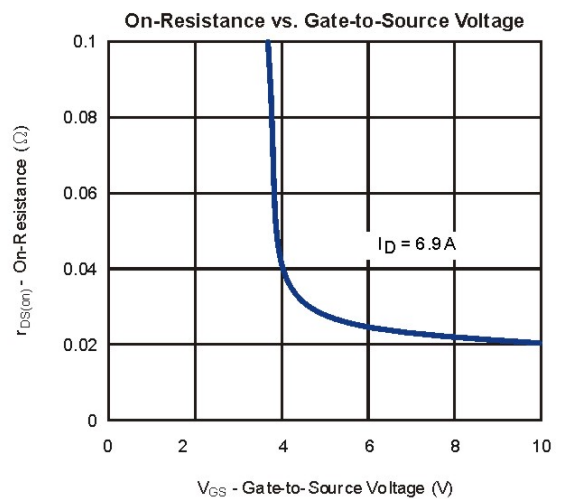
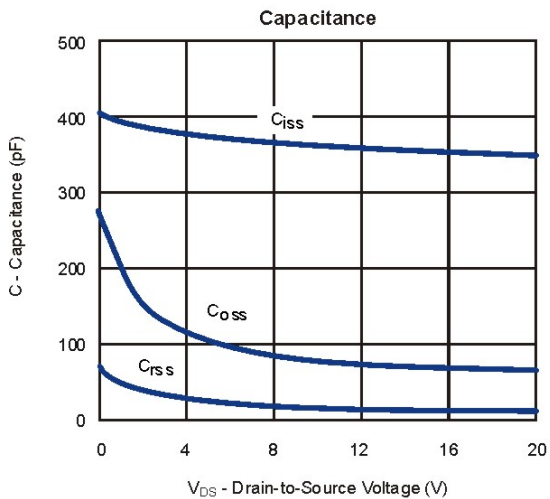
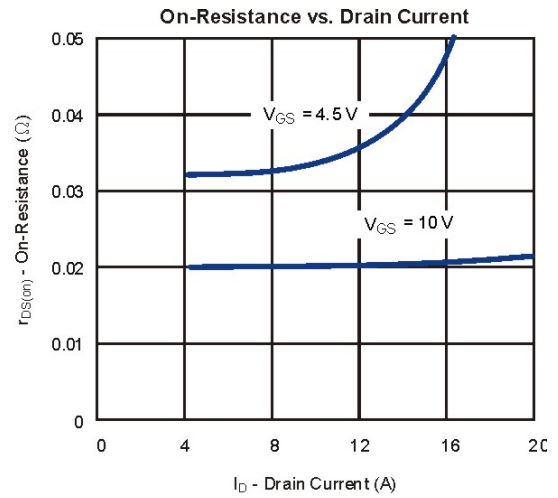
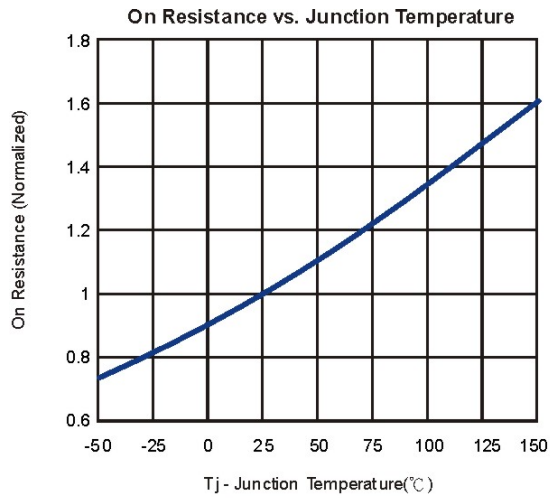
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>STATIC</b>							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\ \mu\text{A}$ $V_{DS}=V_{GS}, I_D=-250\ \mu\text{A}$	N-Ch P-Ch	1.0 -1.0	1.5 -1.5	3.0 -3.0	V
$I_{GSS}$	Gate Leakage Current	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$	N-Ch P-Ch			$\pm 100$ $\pm 100$	nA
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=30\text{V}, V_{GS}=0\text{V}$ $V_{DS}=-30\text{V}, V_{GS}=0\text{V}$	N-Ch P-Ch			1 -1	$\mu\text{A}$
		$V_{DS}=30\text{V}, V_{GS}=0\text{V}, T_J=55^\circ\text{C}$ $V_{DS}=-30\text{V}, V_{GS}=0\text{V}, T_J=55^\circ\text{C}$	N-Ch P-Ch			25 -25	
$I_{D(ON)}$	On-State Drain Current <sup>a</sup>	$V_{DS} \geq 5\text{V}, V_{GS}=10\text{V}$ $V_{DS} \leq -5\text{V}, V_{GS}=-10\text{V}$	N-Ch P-Ch	20 -20			A
$R_{DS(ON)}$	Drain-Source On-State Resistance <sup>a</sup>	$V_{GS}=10\text{V}, I_D=6.7\text{A}$ $V_{GS}=-10\text{V}, I_D=-6.1\text{A}$	N-Ch P-Ch		21 30	25 35	m $\Omega$
		$V_{GS}=4.5\text{V}, I_D=5.0\text{A}$ $V_{GS}=-4.5\text{V}, I_D=-5.0\text{A}$	N-Ch P-Ch		32 48	40 58	
$V_{SD}$	Diode Forward Voltage	$I_S=1.7\text{A}, V_{GS}=0\text{V}$ $I_S=-1.7\text{A}, V_{GS}=0\text{V}$	N-Ch P-Ch		0.8 -0.8	1.2 -1.2	V
<b>DYNAMIC</b>							
$Q_g$	Total Gate Charge	N-Channel $V_{DS}=15\text{V}, V_{GS}=10\text{V}, I_D=6.7\text{A}$ P-Channel $V_{DS}=-15\text{V}, V_{GS}=-10\text{V}, I_D=-6.1\text{A}$	N-Ch P-Ch		12 21	15 25	nC
$Q_{gs}$	Gate-Source Charge		N-Ch P-Ch		2 4		
$Q_{gd}$	Gate-Drain Charge		N-Ch P-Ch		2.5 6		
$C_{iss}$	Input Capacitance	N-Channel $V_{DS}=15\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$ P-Channel $V_{DS}=15\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$	N-Ch P-Ch		360 840	420 980	pF
$C_{oss}$	Output Capacitance		N-Ch P-Ch		70 120		
$C_{rss}$	Reverse Transfer Capacitance		N-Ch P-Ch		17 32		
$R_g$	Gate Resistance	$V_{DS}=0\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$	N-Ch P-Ch		0.5 5.5		$\Omega$
$t_{d(on)}$	Turn-On Delay Time	N-Channel $V_{DD}=15\text{V}, R_L=15\ \Omega$ $I_D=1\text{A}, V_{GEN}=10\text{V}, R_G=6\ \Omega$ P-Channel $V_{DD}=-15\text{V}, R_L=15\ \Omega$ $I_D=-1\text{A}, V_{GEN}=-10\text{V}, R_G=6\ \Omega$	N-Ch P-Ch		9.3 32	13 41	ns
$t_r$	Turn-On Rise Time		N-Ch P-Ch		14 13	18 17	
$t_{d(off)}$	Turn-Off Delay Time		N-Ch P-Ch		32 58	41 75	
$t_f$	Turn-Off Fall Time		N-Ch P-Ch		3.2 6.8	5 9	

 Notes: a. Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$

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**Typical Characteristics (T<sub>J</sub> = 25°C Noted)**

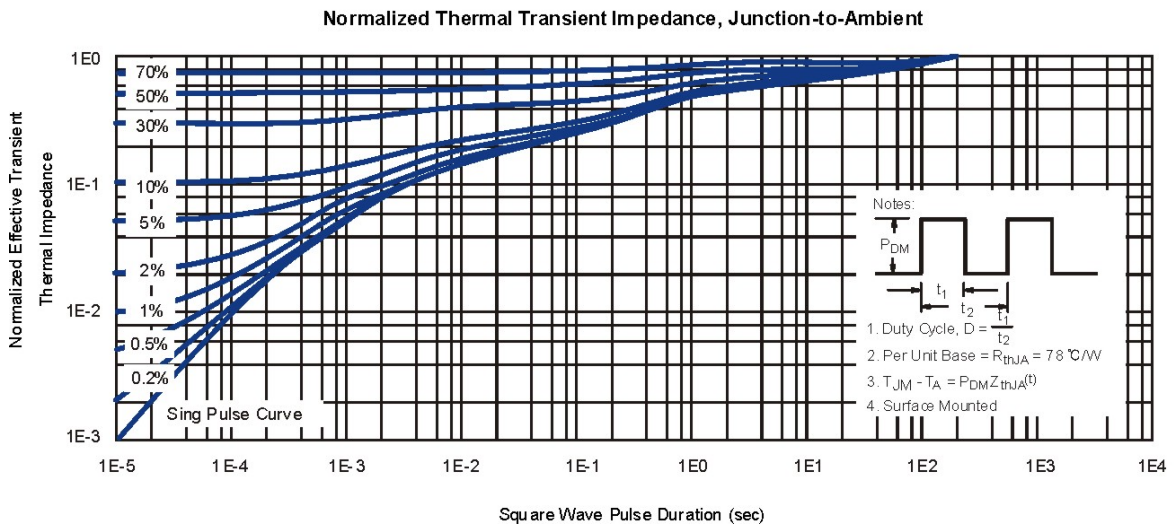
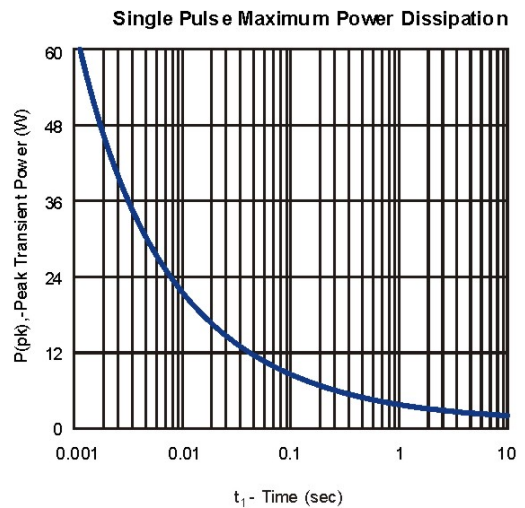
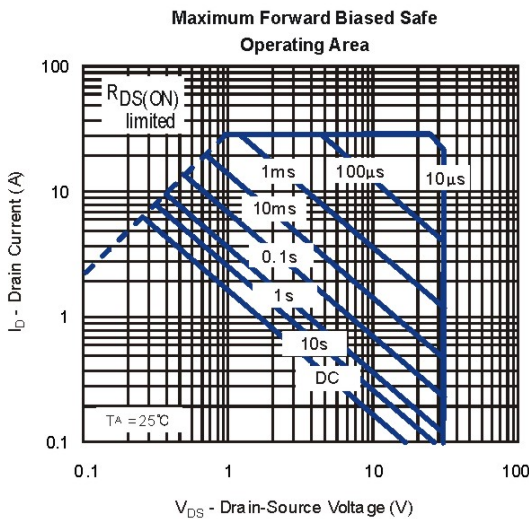
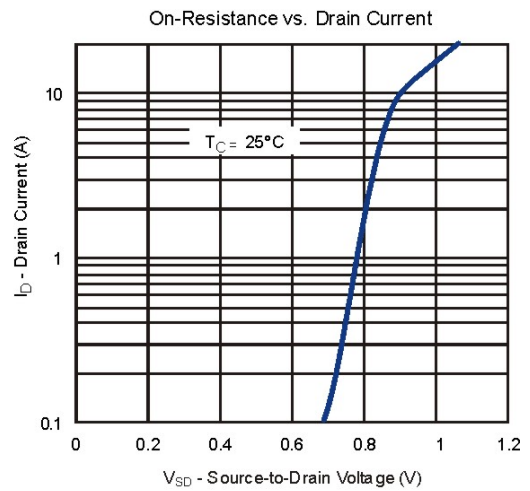
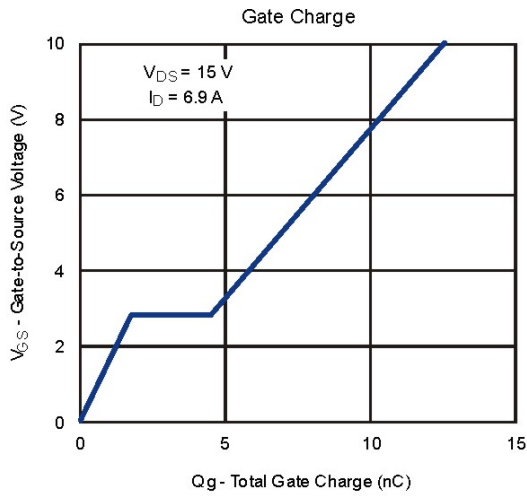
**N-CHANNEL**



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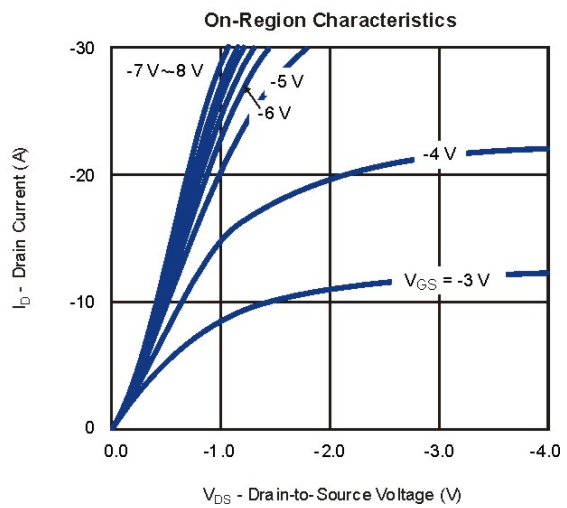
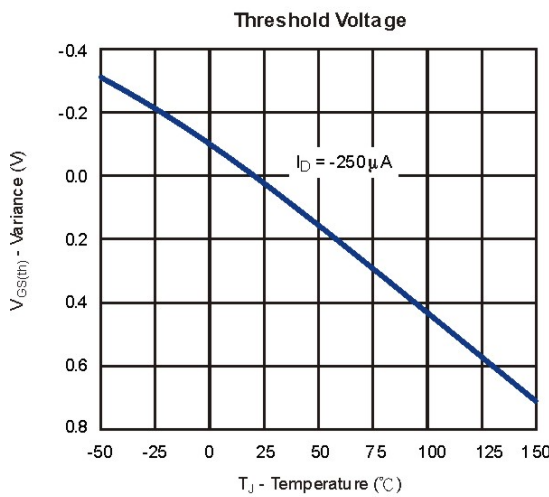
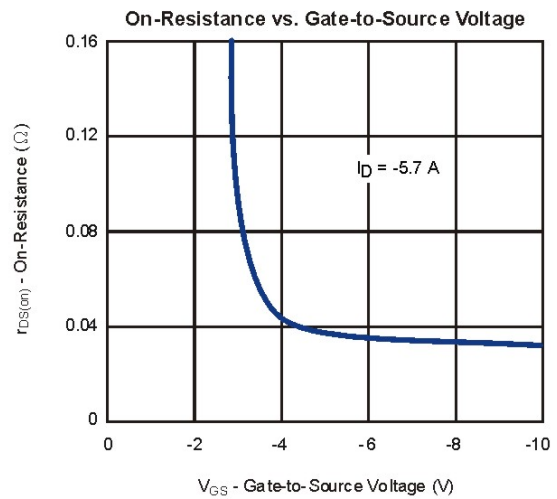
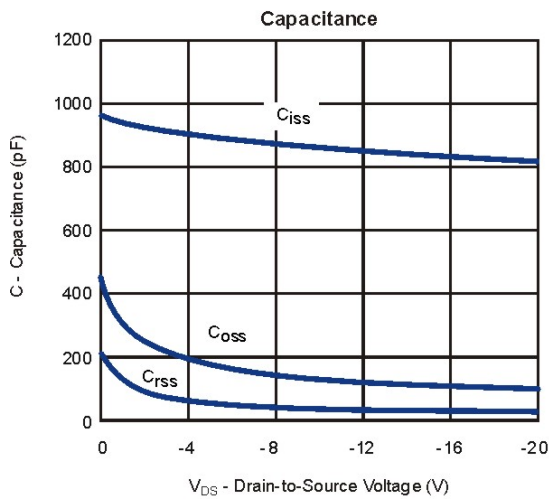
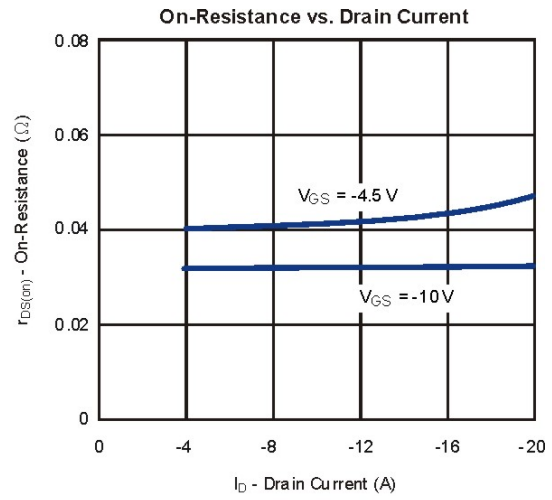
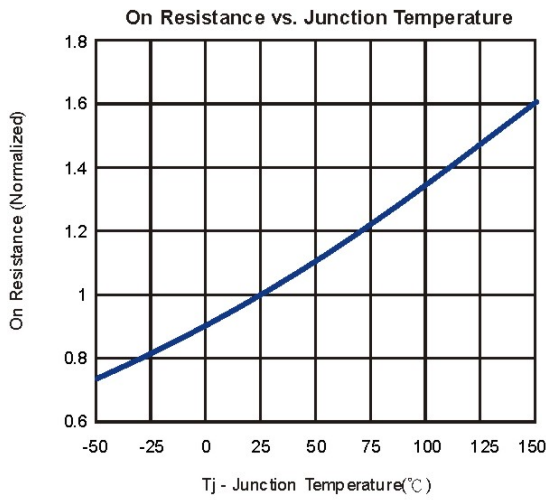
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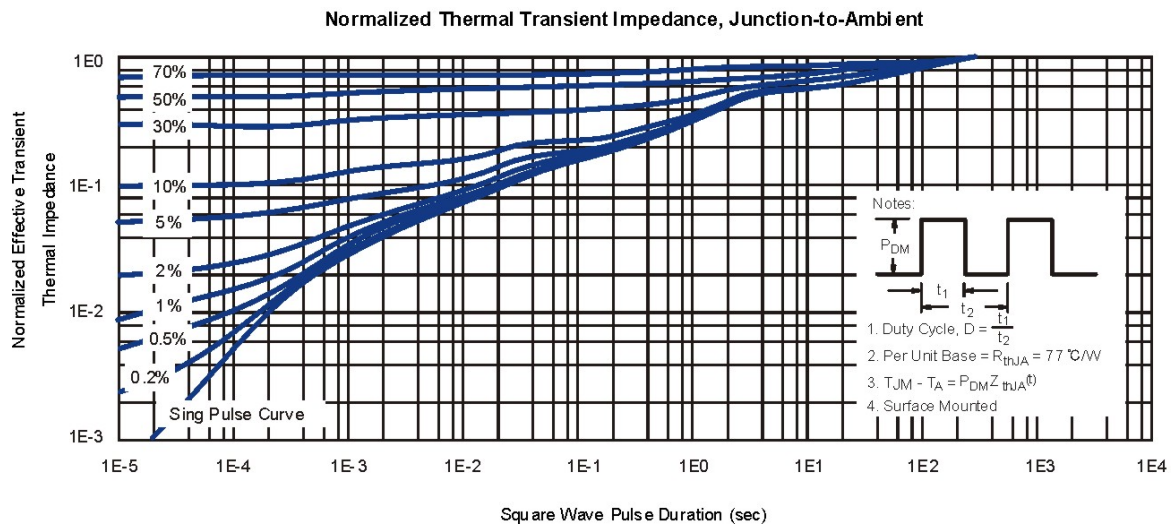
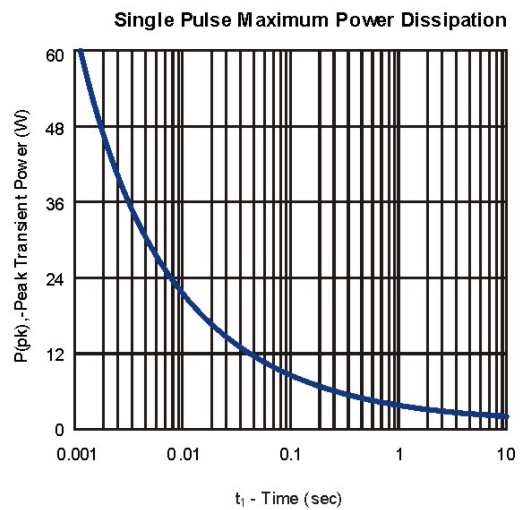
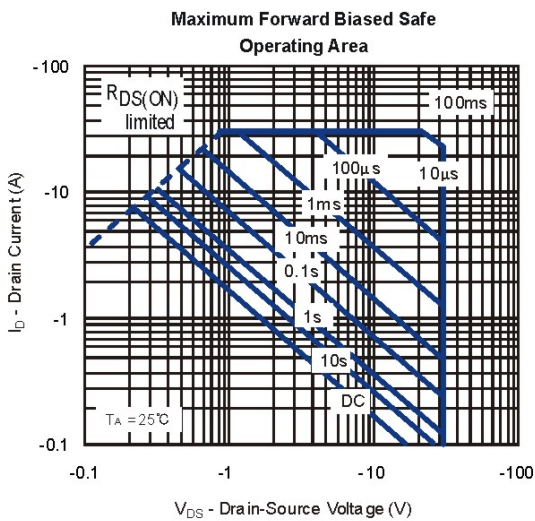
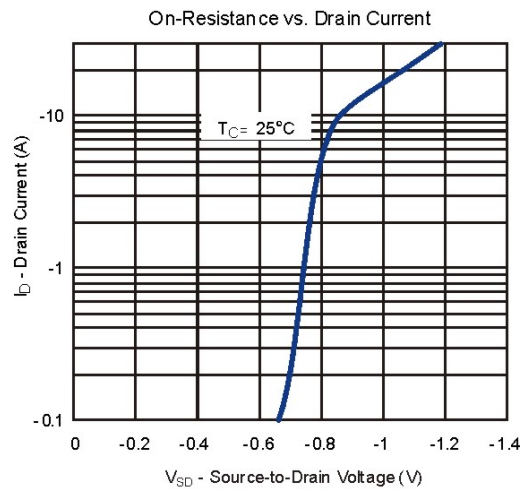
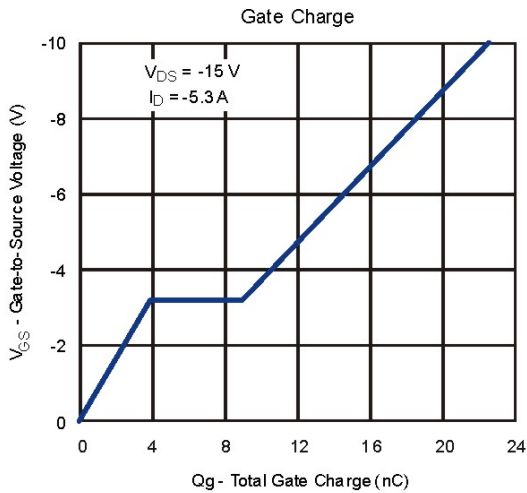
**P-CHANNEL**



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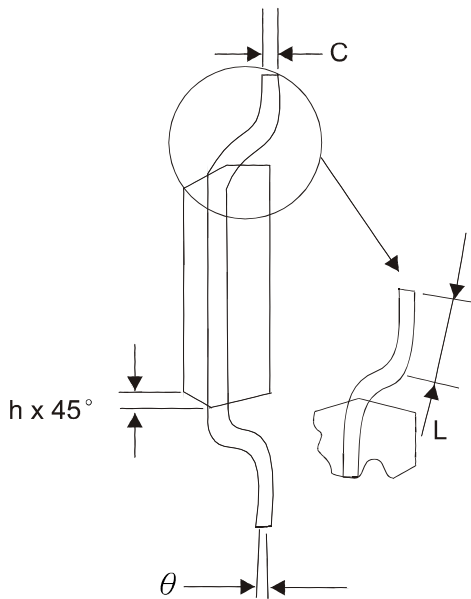
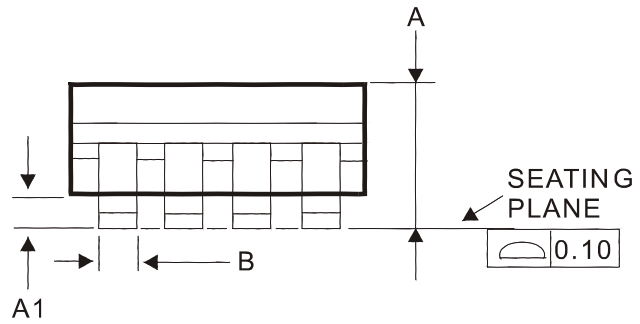
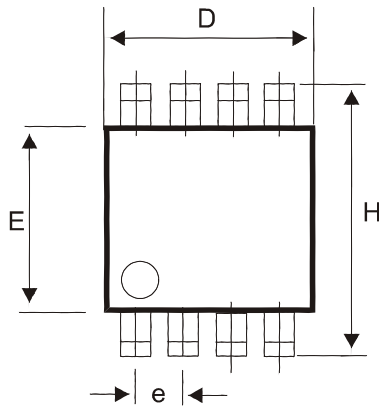
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**P-CHANNEL**



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**SOP-8 Package Outline**



DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°