

N- and P-Channel 30-V Power MOSFET

GENERAL DESCRIPTION

The LT4544C is the N- and P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

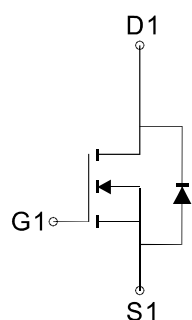
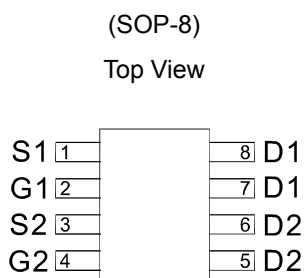
FEATURES

- $R_{DS(ON)} \leq 28m\Omega @ V_{GS}=10V$ (N-Ch)
- $R_{DS(ON)} \leq 42m\Omega @ V_{GS}=4.5V$ (N-Ch)
- $R_{DS(ON)} \leq 60m\Omega @ V_{GS}=-10V$ (P-Ch)
- $R_{DS(ON)} \leq 90m\Omega @ V_{GS}=-4.5V$ (P-Ch)
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

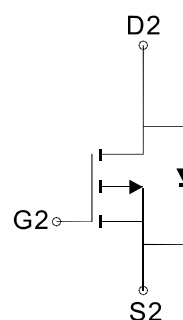
APPLICATIONS

- Power Management
- DC/DC Converter
- LCD TV & Monitor Display inverter
- CCFL inverter
- LCD Display inverter

PIN CONFIGURATION



N-Channel MOSFET



P-Channel MOSFET

Absolute Maximum Ratings ($T_A=25^\circ C$ Unless Otherwise Noted)

Parameter	Symbol	N-Channel		P-Channel		Unit	
		10 secs	Steady State	10 secs	Steady State		
Drain-Source Voltage	V_{DSS}	30		-30		V	
Gate-Source Voltage	V_{GSS}	± 20		± 20			
Continuous Drain Current ($T_J=150^\circ C$)	I_D	$T_A=25^\circ C$	7.6	6	-5.1	-4	A
		$T_A=70^\circ C$	6.1	4.8	-4	-3.2	
Pulsed Drain Current	I_{DM}	30		-30		W	
Maximum Power Dissipation	P_D	$T_A=25^\circ C$	2.6	1.6	2.5		1.5
		$T_A=70^\circ C$	1.67	1	1.6	0.99	
Operating Junction Temperature	T_J	-55 to 150				$^\circ C$	
Thermal Resistance-Junction to Ambient *	$R_{\theta JA}$	48	78	50	81	$^\circ C/W$	
Thermal Resistance-Junction to Case *	$R_{\theta JC}$	50		52		$^\circ C/W$	

*The device mounted on 1in2 FR4 board with 2 oz copper

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Electrical Characteristics ($T_A=25^\circ\text{C}$ Unless Otherwise Specified)

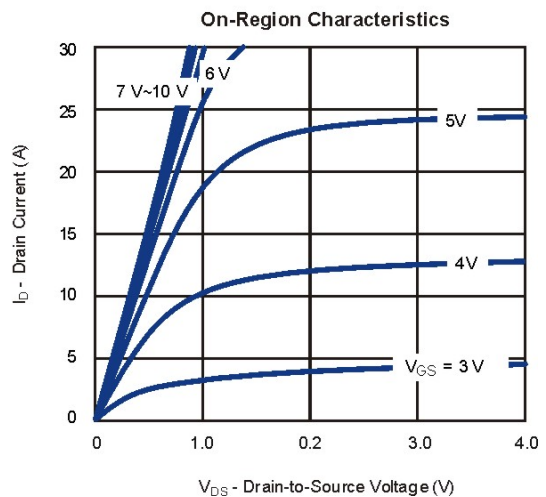
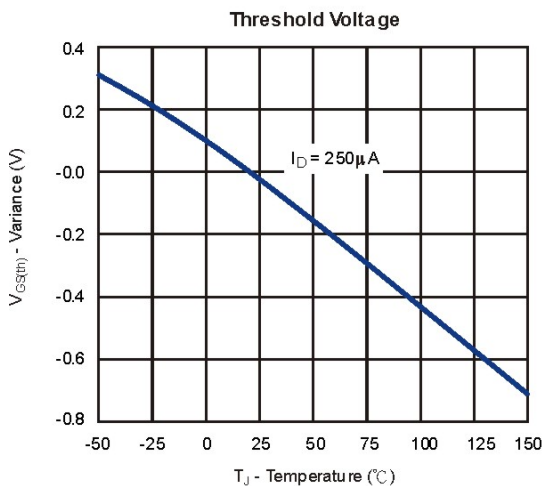
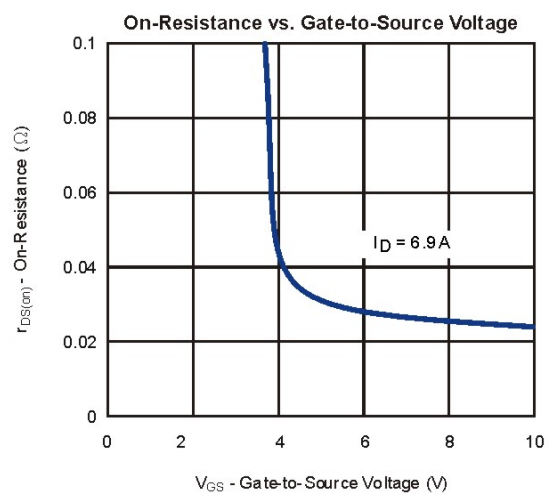
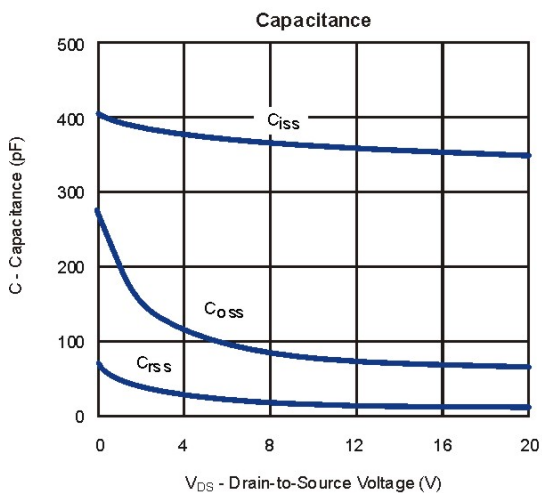
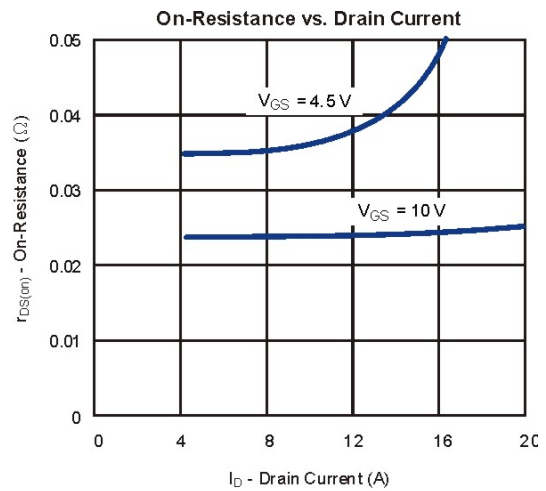
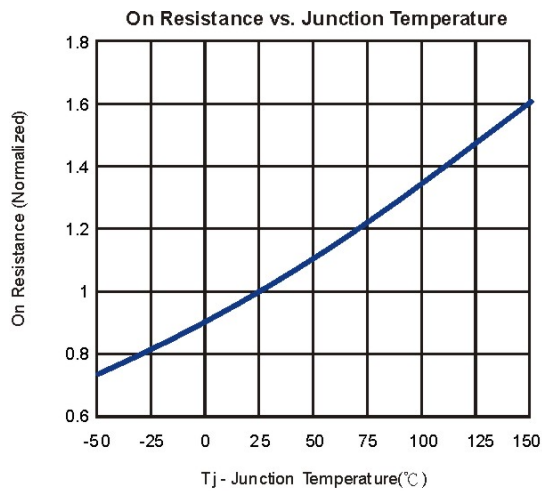
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
STATIC							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\ \mu\text{A}$ $V_{DS}=V_{GS}, I_D=-250\ \mu\text{A}$	N-Ch P-Ch	1.0 -1.0	1.5 -1.5	3.0 -3.0	V
I_{GSS}	Gate Leakage Current	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$	N-Ch P-Ch			± 100 ± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=30\text{V}, V_{GS}=0\text{V}$ $V_{DS}=-30\text{V}, V_{GS}=0\text{V}$	N-Ch P-Ch			1 -1	μA
		$V_{DS}=30\text{V}, V_{GS}=0\text{V}, T_J=55^\circ\text{C}$ $V_{DS}=-30\text{V}, V_{GS}=0\text{V}, T_J=55^\circ\text{C}$	N-Ch P-Ch			25 -25	
$I_{D(ON)}$	On-State Drain Current ^a	$V_{DS} \geq 5\text{V}, V_{GS}=10\text{V}$ $V_{DS} \leq -5\text{V}, V_{GS}=-10\text{V}$	N-Ch P-Ch	20 -20			A
$R_{DS(ON)}$	Drain-Source On-State Resistance ^a	$V_{GS}=10\text{V}, I_D=6.9\text{A}$ $V_{GS}=-10\text{V}, I_D=-6.1\text{A}$	N-Ch P-Ch		22 52	28 60	m Ω
		$V_{GS}=4.5\text{V}, I_D=5.8\text{A}$ $V_{GS}=-4.5\text{V}, I_D=-5.1\text{A}$	N-Ch P-Ch		33 69	42 90	
V_{SD}	Diode Forward Voltage	$I_S=1.7\text{A}, V_{GS}=0\text{V}$ $I_S=-1.7\text{A}, V_{GS}=0\text{V}$	N-Ch P-Ch		0.8 -0.8	1.2 -1.2	V
DYNAMIC							
Q_g	Total Gate Charge	N-Channel $V_{DS}=15\text{V}, V_{GS}=10\text{V}, I_D=6.9\text{A}$ P-Channel $V_{DS}=-15\text{V}, V_{GS}=-10\text{V}, I_D=-6.1\text{A}$	N-Ch P-Ch		12 14	15 17	nC
Q_{gs}	Gate-Source Charge		N-Ch P-Ch		2 4		
Q_{gd}	Gate-Drain Charge		N-Ch P-Ch		2.5 3		
C_{iss}	Input Capacitance	N-Channel $V_{DS}=15\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$ P-Channel $V_{DS}=15\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$	N-Ch P-Ch		360 450	420 490	pF
C_{oss}	Output Capacitance		N-Ch P-Ch		70 70		
C_{rss}	Reverse Transfer Capacitance		N-Ch P-Ch		17 20		
R_g	Gate Resistance	$V_{DS}=0\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$	N-Ch P-Ch		0.5 3.5		Ω
$t_{d(on)}$	Turn-On Delay Time	N-Channel $V_{DD}=15\text{V}, R_L=15\ \Omega$ $I_D=1\text{A}, V_{GEN}=10\text{V}, R_G=6\ \Omega$ P-Channel $V_{DD}=-15\text{V}, R_L=15\ \Omega$ $I_D=-1\text{A}, V_{GEN}=-10\text{V}, R_G=6\ \Omega$	N-Ch P-Ch		9.3 27	13 33	ns
t_r	Turn-On Rise Time		N-Ch P-Ch		14 11	18 15	
$t_{d(off)}$	Turn-Off Delay Time		N-Ch P-Ch		32 40	41 52	
t_f	Turn-Off Fall Time		N-Ch P-Ch		3.2 4	5 6	

 Notes: a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$

N- and P-Channel 30-V Power MOSFET

Typical Characteristics (T_J = 25°C Noted)

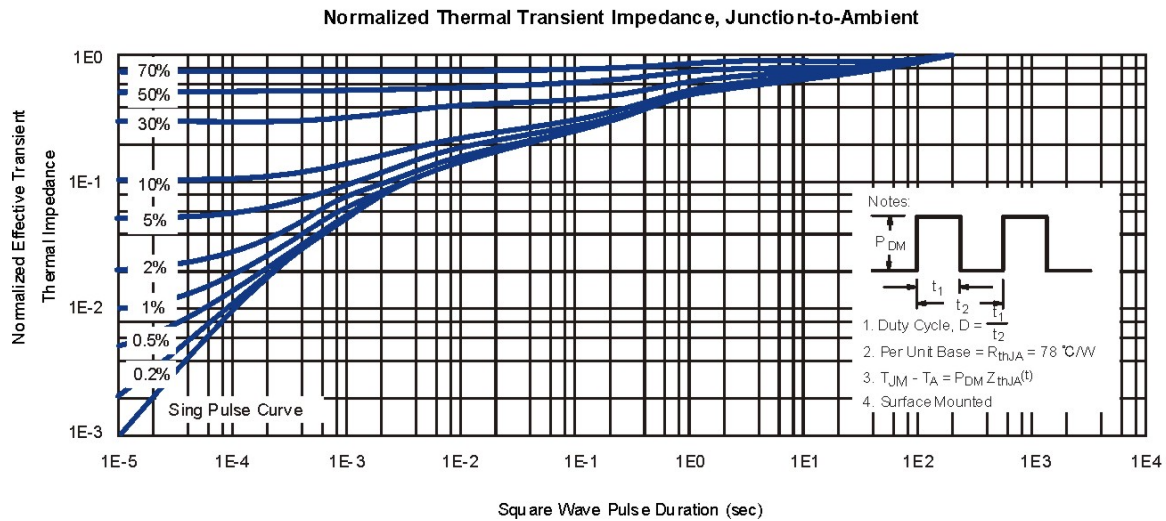
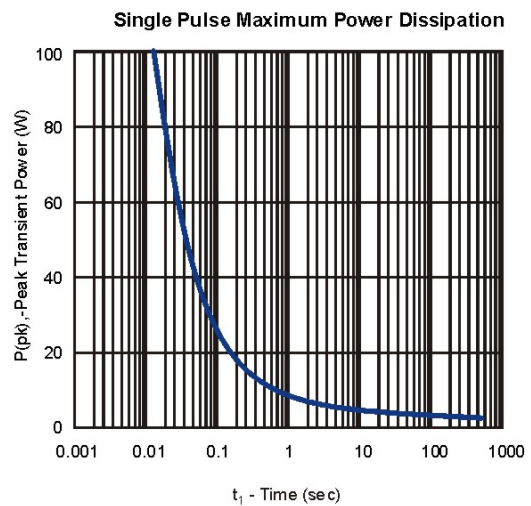
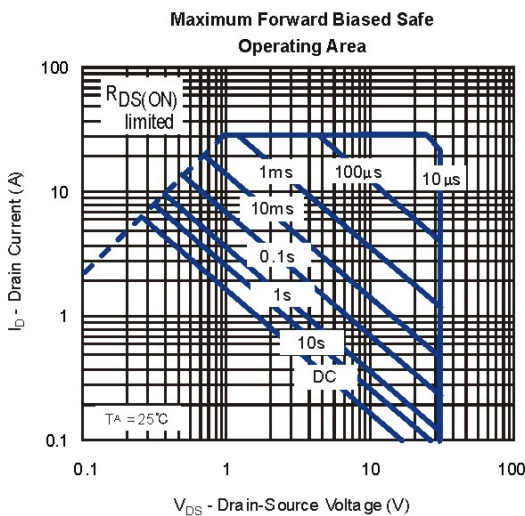
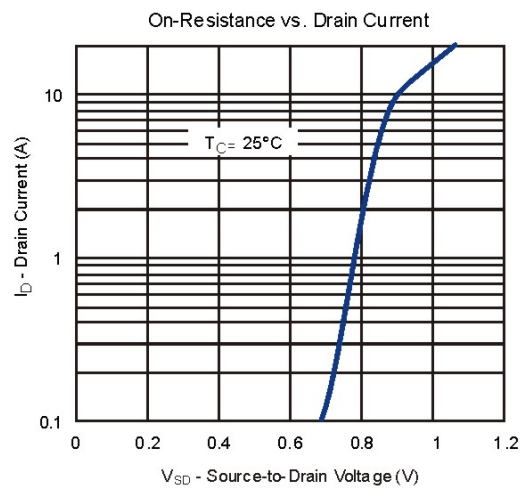
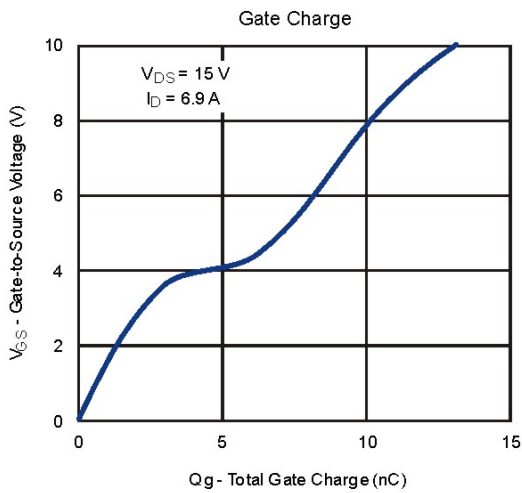
N-CHANNEL



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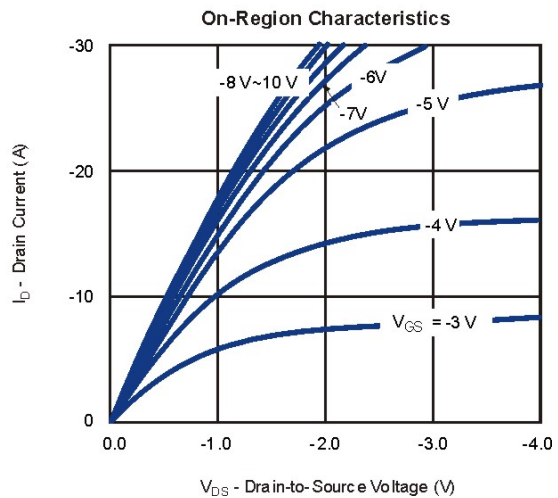
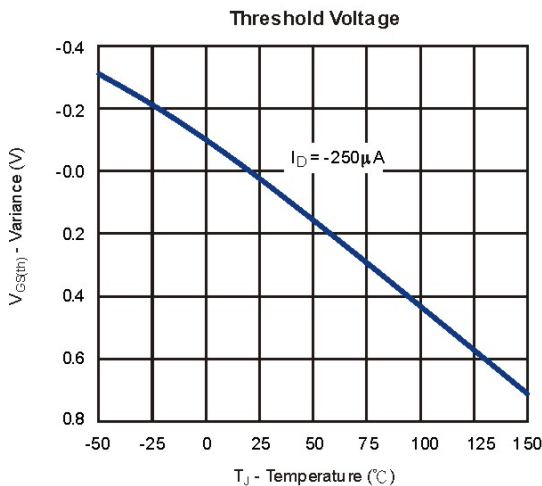
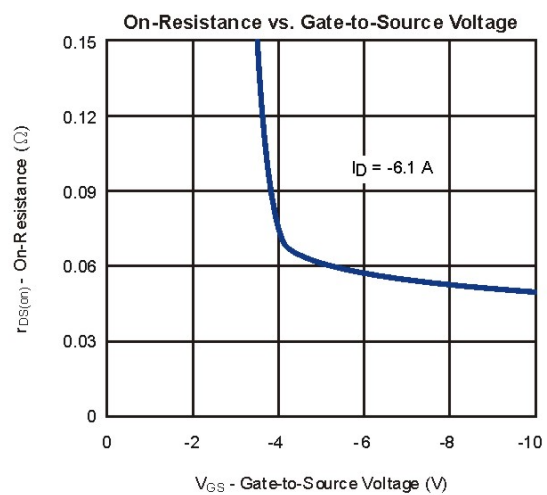
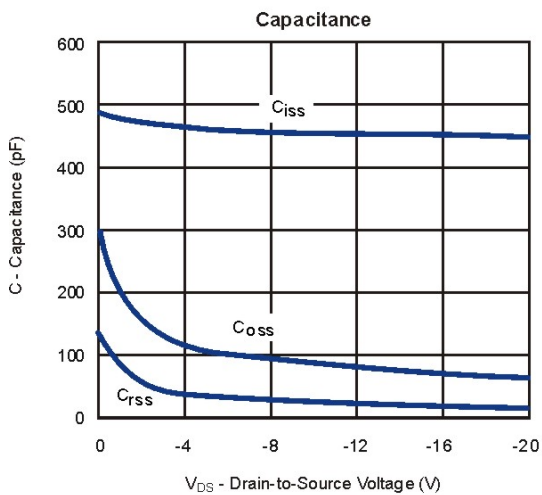
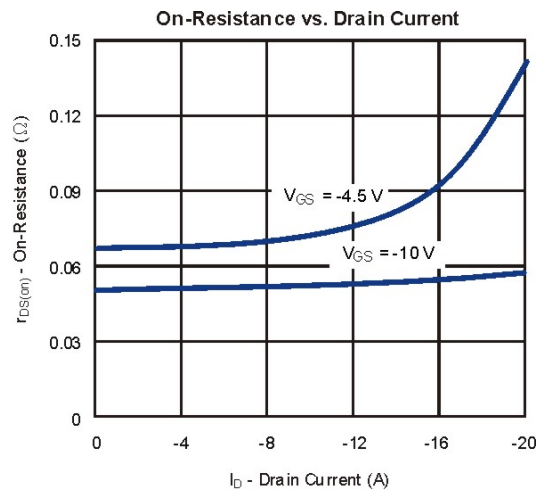
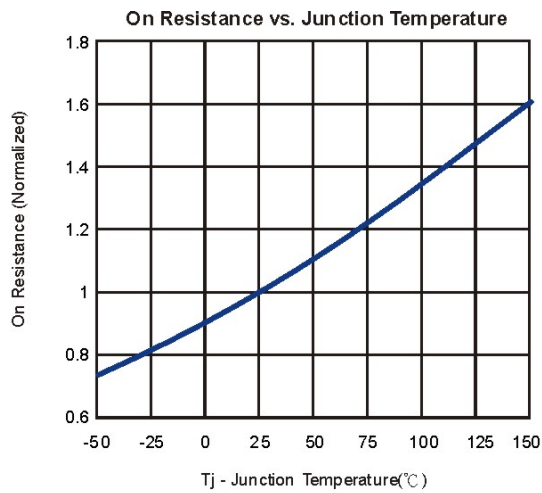
N-CHANNEL



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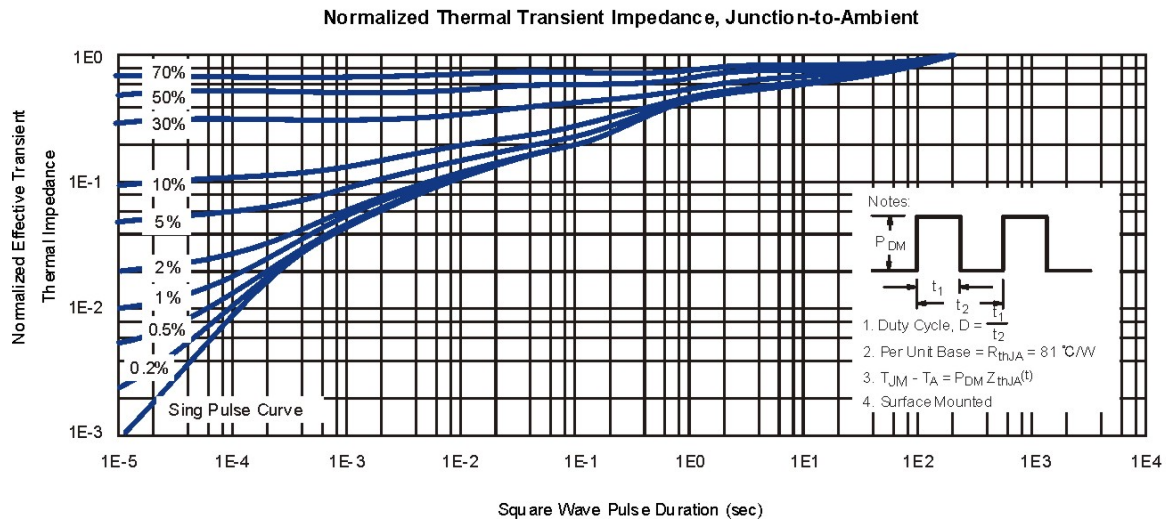
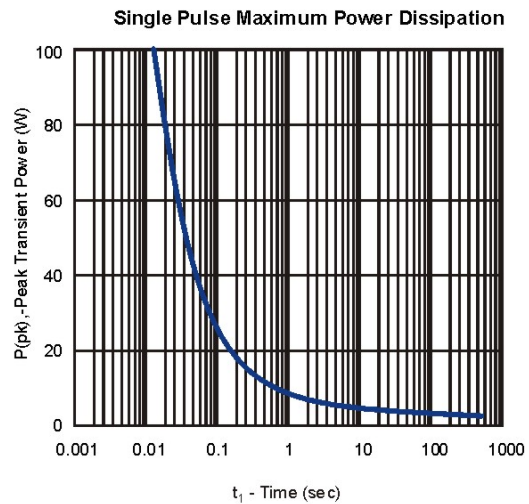
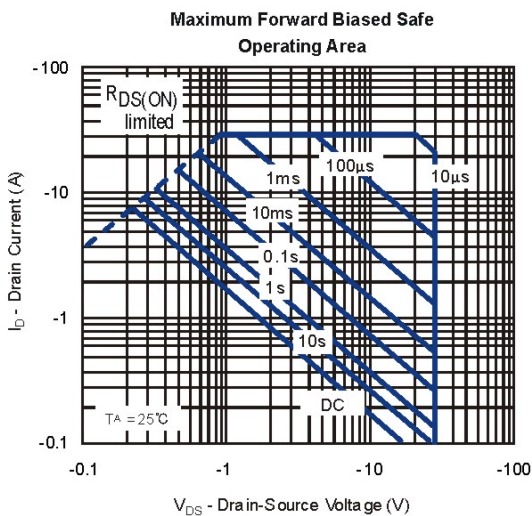
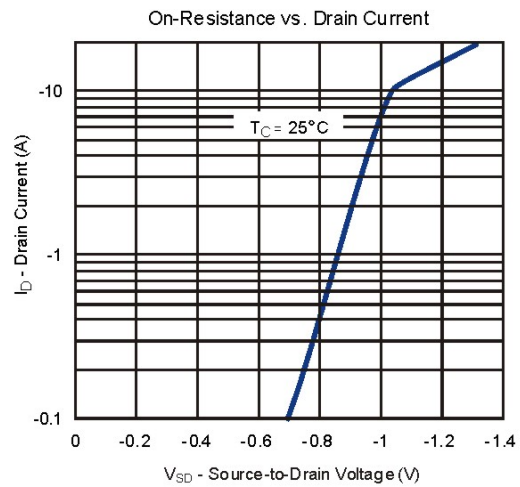
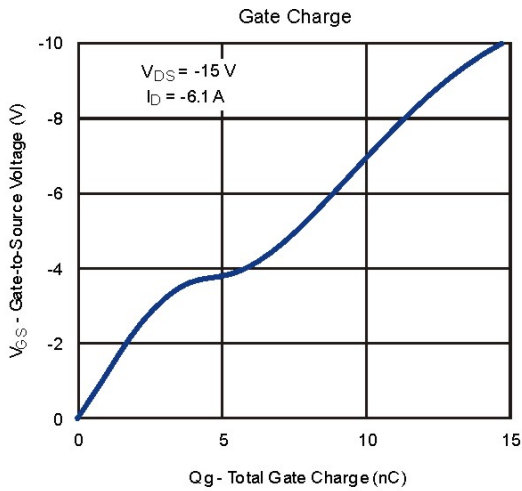
P-CHANNEL



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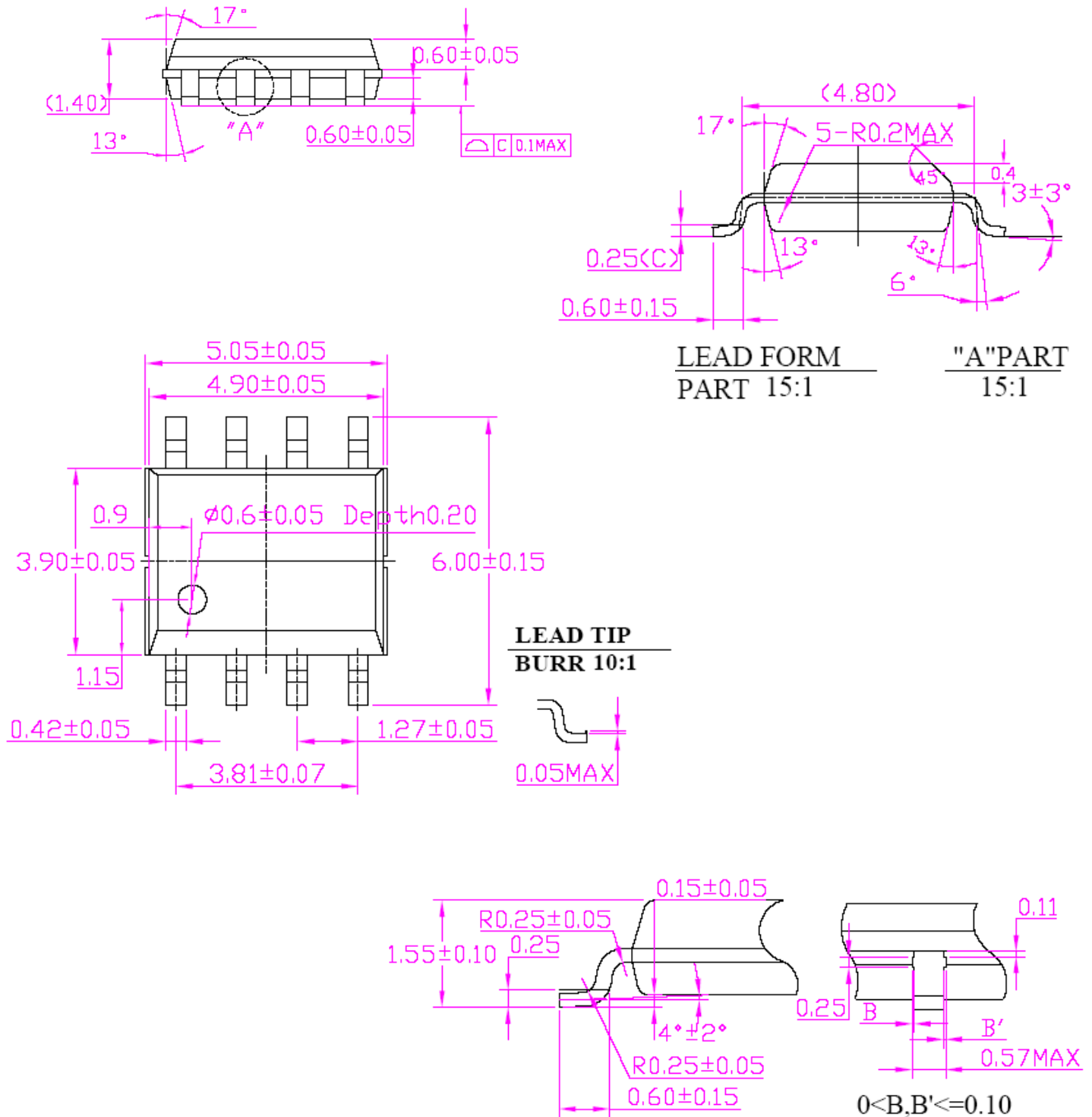
Typical Characteristics (T_J = 25°C Noted)

P-CHANNEL



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SOP-8 Package Outline



NOTES:

1. PKG ALL SURFACES ARE Ra0.8-1.2um.
2. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm in total(both sides) .