UNRF1AF

Silicon PNP epitaxial planar type

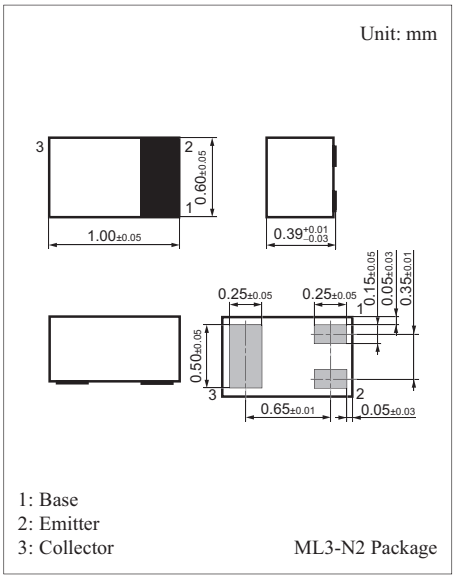
For digital circuits

■ Features

- Optimum for high-density mounting and downsizing of the equipment for Ultraminiature leadless package 0.6 mm × 1.0 mm (height 0.39 mm)

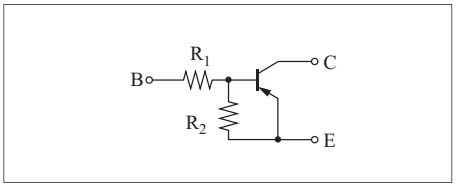
■ Absolute Maximum Ratings $T_a = 25°C$

Parameter	Symbol	Rating	Unit
Collector-base voltage (Emitter open)	V_{CBO}	–50	V
Collector-emitter voltage (Base open)	V_{CEO}	–50	V
Collector current	I_C	–80	mA
Total power dissipation	P_T	100	mW
Junction temperature	T_j	125	°C
Storage temperature	T_{stg}	–55 to +125	°C



Marking Symbol: 4K

Internal Connection

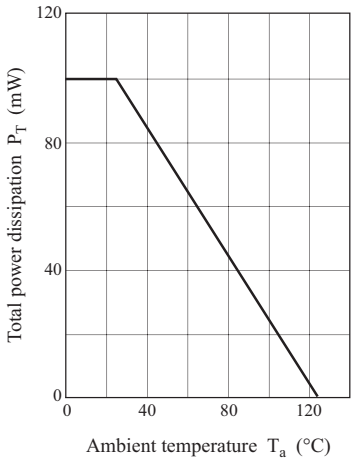


■ Electrical Characteristics $T_a = 25°C \pm 3°C$

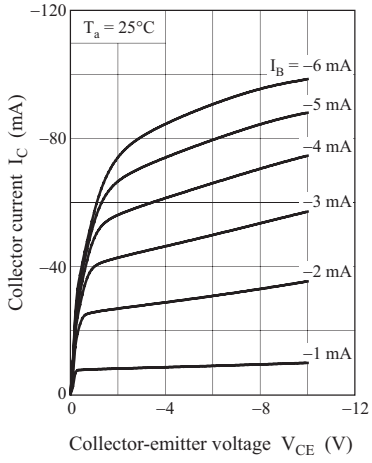
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Collector-base voltage (Emitter open)	V_{CBO}	$I_C = -10$ µA, $I_E = 0$	–50			V
Collector-emitter voltage (Base open)	V_{CEO}	$I_C = -2$ mA, $I_B = 0$	–50			V
Collector-base cutoff current (Emitter open)	I_{CBO}	$V_{CB} = -50$ V, $I_E = 0$			– 0.1	µA
Collector-emitter cutoff current (Base open)	I_{CEO}	$V_{CE} = -50$ V, $I_B = 0$			– 0.5	µA
Emitter-base cutoff current (Collector open)	I_{EBO}	$V_{EB} = -6$ V, $I_C = 0$			–1.0	mA
Forward current transfer ratio	h_{FE}	$V_{CE} = -10$ V, $I_C = -5$ mA	30			—
Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_C = -10$ mA, $I_B = -0.3$ mA			– 0.25	V
Output voltage high-level	V_{OH}	$V_{CC} = -5$ V, $V_B = -0.5$ V, $R_L = 1$ kΩ	–4.9			V
Output voltage low-level	V_{OL}	$V_{CC} = -5$ V, $V_B = -2.5$ V, $R_L = 1$ kΩ			– 0.2	V
Input resistance	R_1		–30%	4.7	+30%	kΩ
Resistance ratio	R_1 / R_2		0.37	0.47	0.57	—
Transition frequency	f_T	$V_{CB} = -10$ V, $I_E = 1$ mA, $f = 200$ MHz		80		MHz

Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

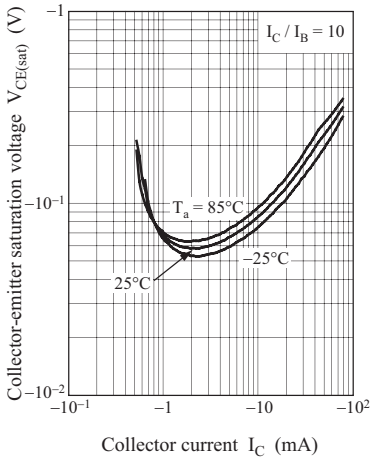
P_T — T_a



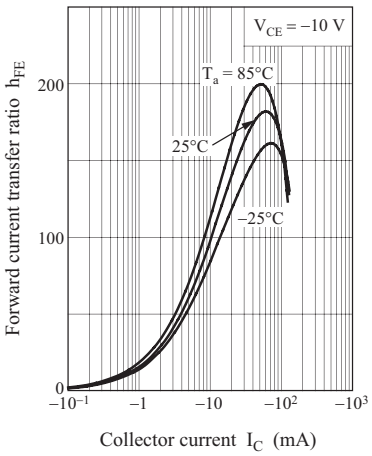
I_C — V_{CE}



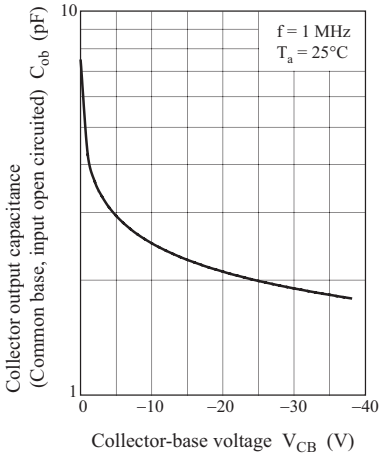
$V_{CE(sat)}$ — I_C



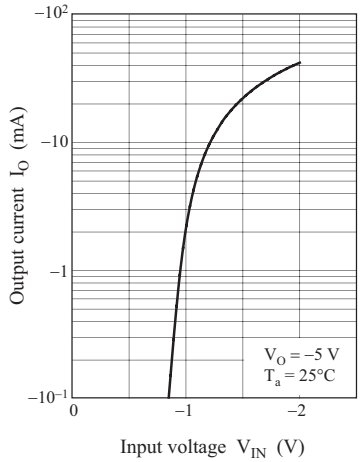
h_{FE} — I_C



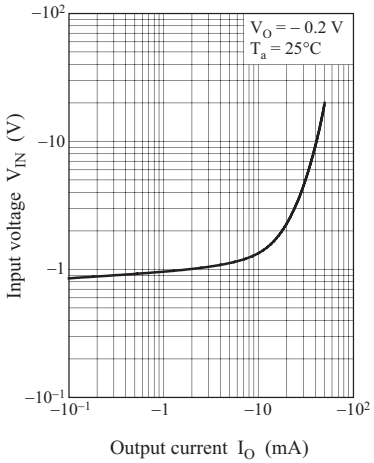
C_{ob} — V_{CB}



I_O — V_{IN}



V_{IN} — I_O



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