PRELIMINARY

16-CHARACTER 2-LINE DOT MATRIX LCD CONTROLLER DRIVER

■ GENERAL DESCRIPTION

The **NJU6635** is a 1Chip Dot Matrix LCD controller driver for up to 16-character 2-line display with double height function.

It contains microprocessor Interface circuits, Instruction decoder controller, character generator ROM/RAM and common and segment drivers.

The bleeder resistance generates for LCD Bias voltage Internally.

The CR oscillator Incorporates C and R, therefore no external components for oscillation are required.

The microprocessor Interface circuits which operate 2MHz frequency, can be connected directly to 4/8bit microprocessor.

The character generator consists of 9,600 bits ROM and 32 x 5 bits RAM. The standard version ROM is coded with 240 characters including capital and small letter fonts.

The 16-common and 80-segment drive up to 16-character 2-line LCD panel which divided two common electrode blocks.

The rectangle outlook is very applicable to COG.

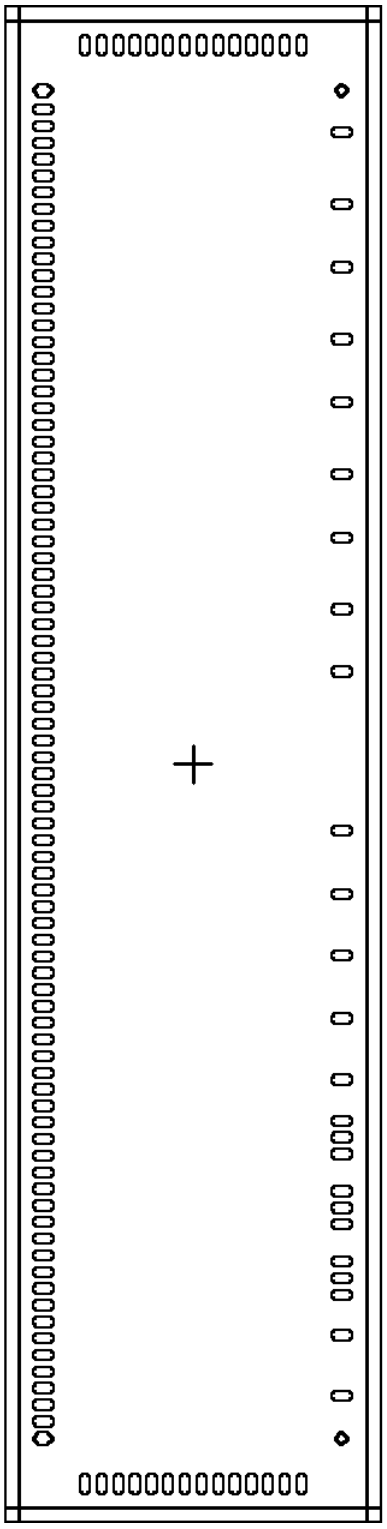
■ PACKAGE OUTLINE

NJU6635CH

■ FEATURES

- 16-character 2-line Dot Matrix LCD Controller Driver
- 4/8 Bit Microprocessor direct Interface
- Display Data RAM :32 x 8 bits : Maximum 16-character 2line Display
- Character Generator ROM :9,600 bits ; 240 characters for 5 x 8 dots
- Character Generator RAM :32 x 5 bits ; 4 Patterns(5 x 8 dots)
- Microprocessor direst accessing to Display Data RAM and Character Generator RAM
- High Voltage LCD Driver :16-common / 80-segment
- Duty Ratio :1/16 Duty
- Maximum Display Characters ; 32 Characters
- Useful Instruction Set
  Clear Display, Returns Home, Display ON/OFF Cont, Cursor ON/OFF Cont, Display Blink, Cursor Shift, Character Shift, Double Height Function.
- Power On Reset / Hardware Reset Function
- Oscillation Circuit on chip
- Bleeder Resistance on chip
- Low Power Consumption
- Operating Voltage --- +5V
- Package Outline --- Bumped Chip
- C-MOS Technology

■ PAD LOCATION



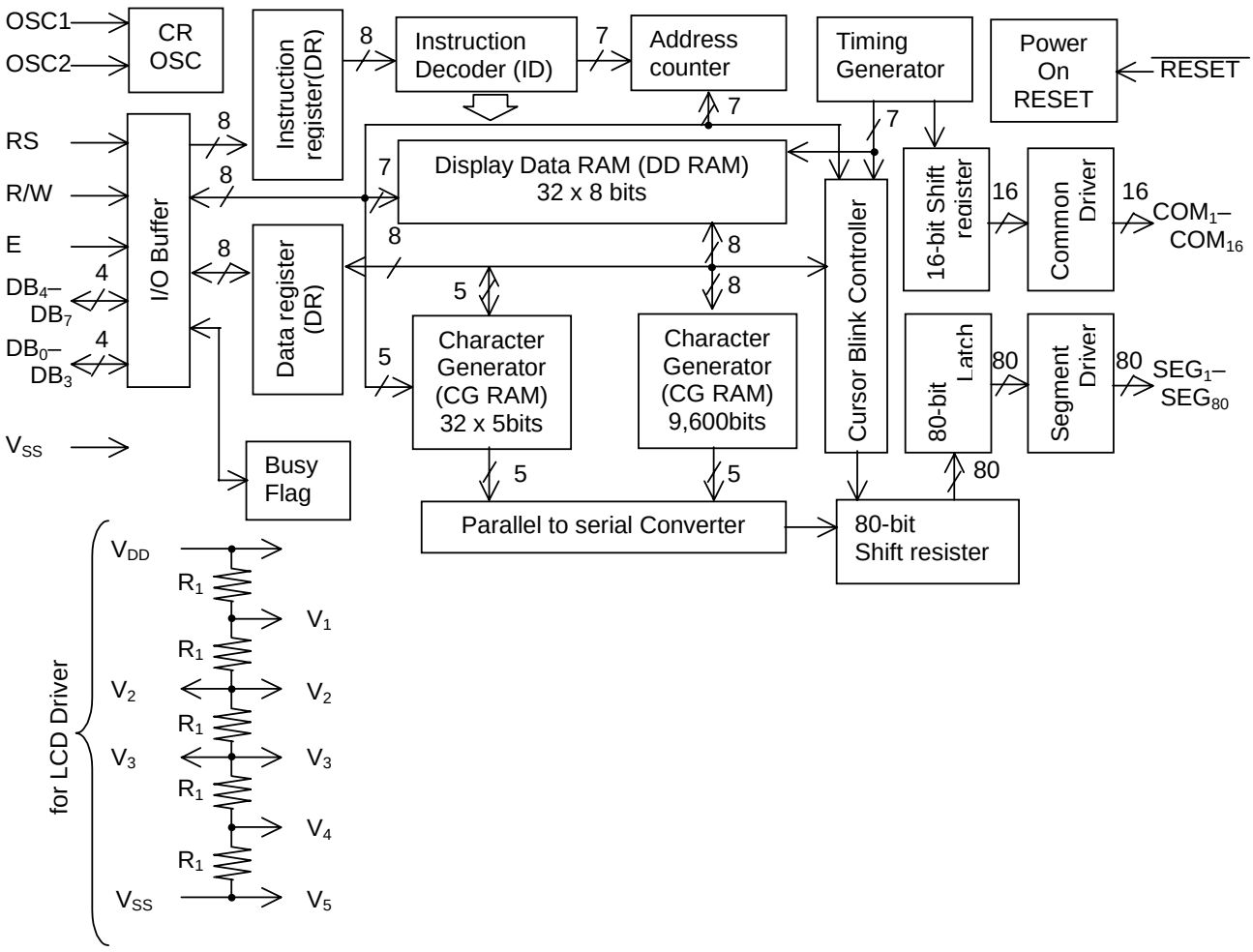
CHIP SIZE	:5.49 x 1.37mm	BUMP SIZE	:45 x 83µm
CHIP CENTER	:X=0µm, Y=0µm	BUMP HEIGHT	:17.5µm Typ.
		BUMP MATERIAL	:Au

■ PAD COORDINATES

Chip Size(5490μm x 1370μm)

PAD No.	PAD Name		X= um	Y= um
	A mode	B mode		
1	DMY_1	DMY_1	-2435	-534
2	OSC1	OSC1	-2282	-534
3	OSC2	OSC2	-2061	-534
4	V_{SS}	V_{SS}	-1916	-534
5	V_{SS}	V_{SS}	-1856	-534
6	V_{SS}	V_{SS}	-1796	-534
7	V_{DD}	V_{DD}	-1661	-534
8	V_{DD}	V_{DD}	-1601	-534
9	V_{DD}	V_{DD}	-1541	-534
10	V_5	V_5	-1407	-534
11	V_5	V_5	-1347	-534
12	V_5	V_5	-1287	-534
13	V_3	V_3	-1138	-534
14	V_2	V_2	-918	-534
15	RESET	RESET	-689	-534
16	RS	RS	-468	-534
17	RW	RW	-239	-534
18	E	E	336	-534
19	DB_0	DB_0	561	-534
20	DB_1	DB_1	820	-534
21	DB_2	DB_2	1049	-534
22	DB_3	DB_3	1308	-534
23	DB_4	DB_4	1537	-534
24	DB_5	DB_5	1797	-534
25	DB_6	DB_6	2025	-534
26	DB_7	DB_7	2285	-534
27	DMY_2	DMY_2	2435	-534
28	DMY_3	DMY_3	2600	-390
29	DMY_4	DMY_4	2600	-330
30	DMY_5	DMY_5	2600	-270
31	DMY_6	DMY_6	2600	-210
32	COM_1	COM_9	2600	-150
33	COM_2	COM_{10}	2600	-90
34	COM_3	COM_{11}	2600	-30
35	COM_4	COM_{12}	2600	30
36	COM_5	COM_{13}	2600	90
37	COM_6	COM_{14}	2600	150
38	COM_7	COM_{15}	2600	210
39	COM_8	COM_{16}	2600	270
40	DMY_7	DMY_7	2600	330
41	DMY_8	DMY_8	2600	390
42	DMY_9	DMY_9	2435	541
43	SEG_1	SEG_{80}	2370	541
44	SEG_2	SEG_{79}	2310	541
45	SEG_3	SEG_{78}	2250	541
46	SEG_4	SEG_{77}	2190	541
47	SEG_5	SEG_{76}	2130	541
48	SEG_6	SEG_{75}	2070	541
49	SEG_7	SEG_{74}	2010	541
50	SEG_8	SEG_{73}	1950	541
51	SEG_9	SEG_{72}	1890	541
52	SEG_{10}	SEG_{71}	1830	541
53	SEG_{11}	SEG_{70}	1770	541
54	SEG_{12}	SEG_{69}	1710	541
55	SEG_{13}	SEG_{68}	1650	541
56	SEG_{14}	SEG_{67}	1590	541
57	SEG_{15}	SEG_{66}	1530	541
58	SEG_{16}	SEG_{65}	1470	541
59	SEG_{17}	SEG_{64}	1410	541
60	SEG_{18}	SEG_{63}	1350	541
61	SEG_{19}	SEG_{62}	1290	541
62	SEG_{20}	SEG_{61}	1230	541
63	SEG_{21}	SEG_{60}	1170	541
64	SEG_{22}	SEG_{59}	1110	541
65	SEG_{23}	SEG_{58}	1050	541
66	SEG_{24}	SEG_{57}	990	541
67	SEG_{25}	SEG_{56}	930	541
68	SEG_{26}	SEG_{55}	870	541
69	SEG_{27}	SEG_{54}	810	541
70	SEG_{28}	SEG_{53}	750	541
71	SEG_{29}	SEG_{52}	690	541
72	SEG_{30}	SEG_{51}	630	541
73	SEG_{31}	SEG_{50}	570	541
74	SEG_{32}	SEG_{49}	510	541
75	SEG_{33}	SEG_{48}	450	541
76	SEG_{34}	SEG_{47}	390	541
77	SEG_{35}	SEG_{46}	330	541
78	SEG_{36}	SEG_{45}	270	541
79	SEG_{37}	SEG_{44}	210	541
80	SEG_{38}	SEG_{43}	150	541
81	SEG_{39}	SEG_{42}	90	541
82	SEG_{40}	SEG_{41}	30	541
83	SEG_{41}	SEG_{40}	-30	541
84	SEG_{42}	SEG_{39}	-90	541
85	SEG_{43}	SEG_{38}	-150	541
86	SEG_{44}	SEG_{37}	-210	541
87	SEG_{45}	SEG_{36}	-270	541
88	SEG_{46}	SEG_{35}	-330	541
89	SEG_{47}	SEG_{34}	-390	541
90	SEG_{48}	SEG_{33}	-450	541
91	SEG_{49}	SEG_{32}	-510	541
92	SEG_{50}	SEG_{31}	-570	541
93	SEG_{51}	SEG_{30}	-630	541
94	SEG_{52}	SEG_{29}	-690	541
95	SEG_{53}	SEG_{28}	-750	541
96	SEG_{54}	SEG_{27}	-810	541
97	SEG_{55}	SEG_{26}	-870	541
98	SEG_{56}	SEG_{25}	-930	541
99	SEG_{57}	SEG_{24}	-990	541
100	SEG_{58}	SEG_{23}	-1050	541
101	SEG_{59}	SEG_{22}	-1110	541
102	SEG_{60}	SEG_{21}	-1170	541
103	SEG_{61}	SEG_{20}	-1230	541
104	SEG_{62}	SEG_{19}	-1290	541
105	SEG_{63}	SEG_{18}	-1350	541
106	SEG_{64}	SEG_{17}	-1410	541
107	SEG_{65}	SEG_{16}	-1470	541
108	SEG_{66}	SEG_{15}	-1530	541
109	SEG_{67}	SEG_{14}	-1590	541
110	SEG_{68}	SEG_{13}	-1650	541
111	SEG_{69}	SEG_{12}	-1710	541
112	SEG_{70}	SEG_{11}	-1770	541
113	SEG_{71}	SEG_{10}	-1830	541
114	SEG_{72}	SEG_9	-1890	541
115	SEG_{73}	SEG_8	-1950	541
116	SEG_{74}	SEG_7	-2010	541
117	SEG_{75}	SEG_6	-2070	541
118	SEG_{76}	SEG_5	-2130	541
119	SEG_{77}	SEG_4	-2190	541
120	SEG_{78}	SEG_3	-2250	541
121	SEG_{79}	SEG_2	-2310	541
122	SEG_{80}	SEG_1	-2370	541
123	DMY_10	DMY_10	-2435	541
124	DMY_11	DMY_11	-2600	390
125	DMY_12	DMY_12	-2600	330
126	COM_{16}	COM_8	-2600	270
127	COM_{15}	COM_7	-2600	210
128	COM_{14}	COM_6	-2600	150
129	COM_{13}	COM_5	-2600	90
130	COM_{12}	COM_4	-2600	30
131	COM_{11}	COM_3	-2600	-30
132	COM_{10}	COM_2	-2600	-90
133	COM_9	COM_1	-2600	-150
134	DMY_13	DMY_13	-2600	-210
135	DMY_14	DMY_14	-2600	-270
136	DMY_15	DMY_15	-2600	-330
137	DMY_16	DMY_16	-2600	-390

■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

PAD No.		SYMBOL	I/O	F U N C T I O N
A mode	B mode			
4 – 9	4 – 9	V_{DD}, V_{SS}	–	Power Source : V_{DD} = +5V, GND : V_{SS} = 0V
10 – 14	10 – 14	V_2, V_3, V_5	–	LCD driving Power Source
2	2	OSC_1	I	Oscillation Frequency Adjustment Terminals. Normally Open. (Oscillation C and R are Incorporated, Osc Freq.=540kHZ)
3	3	OSC_2	O	Oscillation Frequency Adjustment Terminals. Normally Open. This terminal also operates as the clock frequency monitor.
16	16	RS	I	Resister selection signal Input "0":Instruction Resister (Writing) Busy Flag (Reading) "1":Data Register (Writing / Reading)
17	17	R/W	I	Read/Write selection signal Input "0":Write "1":Read
18	18	E	I	Read/write activation Signal Input
26 – 23	26 – 23	DB_7 – DB_4	I/O	3-state Data Bus(Upper) to transfer the data between MPU and **NJU6635**. DB_7 is also used for the Busy Flag reading.
19 – 22	19 – 22	DB_3 – DB_0	I/O	3-state Data Bus(Lower) to transfer the data between MPU and **NJU6635**. In serial and 4bit parallel mode, these terminals are not used and should be open.
32 – 39, 126 – 133	133 – 126, 39 – 32	COM_1 – COM_{16}	O	LCD Common driving signal Terminals
43 – 122	122 – 43	SEG_1 – SEG_{80}	O	LCD segment driving signal Terminals
15	15	$\overline{RESET}$	I	Reset Terminal. When the “L” level Input over than 1.2ms to this terminal, the system will be reset.(f_{OSC}=540kHz)
1, 27 – 31, 40 – 42, 123 – 125, 134 – 137	1, 27 – 31, 40 – 42, 123 – 125, 134 – 137	$DUMMY_1$ – $DUMMY_{15}$	O	Dummy Terminal These terminals are electrically open.

■ FUNCTIONAL DESCRIPTION

(1)Description for each blocks

(1-1)Register

The **NJU6635** incorporates two 8-bit registers, an Instruction Register (IR) and a Data Register (DR).

The Register (IR) stores Instruction codes such as “Clear Display” and “Return Home”, and address data for Display Data RAM (DD RAM) and Character Generator RAM (CG RAM). The MPU can write the Instruction code and address data to the Register (IR), but it can not read out from the Register (IR).

The Register (DR) is a temporary storing register, the data in the Register (DR) is written into the DD RAM or CG RAM and read out from the DD RAM or CG RAM.

The data in the Register (DR) written by the MPU is transferred from the Register automatically to the DD RAM or CG RAM by Internal operation.

After reading the data in the Register (DR) by the MPU, the next address data in the DD RAM or CG RAM is transferred automatically to the Register (DR) for the next MPU reading.

These two registers are selected by the selection signal RS as shown below:

Table 1. Register operation control by RS and R/W signals.

Table 1. Register Operation

RS	R/W	Operation
0	0	Write
0	1	Read busy flag (DB_7) and address counter (DB_0 to DB_7)
1	0	Write (DR to DD or CG RAM)
1	1	Read (DD or CG RAM to DR)

(1-2)Busy Flag (BF)

When the internal circuits are operating, the busy flag is “1”, and any instruction reading is inhibited.

The busy flag (BF) is output from DB_7 when RS=”0” and R/W=”1” as shown in table 1.

The next instruction should be written after busy flag (BF) goes to “0”.

(1-3)Address Counter(AC)

The address Counter (AC) addresses the DD RAM and CG RAM.

When the address setting instruction is written into the Register (IR), the address information is transferred from Register (IR) to the counter (AC). The selection of either the DD RAM or CG RAM is also determined by this instruction.

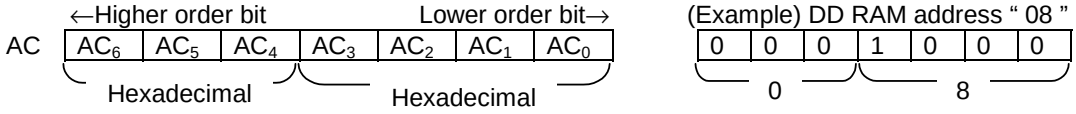
After writing (or reading) the display data to (or from) the DD RAM or CG RAM, the counter (AC) increments (or decrements) “1” automatically.

The address data in the Counter (AC) is output from DB_6 to DB_0 when RS=”0” and R/W=”1” as shown in table 1.

(1-4)Display Data RAM (DD RAM)

The display data RAM (DD RAM) consisting of 32 x 8 bits stores up to 32-character display data represented in 8-bit code.

The DD RAM address data set in the address Counter (AC) is represented in hexadecimal.



(1-4-1)16-character 2-line Display

The **NJU6635** has two kinds of addressing mode as " Addressing mode 1 " and " Addressing mode 2 " which is determined by the Function Set Instruction (A=0 and 1).

"Addressing mode 1" uses sequential address of $(00)_H$ through $(1F)_H$ for front half 16-character and last half 16-character. "Addressing mode 2 " does not use sequential address like as $(00)_H$ through $(1F)_H$ and $(40)_H$ through $(4F)_H$ for front half 16-character and last half 16-character respectively.

- Addressing mode 1: A=0

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	←Display Position
1st line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	←DD RAM Address
2nd line	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	(Hexadecimal)

The relation between DD RAM address and display position on the LCD shown below.

[Left Shift Display]

(00) ←	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
(10) ←	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	00

[Right Sift Display]

	1F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	→ (0F)
	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	→ (1F)

- Addressing mode 2: A=1

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← Display Position
1st line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← DD RAM Address
2nd line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	(Hexadecimal)

The relation between DD RAM address and display position on the LCD shown below.

[Left Shift Display]

(00) ←	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	00
(40) ←	41	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F

[Right Sift Display]

	0F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	→ (0F)
	4F	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	→ (4F)

(1-4-2)The relation between DD RAM address and display position on the LCD shown below.
(Double Height Sized display Function).

Correspondence between DD RAM Address and display position on the LCD panel.

In case of double height size Display function, the address of DD RAM which is set as follows the display, operates as 16-character 1-line and the addressing mode is ignored.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← Display Position
1st line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← DD RAM Address
2nd line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	(Hexadecimal)

When the display shift is performed, the DD RAM address changes as follows.

[Left Shift Display]

(00) ←	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	00
(00) ←	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	00

[Right Sift Display]

	0F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	→ (0F)
	0F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	→ (0F)

(1-5)Character Generator ROM(CG ROM)

The Character Generator ROM (CG ROM) generates 5 x 8 dots character pattern represented in 8-bit character codes.

The storage capacity is up to 240 kinds of 5 x 8 dots character pattern. The correspondence between character code and standard character pattern is shown in Table 2.

User-defined character pattern (Custom Font) are also available by mask option.

Table 2. CG ROM Character Pattern (ROM version –02)

Lower 4 bit (Hexadecimal) \ Upper 4 bit (Hexadecimal)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CG RAM (01)															
1	(02)															
2	(03)															
3	(04)															
4																
5																
6																
7																
8																
9																
A																
B																
C																
D																
E																
F																

(1-6)Character Generator RAM

The character generator RAM (CG RAM) stores any kinds of character pattern in 5 x 8 dots written by the user program to display user's original character pattern. The CG RAM stores 4 kinds of character in 5 x 8 dots mode.

To display user's original character pattern stored in the CG RAM, the address data $(00)_H$ – $(03)_H$ should be written to the DD RAM as shown in Table 2.

Table 3. shows the correspondence among the character pattern, CG RAM address and data.

Table 3. Correspondence of CG RAM address, DD RAM character code and CG RAM character pattern (5 x 8 dots)

Character Code (DD RAM Data)	CG RAM Address			Character Pattern (CG RAM Data)	
7 6 5 4 3 2 1 0 ← → Upper bit Lower bit	4 3 ← Upper bit	2 1 0 → Lower bit		4 3 2 1 0 ← → Upper bit Lower bit	
0 0 0 0 ∗ ∗ 0 0	00	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1		1 1 1 1 0 1 0 0 0 1 1 0 0 0 1 1 1 1 1 0 1 0 1 0 0 1 0 0 1 0 1 0 0 0 1 0 0 0 0 0	Character Pattern Example (1) ←Cursor Position
0 0 0 0 ∗ ∗ 0 1	0 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1		1 0 0 0 1 0 1 0 1 0 1 1 1 1 1 0 0 1 0 0 1 1 1 1 1 0 0 1 0 0 0 0 1 0 0 0 0 0 0 0	Character Pattern Example (2) ← Cursor Position
		0 0 0 0 0 1			
• • • • •	• • • • •	• • • • •		• • • • •	
0 0 0 0 ∗ ∗ 1 1	1 1	1 0 0 1 0 1 1 1 0 1 1 1			

Notes: 1. Character code bits 0 and 1 correspond to the CG RAM address 3 and 4 (2bits : 4 patterns).

2. CG RAM address 0, 1 and 2 designate a character pattern line position.
   The 8th line is the cursor position and the display is performed by logical OR with cursor. Therefore, in case of the cursor display, the data of 8th line should be "0".
   If there is "1" in the 8th line, the bit "1" is always displayed on the cursor position regardless of cursor existence.
3. Character pattern row position corresponding to the CG RAM data bits 0 to 4 are all shown above. The bits 5 to 7 of the CG RAM do not exist.
4. CG RAM character patterns are selected when character code bits 4 to 7 are all "0" and addressed by character code bits 0 and 1. Therefore the address $(00)_H$, $(04)_H$, $(08)_H$ and $(0C)_H$, select the same character pattern as shown In table 2 and Table 3.
5. "1" for CG RAM data corresponds to display On and "0" to display Off.

(1-7)Timing Generator

The timing generator generates a timing signals for the DD RAM, CG RAM, CG ROM and other internal circuit operation.

RAM read timing for the display and internal operation timing for MPU access are separately generated, so that they may not interfere with each other.

Therefore, when the data write to the DD RAM for example, there will be undesirable Influence, such as flickering, in areas other than the display area.

(1-8)LCD Driver

LCD driver consists of 16-common driver and 80-segment driver.

The 80 bits of character pattern data are shifted in the shift-register and latched when the 40 bits shift performed completely. This latched data controls display driver to output LCD driving waveform.

(1-9)Cursor Blinking Control Circuit

This circuits controls cursor On/Off and cursor position character blinks. The cursor or blinks appears in the digit position at the DD RAM address set in the address counter(AC).

When the address counter is $(08)_H$, a cursor position is shown as follows:

	AC_6	AC_5	AC_4	AC_3	AC_2	AC_1	AC_0
AC	0	0	0	1	0	0	0

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	← Display Position
1st line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	← DD RAM Address
2nd line	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	(Hexadecimal)

Cursor Position

Note) The cursor or blinks appears when the address counter (AC) selects the CG RAM.
But the displayed cursor and blink are meaningless.
If the AC stores the CG RAM address data, the cursor and blink are displayed in the meaningless position.

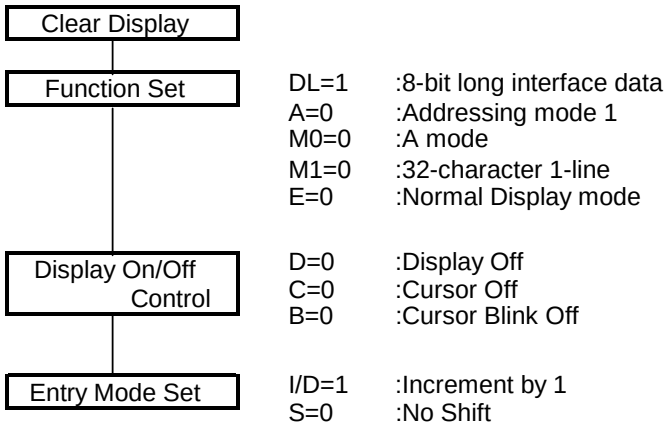
(2)Power on Initialization by internal circuits

(2-1) Initialization By internal Reset circuits

The **NJU6635** is initialized automatically by the internal power on initialization circuits when the power is turned on. In the internal power on initialization, following instructions are executed.

During the internal power on initialization, the busy flag (BF) is "1" and this status is kept 10ms after V_{DD} = 4.5V.

Initialization flow is shown below:

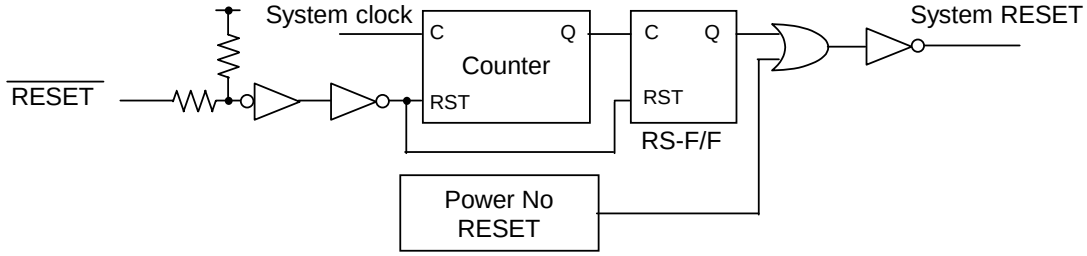


Note) If the condition of power supply rise time described in the Electrical Characteristics is not satisfied, the internal Power on initialization Circuits will not operate and initialization will not be performed. In this case, the initialization by MPU software is required.

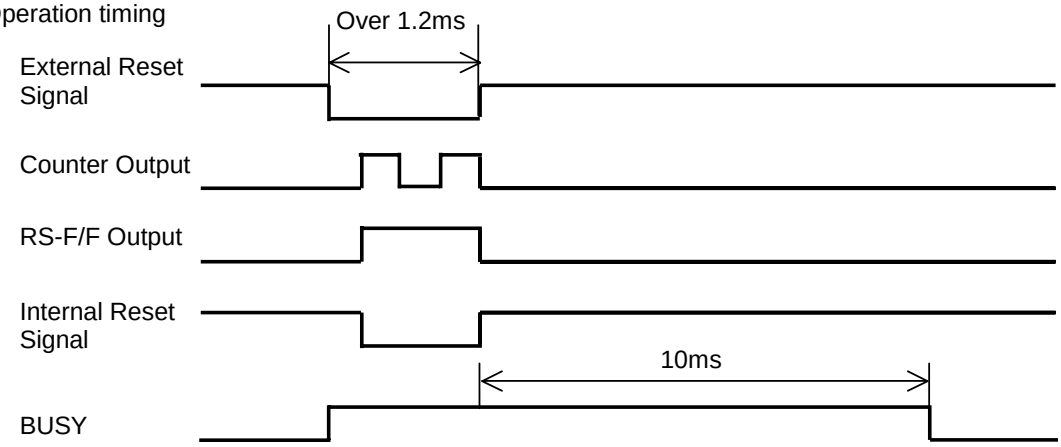
(2-2) Initialization By Hardware

The **NJU6635** incorporates RESET terminal to initialize the all system. When the "L" level input over than 1.2ms to the RESET terminal, the reset sequence is executed. In this time, the busy signal output during 10ms after RESET terminal goes to "H".

- RESET operation



- Operation timing



(3) Instructions

The **NJU6635** incorporates two resisters, which are Instruction Register (IR) and a Data Register (DR).

These two registers store control information temporarily to allow interface between **NJU6635** and MPU or peripheral ICs operating different cycles. The operation of **NJU6635** is determined by this control signal from MPU. The control information includes register selection signals (RS), read/write signals (R/W) and data bus signals (DB_0 to DB_7).

Table 5. Shows each instruction and its operating time.

Note) The execution time mentioned in Table 5. is based on fcp or f_{OSC}=540kHz.
If the oscillation frequency is changed, the execution time is also changed.

Table 5. Table of Instruction

INSTRUCTION	CODE										DESCRIPTION	EXEC TIME (f_{OSC}=540kHz)*
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
Maker Test	0	0	0	0	0	0	0	0	0	0	All “0” code is using for maker testing.	–
Clear Display	0	0	0	0	0	0	0	0	0	1	Display clear and sets DD RAM address 0 in AC.	315.9µs
Return Home / Font Size Set	0	0	0	0	0	0	0	0	1	E	Sets DD RAM address 0 In AC and returns display being shifted to original position. DD RAM contents remain unchanged.	18.5µs
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and species shift of display are performed In data read/write. I/D=1:Increment, I/D=D:Decrement,S=1:Accopa nies display shift.	18.6µs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Sets of display On/Off(D), cursor On/Off(C) and blink of cursor position character(B)	18.6µs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Move cursor and shifts display without changing DD RAM contents. S/C=1 : Display shift S/C=0 : Cursor shift R/L=1 : Shift to right R/L=0 : Shift to the left	28µs
Function Set	0	0	0	0	1	DL	A	*	M1	M0	Sets interface data length(DL), Display address mode(A) DL=1 : 8 bits, DL=0 : 4 bits A=0 : Addressing mode 1 A=1 : Addressing mode 2 M1=0 : 32-Character 1-Line M1=1 : 16-Character 2-Line M0=0 : Pin configuration mode A M0=1 : Pin configuration mode B	18.6µs
Set CG RAM Address	0	0	0	1	*	CG RAM address					Sets CG RAM address. After this instruction, the data is transferred on CG RAM.	18.6µs
Set DD RAM Address	0	0	1	DD RAM address							Sets DD RAM address. After this instruction, the data is transferred on DD RAM.	18.5µs
Read Busy Flag & Address	0	1	BF	AC							Read busy flag and AC contents. BF=1 : Internally operating BF=0 : Can accept instruction	0µs
				*	*	AC						
Write Data to CG or DD or MK RAM	1	0	Write Data(DD RAM)								Writes data into CG or DD RAM.	18.6µs
			*	*	*	(CG RAM)						
Read Data from CG or DD or MK RAM	1	1	Read Data(DD RAM)								Reads data from CG or DD RAM	28µs
			*	*	*	(CG RAM)						
Explanation of Abbreviation	DD RAM : Display data RAM, CG RAM : Character generator RAM ACG : CG RAM address, ADD : DD RAM address, Corresponds to cursor address AC : Address counter used for both DD and CG RAM											

*=Don’t Care

(3-1) Description of instruction

a) Maker Test

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	0	0

All “0” code in 4-bit length is using device testing mode (only for maker).

Therefore, please avoid all “0” input or no meaning Enable signal input at data “0” (Especially please pay attention to the output condition of Enable signal when the power turns on).

All “0” code in 8-bit length is usable for NOP (Not Operating instruction).

b) Clear Display

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	0	1

Clear display instruction is executed when the code “1” is written into DB_0.

In case of normal display mode, when this instruction is executed, the space code $(20)_H$ is written into every DD RAM address, the DD RAM address 0 is set into the address counter and entry mode is set an increment. If the cursor or blink are displayed, they are returned to the left end of the LCD.

The S of entry mode and CG RAM data does not change.

In case of double height mode, when this instruction is executed, the space code $(20)_H$ is written into DD RAM address,$(00)_H$ to $(0F)_H$.

Note: The character pattern for character code $(20)_H$ must be blank code in the user-defined character pattern(Custom font).

c) Return Home / Font Size Set

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	1	E

Return home instruction is executed when the code “1” is written Into DB_1. When this Instruction is executed, the DD RAM address 0 is set to address counter. Display is returned to the original position if shifted, the cursor or blink is returned to the left end of the LCD. If the cursor or blink are on the display, the DD RAM contents are not changed.

The normal display mode is executed when the code “0” is written Into DB_0.

The double height mode function is set by writing “1” Into DB_0.

The character of DD RAM address, $(00)_H$ to $(0F)_H$, are expanded to double height size (5 x 16 dots) and “Return Home” function is operated. In this time, access from $(10)_H$ to $(1F)_H$ or $(40)_H$ to $(4F)_H$ of DD RAM address is not available but the data in RAM are kept. Therefore, when the display mode returns from double height to normal, the kept data in RAM displays again.

In case of no display, “clear display” should be operated before transition from normal mode to double height.

The cursor size is also expanded to 5 x 2 dots.

Double height sized display function and Normal are not operated in the mean time.

The font in double height mode is some as normal.

E	FUNCTION
0	Normal Display mode (Font Size : 5 x 8dots)
1	Double height sized Display mode (Font Size : 5 x 16 dots) in case of DD RAM address : $(00)_H$ to $(0F)_H$.

d) Entry Mode Set

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	1	I/D	S

Entry mode set instruction which sets cursor moving direction and display shift On/Off, is executed when the code "1" is written into DB_2 and the codes of (I/D) and (S) are written into DB_1 (I/D) and DB_0 (S) as shown below.

(I/D) sets the address increment or decrement, and the (S) sets the entire display shift in the DD RAM writing.

I/D	FUNCTION
0	Address increment : The address of the DD RAM increment (+1) when the read/write, and the cursor or blink moves to the right.
1	Address decrement : The address of the DD or CG RAM decrement (-1) when the read/write, and the cursor or blink move to the left.

S	FUNCTION
1	Entire display shift. The shift direction is determined by I/D: shift to the left at I/D=1 and shift to the right at the I/D=0. The shift is operated with only the character, so that it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM and writing/reading into/from CG RAM.
0	The display does not shifting

e) Display ON/OFF Control

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	1	D	C	B

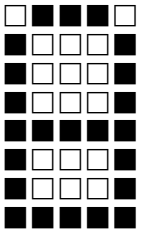
Display On/Off control instruction which controls the display On/Off, the cursor On/Off and the cursor position character blink, is executed when the code "1" is written into DB_3 and the codes of (D), (C) and (B) are written into DB_2(D), DB_1(C) and DB0(B) as shown below.

D	FUNCTION
1	Display On.
0	Display Off. In this mode, the display data remains in the DD RAM so that it is retrieved immediately on the display when the D change to 1.

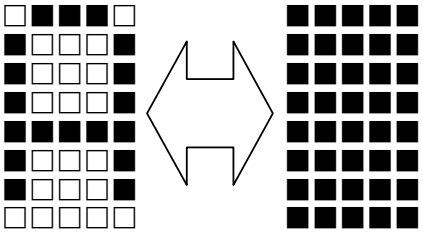
C	FUNCTION
1	Cursor On. The cursor is displayed by 5 dots on the 8th line.
0	Cursor Off. Even if the display data write, the I/D etc does not change.

B	FUNCTION
1	The cursor position character is blinking. Blinking rate is 303.4ms at f_{OSC}=540kHz. The blink is displayed alternatively with all on (it means all black) and characters display. The cursor and the blink can be displayed simultaneously.
0	The character does not blink.

- Normal display mode

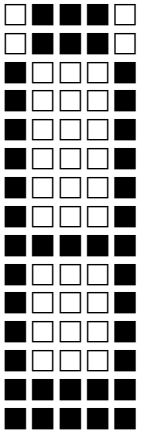


Character Font 5 x 7dots
(1) Cursor display example

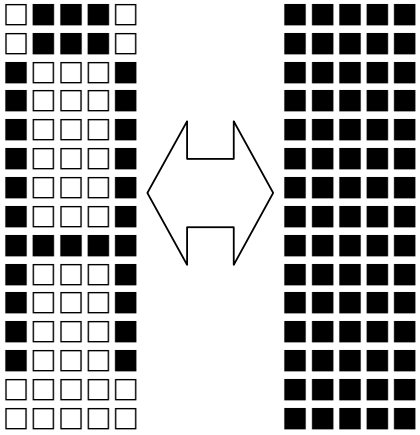


Alternating display
(2) Blink display example

- Double height sized display mode



Character Font 5 x 14dots
(3) Cursor display example



Alternating display
(2) Blink display example

f) Cursor Display Shift

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	1	S/C	R/L	*	*

*=Don't Care

The Cursor/Display shift instruction shifts the cursor position or display the right or left without writing reading display data.

The contents of address counter (AC) is not changed by operation of display shift only.

This instruction is executed when the code "1" is written into DB_4 and the codes of (S/C) and (R/L) are written into DB_3 (S/C) and DB_2(R/L) as shown below.

S/C	R/L	FUNCTION
0	0	Shifts the cursor position to the left ((AC) is decrement by 1)
0	1	Shifts the cursor position to the right ((AC) is incremented by 1)
1	0	Shifts the entire display to the left and the cursor follows it.
1	1	Shifts the entire display to the right and the cursor follows it.

g) Function Set

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	1	DL	A	*	M1	M0

*=Don't Care

Function set instruction which sets the interface data length, the addressing mode for the DD RAM, 1-line or 2-line display, and Pin configuration mode, is executed when the code "1" is written into DB_5 and the codes of (DL), (A), (M1) and (M0) are written into DB_4 (DL), DB_3 (A), DB_1 (M1), and DB_0 (M0) as shown below (character font is fixed 5 x 8 dots).

Note) This function set instruction must be performed at the head of the program prior to all other instructions (except Busy flag/Address read). This function set instruction can not be executed afterwards unless the interface data length change.

DL	FUNCTION
1	Set the interface data length to 8 bits (DB_7 to DB_0)
0	Set the interface data length to 4 bits (DB_7 to DB_4) A couple of data must be sent or received.

A	FUNCTION
0	Set the Addressing Mode 1 for the DD RAM
1	Set the Addressing Mode 2 for the DD RAM

M1	FUNCTION
0	Set the 32-Character 1-Line Display
1	Set the 16-Character 2-Line Display

M0	FUNCTION
0	Set the Pin configuration mode A for Common and Segment Driver (Refer to cord.)
1	Set the Pin configuration mode B for Common and Segment Driver (Refer to cord.)

h) Set CG RAM Address

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	1	*	A	A	A	A	A
				← Higher order bit →		← Lower order bit →				

Set CG RAM address instruction is executed when the code "1" is written into DB_6 and the address is written into DB_4 to DB_0 as shown above.

The address data mentioned by binary code "AAAAA " is written into the address counter (AC) together with the CG RAM addressing condition. After this instruction, the data writing/reading is performed into/from the CG RAM.

CG RAM address

CG RAM : $(00)_H$ – $(1F)_H$

i) Set DD RAM Address

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	1	A	A	A	A	A	A	A
			← Higher order bit →				← Lower order bit →			

Set DD RAM address instruction is executed when the code "1" is written into DB_7 and the address is written into DB_6 to DB_0 as shown above.

The address data mentioned by binary code "AAAAAAA " is written into the address counter (AC) together with the DD RAM addressing condition. After this instruction, the data writing/reading is performed into/from the DD RAM.

The DD RAM address is indicated as follows, which is available for DD RAM address only.

Normal mode condition

	DD RAM address
DD RAM 1-Line	: $(00)_H$ – $(0F)_H$
DD RAM 2-Line (Addressing mode 1)	: $(10)_H$ – $(1F)_H$
DD RAM 2-Line (Addressing mode 2)	: $(40)_H$ – $(4F)_H$

Double height size display condition

	DD RAM address
DD RAM 1-Line	: $(00)_H$ – $(0F)_H$

j) Read Busy Flag & Address

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	1	BF	A	A	A	A	A	A	A
			← Higher order bit →				← Lower order bit →			

This instruction reads out the internal status of the **NJU6635**. When this instruction is executed, the busy flag (BF) which indicates the internal operation, is read out from DB_7 and the address of CG RAM or DD RAM is read out from DB_6 to DB_0 (an address for CG RAM or DD RAM is determined by the previous instruction).

(BF)=1 indicates that internal operation is in progress. The next instruction is inhibited when (BF)=1. Check the (BF) status before the next write operation.

k) Write Data to CG or DD RAM

- Write data to CG RAM

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	0	*	*	*	D	D	D	D	D
			← Higher order bit →				← Lower order bit →			

- Write data to DD RAM

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	0	D	D	D	D	D	D	D	D
			← Higher order bit →				← Lower order bit →			

*=Don't Care

Write Data to CG RAM or DD RAM instruction is executed when the code "1" is written into (RS) and code "0" is written into (R/W).

By the execution of this instruction, the binary 5-bit data "DDDDD" are written into the CG RAM, and the binary 8-bit data "DDDDDDDD" are written into the DD RAM. The selection of the CG RAM or DD RAM is determined by the previous instruction.

After this instruction execution, the address increment(+1) or decrement(-1) is performed automatically according to the entry mode set. And the display shift is also executed according to the previous entry mode set.

l) Read Data from CG or DD RAM

- Read data to DD RAM

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	1	D	D	D	D	D	D	D	D
			← Higher order bit →				← Lower order bit →			

- Read data to CG RAM

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	0	*	*	*	D	D	D	D	D
			← Higher order bit →				← Lower order bit →			

*=Don't Care

Read Data to CG RAM or DD RAM instruction is executed when the code "1" is written into (RS) and (R/W).

By the execution of this instruction, the binary 5-bit data "DDDDD" are read out from CG RAM, and the binary 8-bit data "DDDDDDDD" are read out from DD RAM. The selection of the CG RAM or DD RAM is determined by the previous instruction.

Before executing this instruction, either the CG RAM address set or DD RAM address set must be executed, otherwise the first read out data Invalidated.

When this instruction is serially executed, the next address data is normally read from the second read.

The address set instruction is not required if the cursor shift instruction is executed just beforehand (only DD RAM reading).

The cursor shift instruction has same function as the DD RAM address set, so that after reading the DD RAM, the address increment or decrement is executed automatically according to the entry mode.

But display shift does not occur regardless of the entry mode.

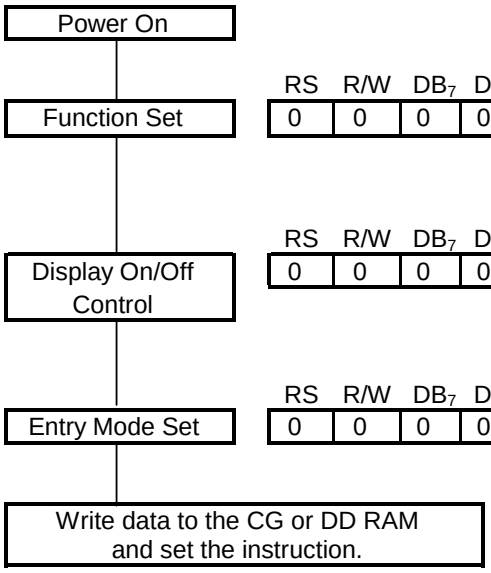
Note) The address counter (AC) is automatically incremented by 1 after write instructions to either of the CG RAM or DD RAM. Even if the read instruction is executed after this instruction, the addressed data can not be read out correctly.
For a correct data read out, either the address set instruction or cursor shift instruction (only with DD RAM) must be implemented just before this instruction or from the second time read out instruction execution if the read out instruction is executed 2 times consecutively.

(3-2)Initialization using the internal reset circuits

a) 32-character 1-line in 8-bit operation Addressing Mode 1 (Using internal reset circuits).

At the 32-character 1-line display, the Function set, On/Off Control and Entry Set Instruction must be executed before the data input, as shown below.

Since the display shift operation changes only display position and the DD RAM contents are unchanged, display data which are entered first can be output when the return home operation is performed.



Initialized.
No display appears.

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Function Set	0	0	0	0	1	1	0	*	0	0

Set the 8-bit operation, 32-Character 1-Line display, Pin configuration mode A, Addressing Mode 1.

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Display On/Off Control	0	0	0	0	0	0	1	1	1	0

Turns on display and cursor. Entire display is in space mode by the initialization.

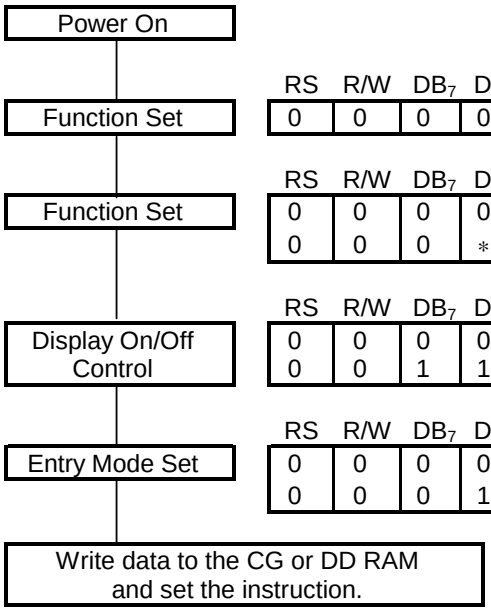
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Entry Mode Set	0	0	0	0	0	0	0	1	1	0

Example for set address increment and cursor right shift when the data write to the DD or CG RAM.

b) 32-character 1-line in 4-bit operation Addressing Mode 1 (Using internal reset circuits).

In the 4-bit operation, the function set must be performed by the user programming.

When the power is turned on, 8-bit operation is selected automatically, therefore the first input is performed under 8-bit operation. In this operation, full instruction can not input because of terminals DB_0 to DB_3 are no connection. Therefore, same instruction must be rewritten on the RS, R/W and DB_7 to DB_4, as shown below. Since one operation is completed by the two accesses in the 4-bit operation mode, rewrite is required to set the instruction code in full. 32-character 1-line in 4bit operation is shown as follows:



Initialized.
No display appears.

	RS	R/W	DB_7	DB_6	DB_5	DB_4
Function Set	0	0	0	0	1	0

Set the 4-bit operation.
This step is executed in 8-bit mode set by initialization.

	RS	R/W	DB_7	DB_6	DB_5	DB_4
Function Set	0	0	0	0	1	0
	0	0	0	*	0	0

Set the 4-bit operation /32-Character 1-Line display, Pin configuration mode A, Addressing Mode 1.
The 4-bit operation starts from this step.

	RS	R/W	DB_7	DB_6	DB_5	DB_4
Display On/Off Control	0	0	0	0	0	0
	0	0	1	1	1	0

Turns on display and cursor. Entire display is in space mode by the initialization.

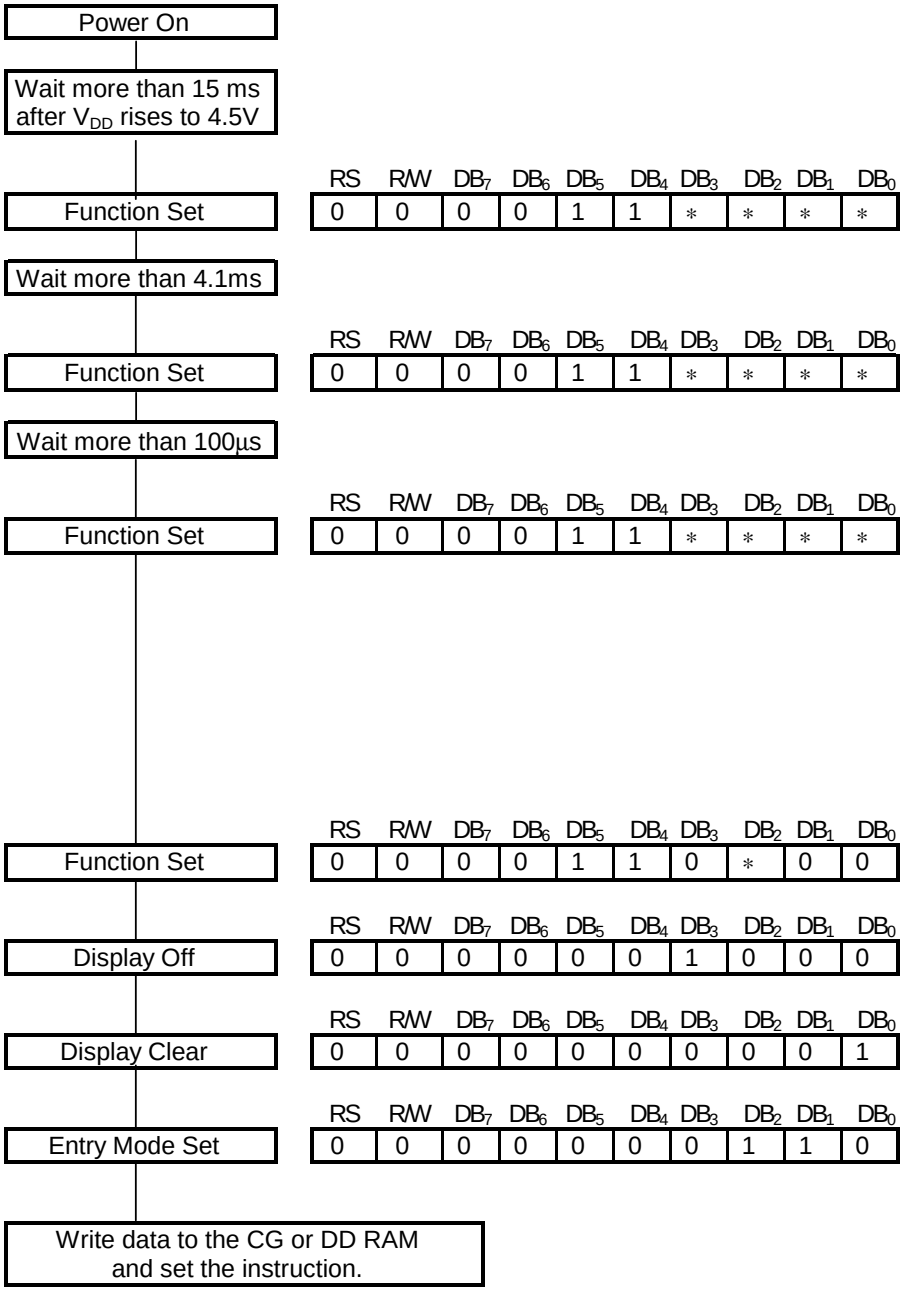
	RS	R/W	DB_7	DB_6	DB_5	DB_4
Entry Mode Set	0	0	0	0	0	0
	0	0	0	1	1	0

Example for set address increment and cursor right shift when the data write to the DD or CG RAM.

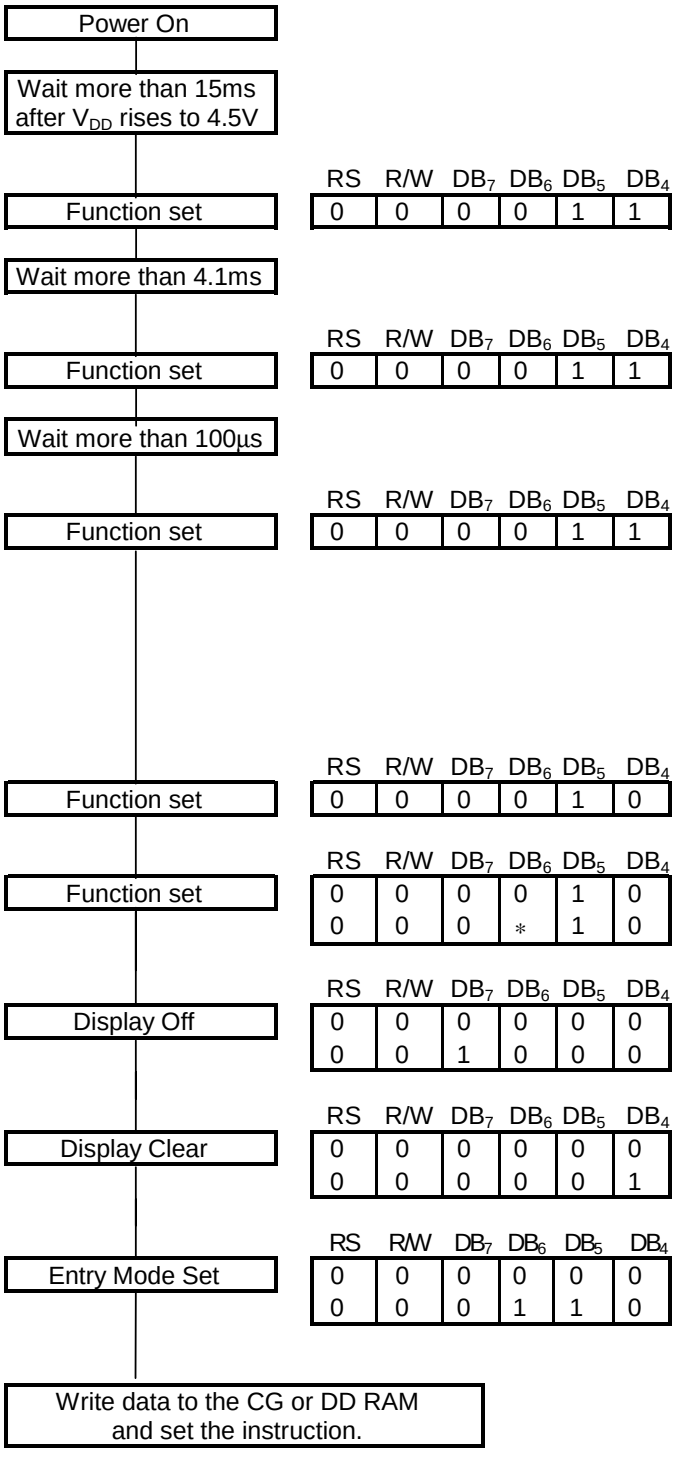
(3-3)Initialization by instruction

If the power supply conditions for the correct operation of the internal reset circuits are not method, the **NJU6635** must be initialized by the instruction.

a) Initialization by Instruction in 8-bit interface



b) Initialization by Instruction in 4-bit interface



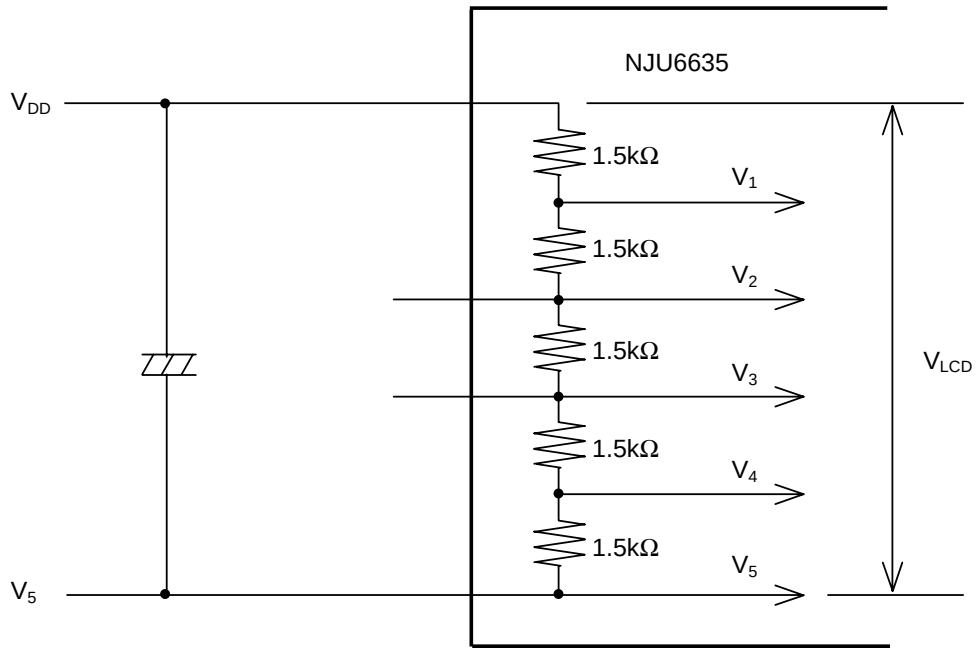
(4) LCD DISPLAY

NJU6635 incorporates bleeder resistance to generate the LCD display driving waveform.
The bleeder resistance is set 1/5 bias suitable for 1/18 duty ratio and 1.5kΩ per resistance.
The decoupling capacitor should be connected between V_{DD} and V_5 terminal.
The value of capacitor is determined depending on the actual LCD panel display evaluation.

LCD Driving Voltage vs. Duty Ratio

Power Supply	Duty Ratio	1/16
	Bias	1/5
	V_2	V_{DD}-2/5V_{LCD}
	V_3	V_{DD}-3/5V_{LCD}
	V_5	V_{DD}-V_{LCD}

∗ The V_{LCD} is maximum swing of LCD waveform.

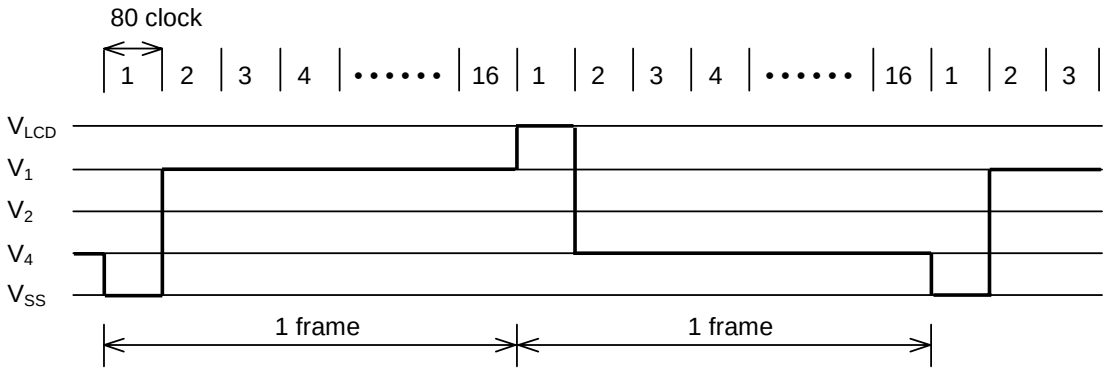


LCD Driving Voltage example

Note) Power ON or power OFF is in the following order.
Power ON : V_5 should be turned on after the V_{DD} turned on or at the same time.
Power OFF : V_5 should be turned off before the V_{DD} turned off or at the same time.

(4-1) Relation between oscillation frequency and LCD frame frequency.
LCD frame frequency example mentioned below is based on 540kHz oscillation.
The clock for the LCD driving is using 270/2 kHz (1 clock = 1.852μs)

- 1/16 duty

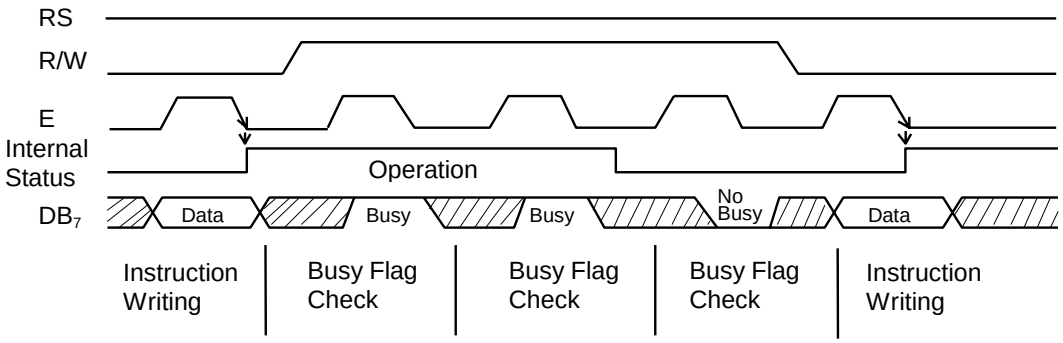


1 frame = 7.4 (μs) x 80 x 16 x 4 = 9.472(ms)
Frame frequency = 1/9.472(ms) = 105.6(Hz)

(5)Interface with MPU

NJU6635 can be interfaced with both of 4/8 bit MPU and the two-time 4-bit or one-time 8-bit data transfer is available.

(5-1)8-bit MPU interface

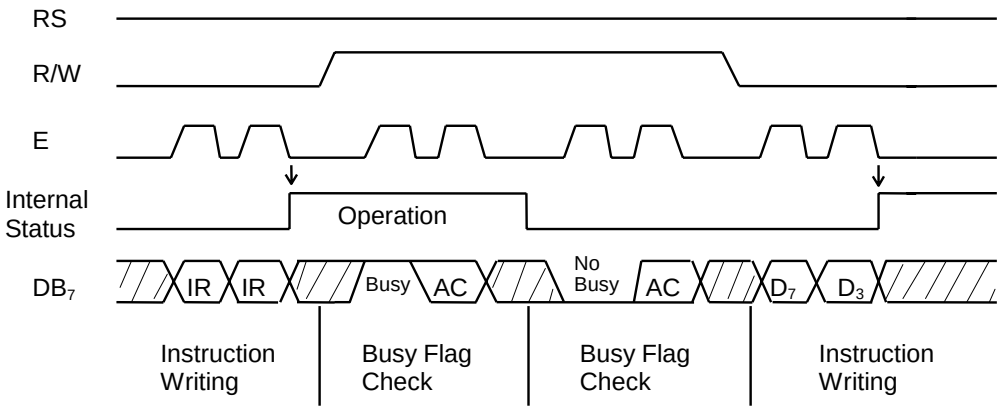


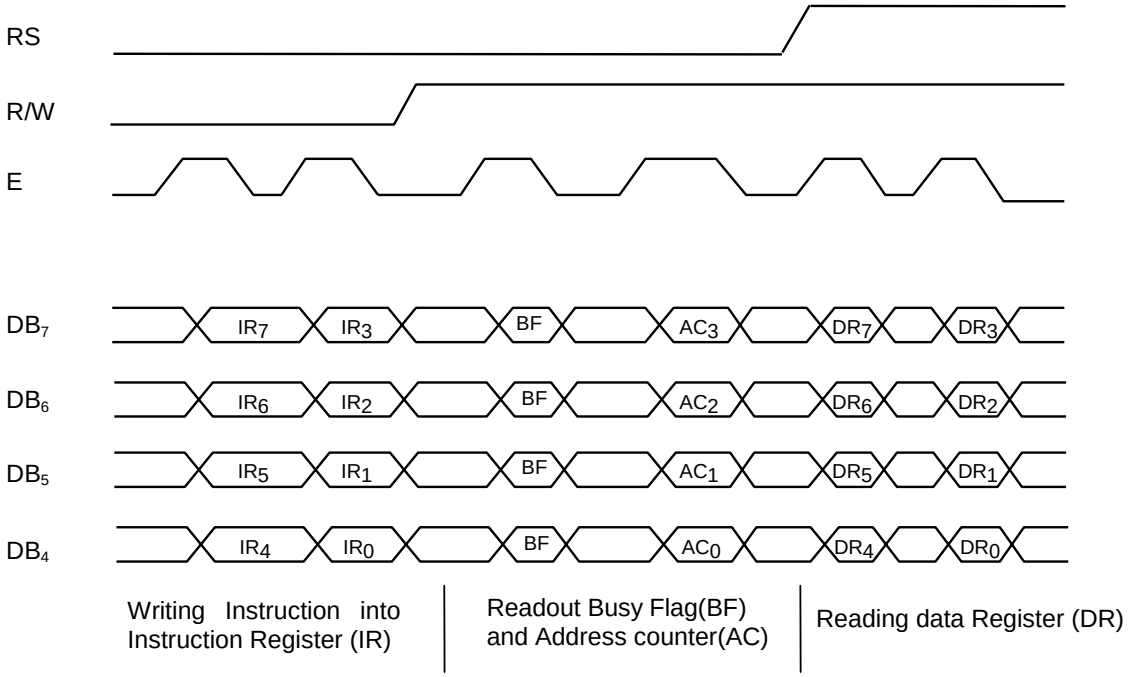
(5-2)4-bit MPU interface

When the interface length is 4-bit, the data transfer is performed by 4 lines connected to DB_4 to DB_7 (DB_0 to DB_3 are not used). The data transfer with the MPU is completed by the two-time 4-bit data transfer.

The data transfer is executed in the sequence of upper 4-bit (the data DB_4 to DB_7 at 8-bit length) and lower 4-bit (the data DB_0 to DB_3 at 8-bit length).

The busy flag check must be executed after two-time 4-bit data transfer (1 instruction execution). In this case the data of busy flag and address counter are also output twice.





■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

P A R A M E T E R	SYMBOL	R A T I N G S	UNIT
Supply Voltage	V_{DD}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.3 to V_{DD}+0.3	V
Operating Temperature	T_{opr}	-30 to +80	°C
Storage Temperature	T_{stg}	-55 to +125	°C

Note 1.) If the LSI is used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause malfunction and poor reliability.

Note 2.) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the LSI.

Note 3.) All voltage values are specified as V_{SS} =0V

Note 4.) The relation $V_{DD}>V_5\geq V_{SS}$, V_{SS}=0V must be maintained.

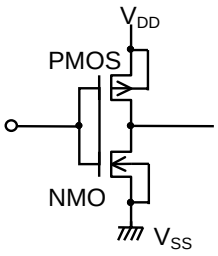
■ ELECTRICAL CHARACTERISTICS (V_{DD}=4.5 to 5.5V, V_{SS}=0V, Ta=-20 to 75°C)

PARAMETER	SYMBOL	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Operating Volt.	V_{DD}	V_{DD}	4.5	5.0	5.5	V	
Input Voltage 1	V_{IH1}	All Input / Output Terminals except OSC and E Terminals	2.3	–	V_{DD}	V	5
	V_{IL1}		–	–	0.8	V	
Input Voltage 2	V_{IH2}	Only OSC Terminals	V_{DD}-1.0	–	V_{DD}	V	5
	V_{IL2}		–	–	1.0	V	
Input Voltage 3	V_{IH3}	Only E Terminal	0.8 V_{DD}	–	V_{DD}	V	5
	V_{IL3}		–	–	0.2 V_{DD}	V	
Output Voltage	I_{OH}	$-I_{OH}$=0.205mA	2.4	–	–	V	6
	I_{OL}	I_{OL}=1.6mA	–	–	0.4	V	
Driver On-resist. (COM)	R_{COM}	$\pm I_d$=50µA (All com. Term.)	–	–	20	kΩ	9
Driver On-resist.(SEG)	R_{SEG}	$\pm I_d$=50µA (All SEG. Term.)	–	–	30	kΩ	
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{DD}	-1	–	1	µA	7
Pull-up Resist Current	$-I_P$	V_{DD}=5V	50	125	250	µA	
Operating Current	I_{DD}	V_{DD}=5V f_{OSC}=540kHz(CR Oscillation)	–	2.0	3.6	mA	8
LCD Driving Voltage	V_2	V_{DD}=5V, Ta=25°C, V_5=0V	2.7	3.0	3.3	V	
	V_3		1.7	2.0	2.3	V	
Bleeder Resistance	R_B	V_{DD}-V_5=5V, Ta=25°C	3.7	7.5	11.3	kΩ	
Oscillation Frequency	f_{OSC}	V_{DD}=5V, Ta=25°C	270	540	810	kHz	
LCD Driving Voltage	V_{LCD}	V_{LCD}= V_{DD}-V_5, $V_5\geq V_{SS}$	3	–	V_{DD}	V	10

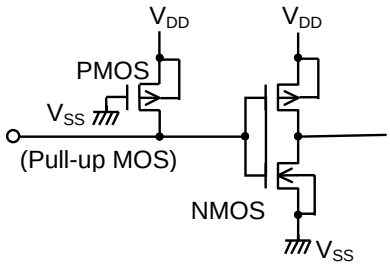
Note 5) Input / Output structure except LCD driver are shown below:

- Input Terminal Structure

E Terminal

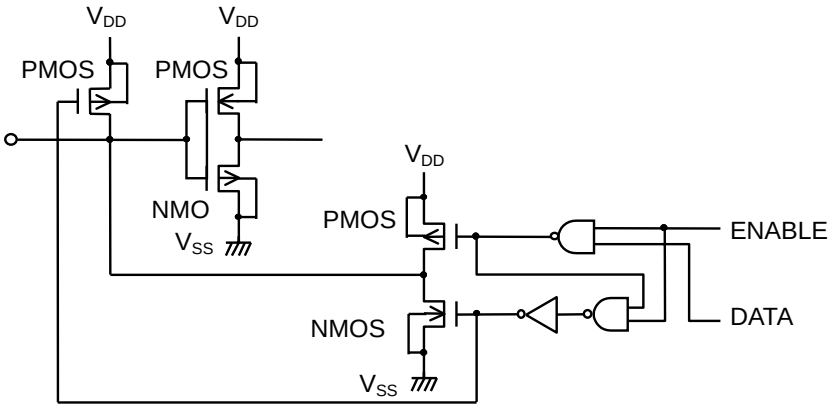


RS, R/W, RESET Terminals



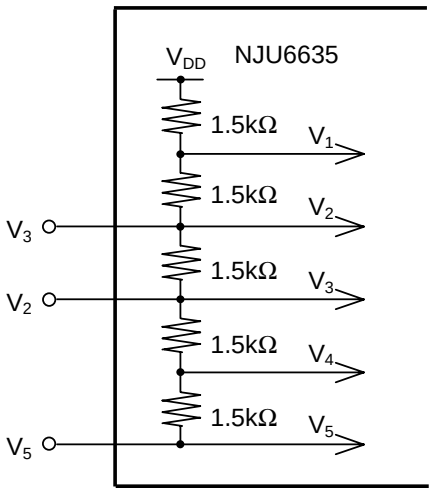
- Input / Output Terminal Structure

DB_0 to DB_7 Terminals



Note 6.) Apply to the Input / Output Terminals.
Note 7.) Except pull-up resistance current and output driver current.
Note 8.) Except Input / Output current but including the current flow on bleeder resistance.
Note 9.) RCOM and RSEG are the resistance values between power supply terminals(V_{DD}, V_2, V_3, V_5) and each common terminal (COM_1 to COM_{16}), and supply voltage (V_{DD}, V_2, V_3, V_5) and each segment terminal(SEG_1 to SEG_{80}) respectively, and measured when the current Id is flown on every common and segment terminals at the same time.
Note10.) Apply to the output voltage from each COM and SEG are less than ±0.15V against the LCD driving constant voltage (V_{DD},V_5) at no load condition.

- Bleeder resistance



■ Bus timing characteristics (V_{DD}=4.5 to 5.5V, V_{SS}=0V, Ta=-20 to 75°C)

• Write operation sequence (write from MPU to **NJU6635**)

PARAMETER		SYMBOL	MIN	MAX	UNIT	CONDITION
Enable Cycle Time		t_{CYCE}	500	–	ns	Fig.1
Enable Pulse Width	"High" level	PW_{EH}	220	–		
	Low" level	PW_{EL}	280	–		
Enable Rise Time, Fall Time		t_{Er}, t_{Ef}	–	20		
Set up Time	RS, R/W-E	t_{AS}	40	–		
Address Hold Time		t_{AH}	10	–		
Data Set up Time		t_{DSW}	60	–		
Data Hold Time		t_H	10	–		

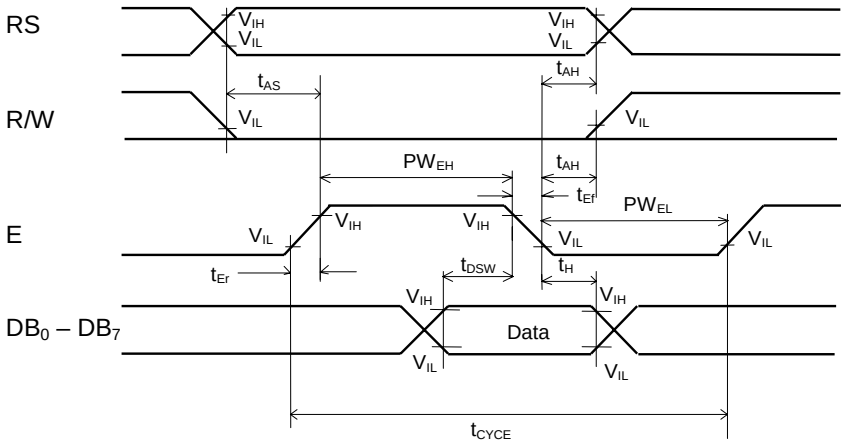


Fig.1 The timing characteristics of the bus write operating sequence.(Write from MPU to **NJU6635**)

• Read operation sequence (Read from **NJU6635** to MPU)

PARAMETER		SYMBOL	MIN	MAX	UNIT	CONDITION
Enable Cycle Time		t_{CYCE}	500	–	ns	Fig.2
Enable Pulse Time	"High" level	PW_{EH}	220	–		
	Low" level	PW_{EL}	280	–		
Enable Rise Time, Fall Time		t_{Er}, t_{Ef}	–	20		
Set up Time	RS, R/W-E	t_{AS}	40	–		
Address Hold Time		t_{AH}	10	–		
Data Delay Time		t_{DDR}	–	240		
Data Hold Time		t_{DHR}	20	–		

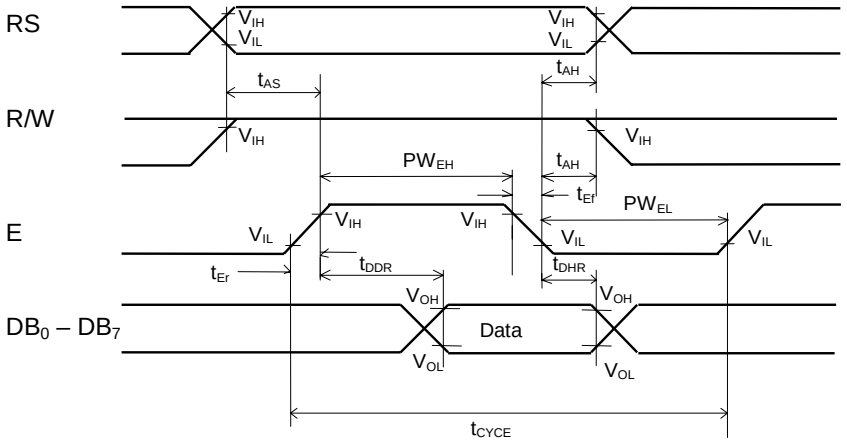
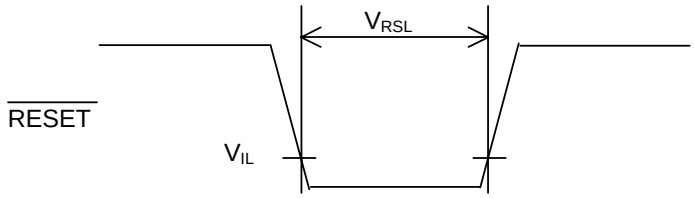


Fig.2 The timing characteristics of the bus write operating sequence.(Write from **NJU6635** to MPU)

• The Input Condition when using the Hardware Reset Circuit

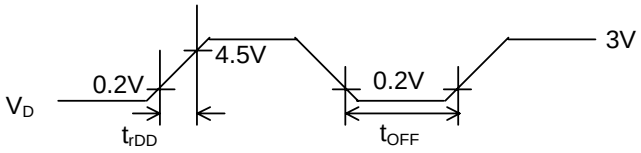
P A R A M E T E R	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
RESET input "Low" level width	t_{RSL}	f_{OSC} =540kHz	1.2	–	–	ms

Input timing



• Power supply condition when using the internal initialization circuit (Ta=-20 to 75°C)

P A R A M E T E R	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Power supply rise time	t_{rDD}	–	0.1	–	5	ms
Power supply OFF time	t_{OFF}	–	1	–	–	ms



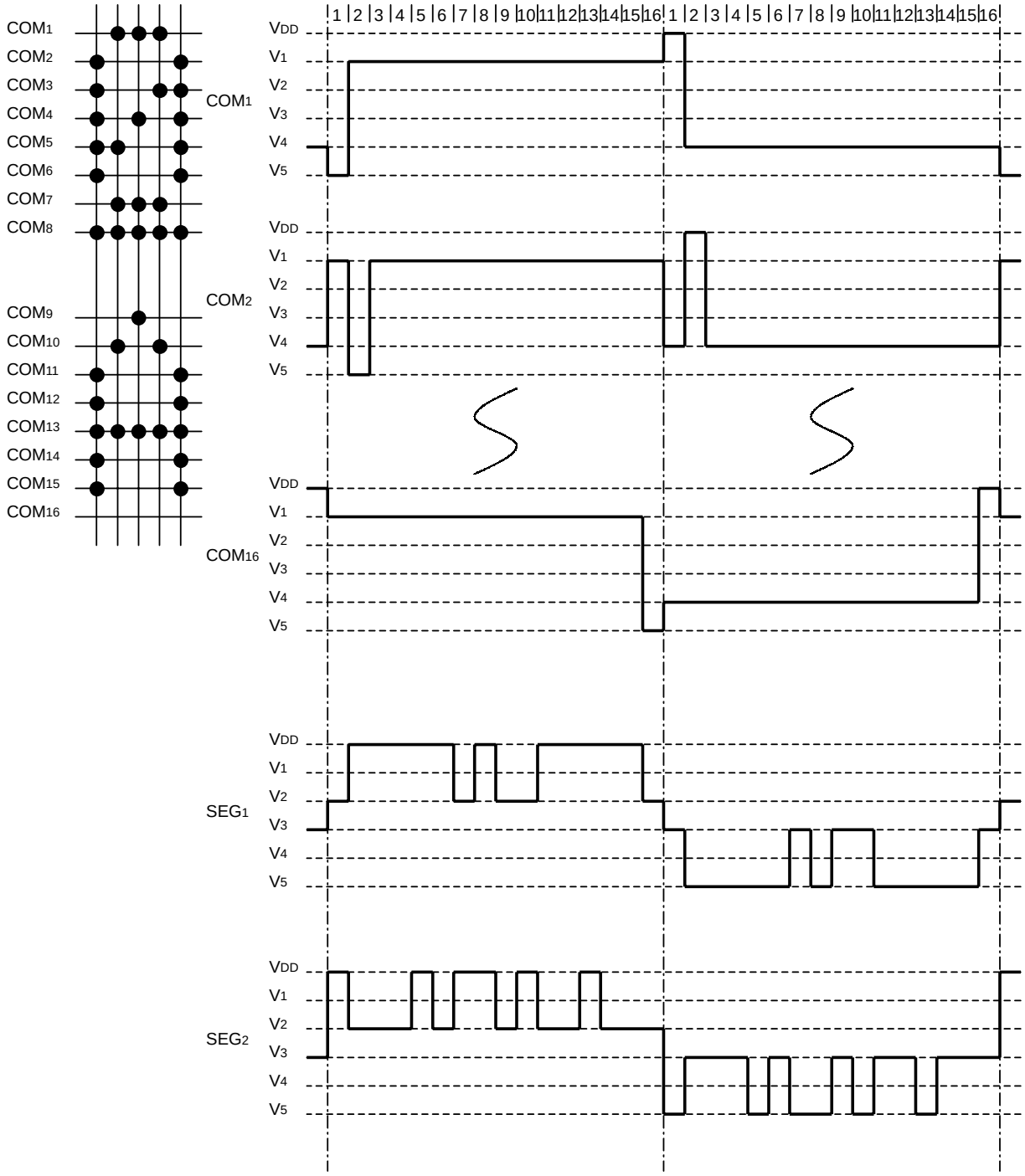
*t_{OFF} specifies the power OFF time in a short period OFF or cyclical ON/OFF

0.1ms ≤ t_{rDD} ≤ 10ms t_{OFF} ≤ 1ms

Note.) Since the internal initialization circuits will not operate normally unless the above conditions are met, in such a case initialize by instruction(Refer to initialization by the instruction).

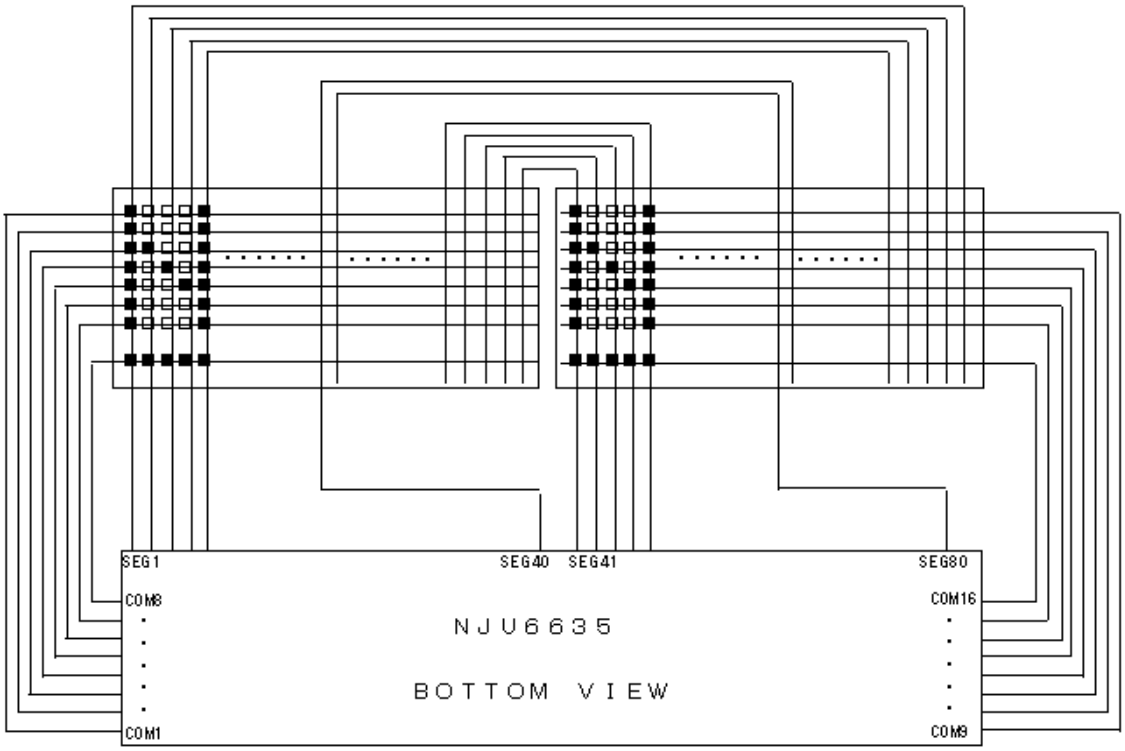
■ LCD DRIVING WAVE FROM

NJU6635 1/16 Duty driving

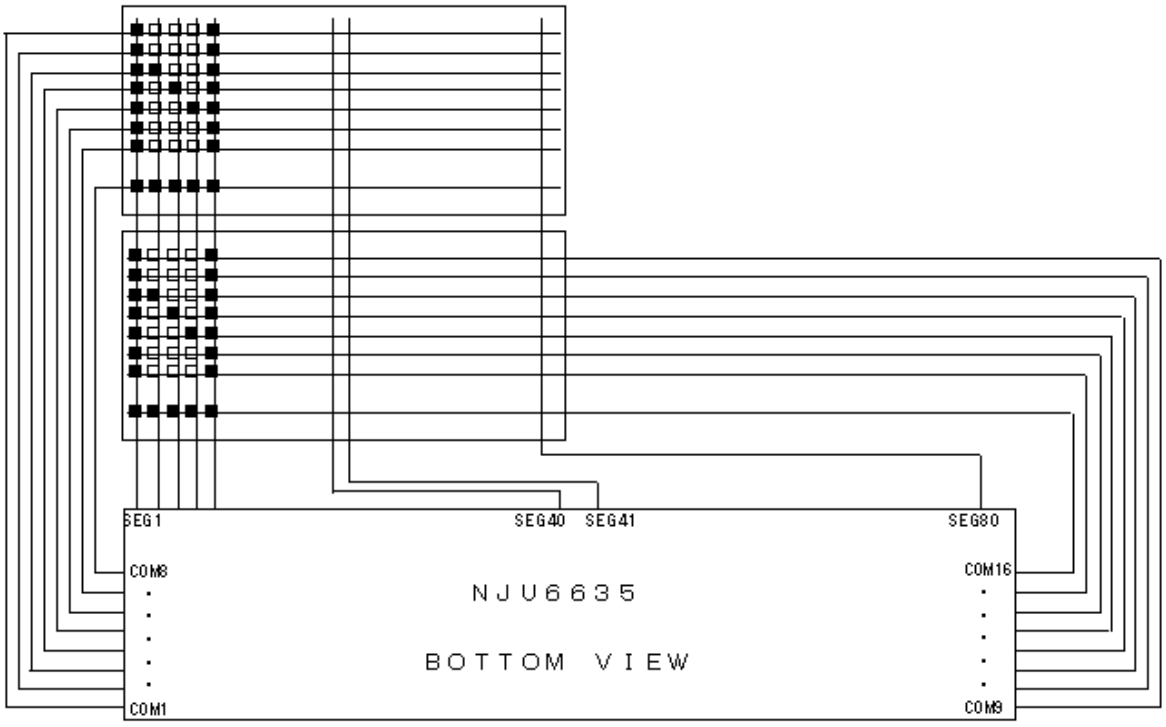


■ APPLICATION CIRCUITS

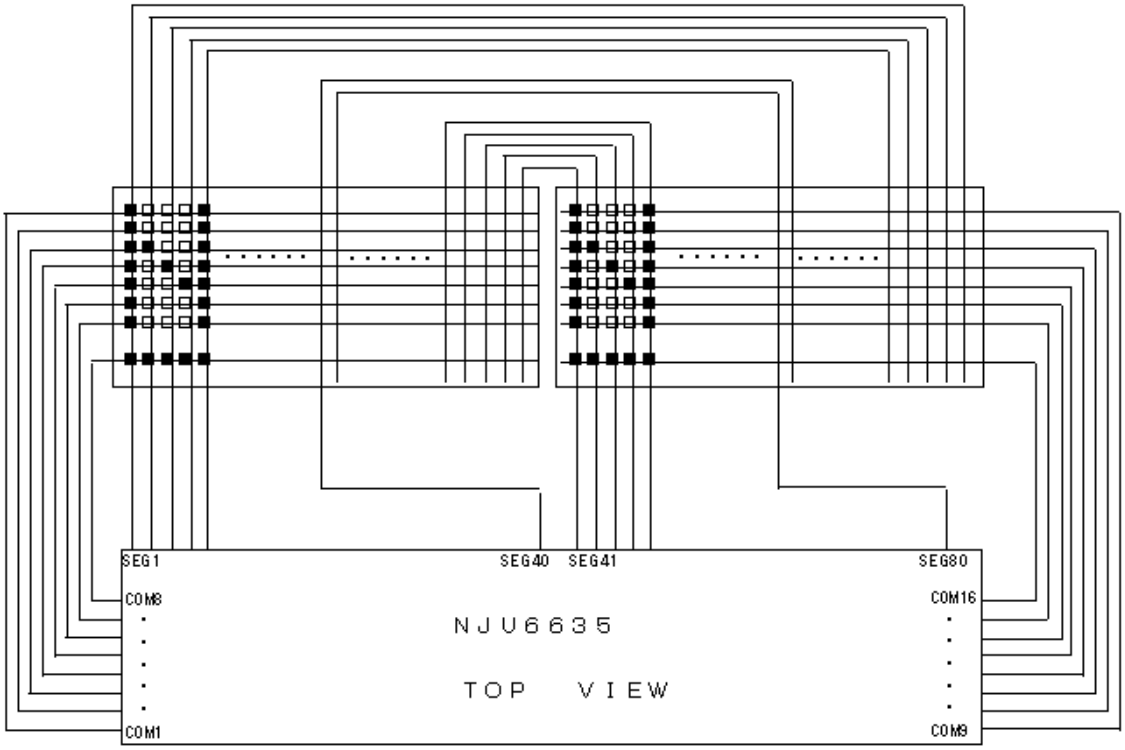
M0=0, M1=0 (32-character 1-line Mode A)



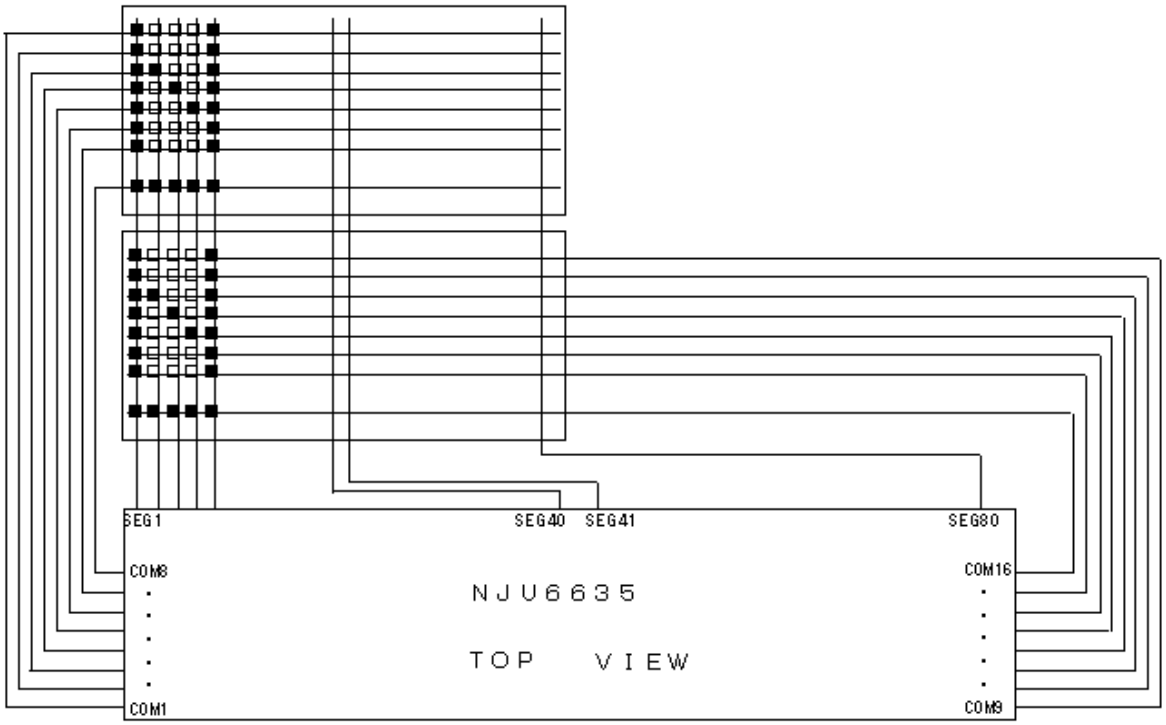
M0=0, M1=1 (16-character 2-line Mode A)



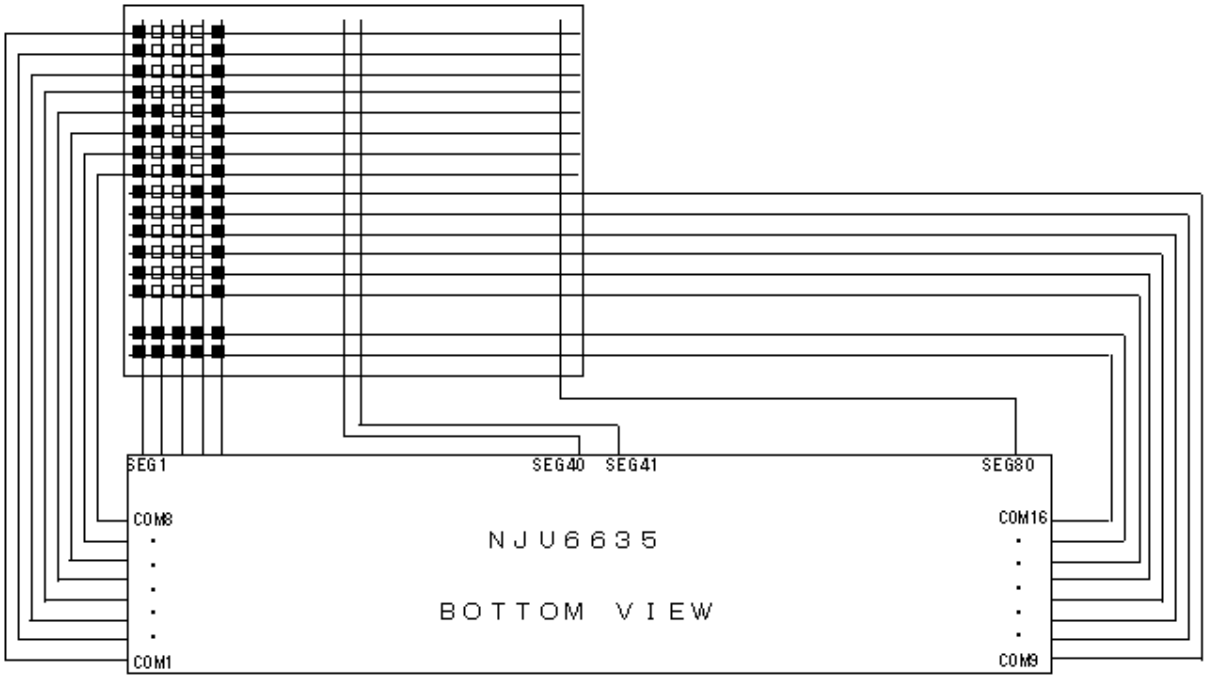
M0=1, M1=0 (32-character 1-line Mode B)



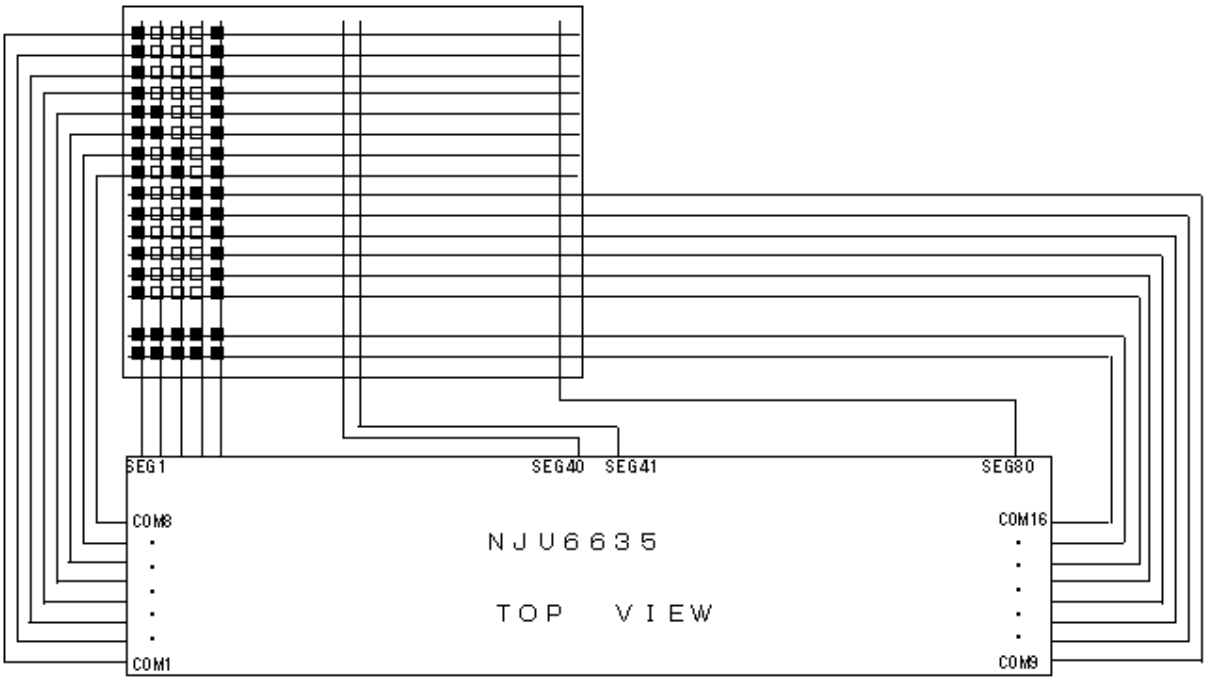
M0=1, M1=1 (16-character 2-line Mode B)



M0=0, M1=1 (16-character 1-line Mode A)



M0=1, M1=1 (16-character 1-line Mode B)



MEMO

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