STRUCTURE	Silicon Monolithic Integrated Circuit
TYPE	1ch Series Regulator Driver IC
PRODUCT SERIES	**BD3552HFN**
FEATURES	・High Accuracy Voltage Regulator(0.650±1%)
	・Vcc : 5.0V
	・Maximum Output Current : 2.0A
	・Non Rush Current on Start up (NRCS)

○Absolute Maximum Ratings (Ta=25℃)

PARAMETER	SYMBOL	RATING	UNIT
Input Voltage 1	VCC	+6.0 *1	V
Input Voltage 2	VIN	+6.0 *1	V
Output Current	IO	2.0*1	A
Enable Input Voltage	VEN	-0.3～+6.0	V
Power Dissipation 1	Pd1	0.63 *2	W
Power Dissipation 2	Pd2	1.35 *3	W
Power Dissipation 3	Pd3	1.75 *4	W
Operating Temperature Range	Topr	-10～+100	℃
Storage Temperature Range	Tstg	-55～+150	℃
Maximum Junction Temperature	Tjmax	+150	℃

*1 Should not exceed Pd.
*2 Reduced by 5.04mW/℃ for each increase in Ta≧25℃ (when mounted on a 70mm×70mm×1.6mm glass-epoxy board, 1-layer)
On less than 0.2% (percentage occupied by copper foil.)
*3 Reduced by 10.8mW/℃ for each increase in Ta≧25℃ (when mounted on a 70mm×70mm×1.6mm glass-epoxy board, 1-layer)
On less than 7.0% (percentage occupied by copper foil.)
*4 Reduced by 14.0mW/℃ for each increase in Ta≧25℃ (when mounted on a 70mm×70mm×1.6mm glass-epoxy board, 1-layer)
On less than 65.0% (percentage occupied by copper foil.)

○Operating Conditions (Ta=25℃)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Voltage 1	VCC	4.3	5.5	V
Input Voltage 2	VIN	0.95	VCC-1 *1 *5	V
Output Voltage Setting Range	VO	VFB	2.7	V
Enable Input Voltage	VEN	0	5.5	V
NRCS Capacity	CNRCS	0.001	1	uF

*5 VCC and VIN do not have to be implemented in the order listed.
★This product is not designed for use in radioactive environments.

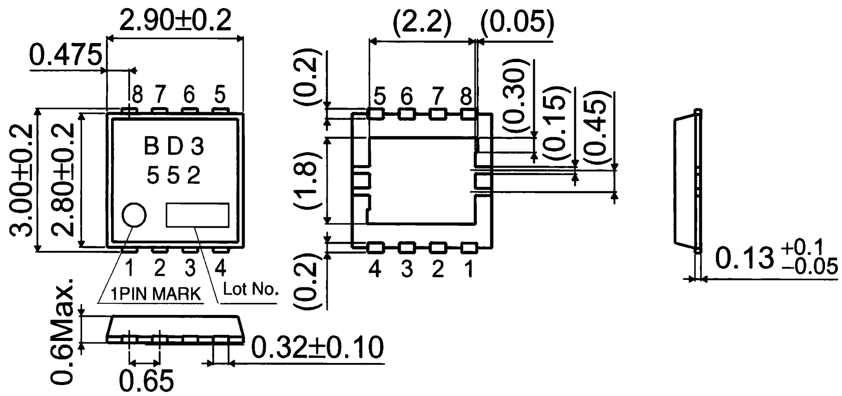
Status of this document
The Japanese version of this document is the official specification.
This translated version is intended only as a reference, to aid in understanding the official version.
If there are any differences between the original and translated versions of this document, the official Japanese language version takes priority.

○ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, Ta=25℃ VCC=5V Ven=3V VIN=1.8V R1=3.9kΩ R2=3.3kΩ)

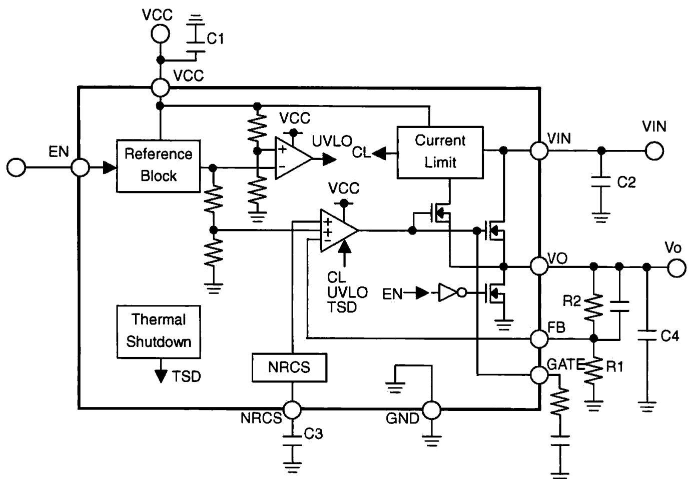
PARAMETER	SYMBOL	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
Bias current	ICC	-	0.5	1.0	mA	
Shut-Down Mode Current	IST	-	0	10	uA	Ven=0V
Maximum Output Current	Io	2.0	-	-	A	
Feed Back Voltage 1	VFB1	0.643	0.650	0.657	V	
Feed Back Voltage 2	VFB2	0.637	0.650	0.663	V	Tj=-10 to 100℃
Load Regulation	Reg.L	-	0.5	10	mV	Io=0 to 2A
Line Regulation 1	Reg.l1	-	0.1	0.5	%/V	VCC=4.3V to 5.5V
Line Regulation 2	Reg.l2	-	0.1	0.5	%/V	VIN=1.2V to 3.3V
Dropout Voltage	dVo	-	100	150	mV	Io=1A,VIN=1.2V Tj=-10 to 100℃
Standby Discharge Current	Iden	1	-	-	mA	Ven=0V, Vo=1V
[Enable]						
High level Enable Input Voltage	Enhi	2	-	-	V	
Low level Enable Input Voltage	Enlow	0	-	0.8	V	
Enable pin Input Current	Ien	-	7	10	uA	Ven=3V
[Voltage Feed Back]						
Feed Back terminal Bias Current	IFB	-100	0	100	nA	
[NRCS]						
NRCS Charge Current	Inrcs	14	20	26	uA	Vnrcs=0.5V
NRCS Standby Voltage	VSTB	-	0	50	mV	Ven=0V
[UVLO]						
VCC UVLO	VccUVLO	3.5	3.8	4.1	V	Vcc:Sweep-up
VCC UVLO Hysterisis	Vcchys	100	160	220	mV	Vcc:Sweep-down
[AMP]						
Gate Source Current	I_{GSO}	0.9	1.6	2.3	mA	V_{FB}=0, V_{GATE}=2.5V
Gate Sink Current	I_{GSI}	1.8	3.5	5.2	mA	V_{FB}=VCC, V_{GATE}=2.5V

○PHYSICAL DIMENSIONS



(UNIT : mm)
HSON8

○BLOCK DIAGRAM



○Pin number Pin name

PIN No.	PIN name
1	VCC
2	EN
3	GATE
4	VIN
5	VO
6	FB
7	NRCS
8	GND
–	FIN

○ NOTES FOR USE

(1) Absolute maximum range
Although the quality of this product is rigorously controlled, and circuit operation is guaranteed within the operation ambient temperature range, the device may be destroyed when applied voltage or operating temperature exceeds its absolute maximum rating. Because the failure mode (such as short mode or open mode) cannot be identified in this instance, it is important to take physical safety measures such as fusing if a specific mode in excess of absolute rating limits is considered for implementation.

(2) Ground potential
Make sure the potential for the GND pin is always kept lower than the potentials of all other pins, regardless of the operating mode, including transient conditions.

(3) Thermal Design
Provide sufficient margin in the thermal design to account for the allowable power dissipation (Pd) expected in actual use.

(4) Using in the strong electromagnetic field
Use in strong electromagnetic fields may cause malfunctions.

(5) ASO
Be sure that the output transistor for this IC does not exceed the absolute maximum ratings or ASO value.

(6) Thermal shutdown circuit
The IC is provided with a built-in thermal shutdown (TSD) circuit. When chip temperature reaches the threshold temperature shown below, output goes to a cut-off state. Note that the TSD circuit is designed exclusively to shut down the IC in abnormal thermal conditions. It is not intended to protect the IC or guarantee performance when extreme heat occurs. Therefore, the TSD circuit should not be employed with the expectation of continued use or subsequent operation once TSD is operated.

TSD ON temperature [℃] (typ.)	Hysteresis temperature [℃] (typ.)
175	15

(7) GND pattern
When both a small-signal GND and high current GND are present, single-point grounding (at the set standard point) is recommended, in order to separate the small-signal and high current patterns, and to be sure the voltage change stemming from the wiring resistance and high current does not cause any voltage change in the small-signal GND. In the same way, care must be taken to avoid wiring pattern fluctuations in any connected external component GND.

(8) Output Voltage Setting (R1, R2)
Output volage is adjusted with resistor R1 and R2. output voltage is calculated as VFBx(R1+R2)/R1. Total 10kohm resistor (R1+R2) is recommended so that the output voltage is not affected by the VFB bias current (Typ. 100nA).

(9) Output Capacitor (C4)
Mount an output capacitor between Vo1 to Vo3 and GND for stability purposes. The output capacitor is for the open loop gain phase compensation and reduces the output voltage load regulation. If the capacitor value is not large enough, the output voltage may oscillate. And if the equivalent series resistance (ESR) is too large, the output voltage rise/drop increases during a sudden load change. A Low ESR 47uF capacitor is recommended. However, the stability depends on the characteristics of temperature and load. And if several kinds of capacitors are utilized in parallel, the output voltage may oscillate due to lack of phase margin. Please confirm operation across a variety of temperature and load conditions.

(10) Input Capacitor (C1, C2)
The input capacitor reduces the output impedence of the voltage supply source connected in the VCC and VIN. If the output impedence of this power supply increases, the input voltage (VCC,VIN) may become unstable. This may result in the output voltage oscillation or lowering ripple rejection. Stability depends on power supply characteristics and the substrate wiring pattern. Please confirm operation across a variety of temperature and load conditions.

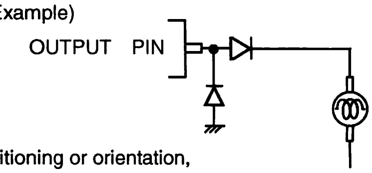
(11) NRCS (Non Rush Current on Start-up) Setting （C3）
The NRCS function is built in this IC to prevent rush current from going through the load (VIN to Vo) for start-up. The constant current comes from the NRCS pin when EN is high or UVLO function is deactivated. Temporary reference voltage is made proportional to time due to current charge the NRCS pin capacitor and make output voltage start up proportional to this reference volatge. To obtain a stable NRCS delay time, a capacitor (X5R or X7R) with susceptiblity to temperature is recommended.

(12) Input Terminal (VCC,VIN,EN)
The EN, VIN, and VCC are isolateted. The UVLO protects incorrect operation when the voltage level of VCC are low. The output becomes high when VCC and EN reach the individual threshold level independent of the start-up pin order. When VIN is the last on power-on seqrence, the output voltage may over shoot.

(13) Heat sink (FIN)
Since the heat sink (FIN) is connected with the Sub, short it to the GND. It is possible to minimize the thermal resistance by soldering it to GND plane of PCB.

(14) Please add a protection diode when a large inductance component is connected to the output terminal, and reverse-polarity power is possible at startup or in output OFF condition.

(Example)



(15) Short-circuits between pins and and mounting errors
Do not short-circuit between output pin (Vo) and supply pin (Vcc) or ground (GND), or between supply pin (Vcc) and ground (GND). Mounting errors, such as incorrect positioning or orientation, may destroy the device.

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Japan /
(Internal Sales)

Tokyo 2-1-1, Yaesu, Chuo-ku, Tokyo 104-0082
TEL : +81(3)5203-0321 FAX : +81(3)5203-0300

Yokohama 2-4-8, Shin Yokohama, Kohoku-ku, Yokohama, Kanagawa 222-8575
TEL : +81(45)476-2131 FAX : +81(45)476-2128

Nagoya Dainagayo Building 9F 3-28-12, Meieki, Nakamura-ku, Nagoya,Aichi 450-0002
TEL : +81(52)581-8521 FAX : +81(52)561-2173

Kyoto 579-32 Higashi Shiokouji-cho, Karasuma Nishi-iru, Shiokoujidori, Shimogyo-ku,
Kyoto 600-8216
TEL : +81(75)311-2121 FAX : +81(75)314-6559

(Contact address for overseas customers in Japan)

Yokohama TEL : +81(45)476-9270 FAX : +81(045)476-9271

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