Preferred Device

PNP Silicon General Purpose High Voltage Transistor

This PNP Silicon Planar Transistor is designed for general purpose amplifier applications. This device is housed in the SC-70/SOT-323 package which is designed for low power surface mount applications.

Features

• Pb-Free Packages are Available

MAXIMUM RATINGS $(T_A = 25^{\circ}C)$

Rating	Symbol	Value	Unit	
Collector-Base Voltage	V _{(BR)CBO}	-300	Vdc	
Collector-Emitter Voltage	V _{(BR)CEO} –300		Vdc	
Emitter-Base Voltage	V _{(BR)EBO}	-5.0	Vdc	
Collector Current – Continuous	I _C	500	mAdc	
Electrostatic Discharge	ESD	MBM > 16,000, MM > 2,000	V	

THERMAL CHARACTERISTICS

Rating	Symbol	Max	Unit	
Power Dissipation (Note 1)	P _D	150	mW	
Junction Temperature	TJ	150	°C	
Storage Temperature Range	T _{stg}	-55 to +150	°C	

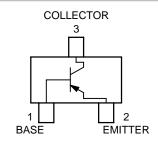
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

 Device mounted on a FR-4 glass epoxy printed circuit board using the minimum recommended footprint.



ON Semiconductor®

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SC-70 (SOT-323) CASE 419 STYLE 3

MARKING DIAGRAM



xx = Device Code x= 2D or D2

M = Date Code*

= Pb-Free Package

(Note: Microdot may be in either location)
*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping [†]
MSB92WT1	SC-70/ SOT-323	3000/Tape & Reel
MSB92WT1G	SC-70/ SOT-323 (Pb-Free)	3000/Tape & Reel
MSB92AWT1	SC-70/ SOT-323	3000/Tape & Reel
MSB92AWT1G	SC-70/ SOT-323 (Pb-Free)	3000/Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit Vdc	
Collector-Emitter Breakdown Voltage $(I_C = -1.0 \text{ mAdc}, I_B = 0)$	V _(BR) CEO	-300	-		
Collector-Base Breakdown Voltage $(I_C = -100 \mu Adc, I_E = 0)$	V _{(BR)CBO}	-300	_	Vdc	
Emitter-Base Breakdown Voltage $(I_E = -100 \mu Adc, I_E = 0)$	V _{(BR)EBO}	-5.0	_	Vdc	
Collector-Base Cutoff Current $(V_{CB} = -200 \text{ Vdc}, I_E = 0)$	I _{CBO}	_	-0.25	μΑ	
Emitter–Base Cutoff Current $(V_{EB} = -3.0 \text{ Vdc}, I_B = 0)$	I _{EBO}	_	-0.1	μΑ	
DC Current Gain (Note 2) MSB92WT1: $(V_{CE} = -10 \text{ Vdc}, I_{C} = -1.0 \text{ mAdc})$ MSB92AWT1: $(V_{CE} = -10 \text{ Vdc}, I_{C} = -1.0 \text{ mAdc})$ $(V_{CE} = -10 \text{ Vdc}, I_{C} = -10 \text{ mAdc})$ $(V_{CE} = -10 \text{ Vdc}, I_{C} = -30 \text{ mAdc})$	h _{FE1} h _{FE1} h _{FE2} h _{FE3}	25 120 40 25	_ 200 _ _	-	
Collector-Emitter Saturation Voltage (Note 2) $(I_C = -20 \text{ mAdc}, I_B = -2.0 \text{ mAdc})$	V _{CE(sat)}	-	-0.5	Vdc	
Base–Emitter Saturation Voltage (I _C = -20 mAdc, I _B = -2.0 mAdc)	V _{BE(sat)}	-	-0.9	Vdc	
SMALL SIGNAL CHARACTERISTICS	<u> </u>				
Current – Gain – Bandwidth Product (I _C = –10 mAdc, V _{CE} = –20 Vdc, f = 20 MHz)	f⊤	50	_	MHz	
Collector–Base Capacitance (V _{CB} = -20 Vdc, I _E = 0, f = 1.0 MHz)	C _{cb}	_	6.0	pF	

^{2.} Pulse Test: Pulse Width ≤ 300 μs, D.C. ≤ 2%.

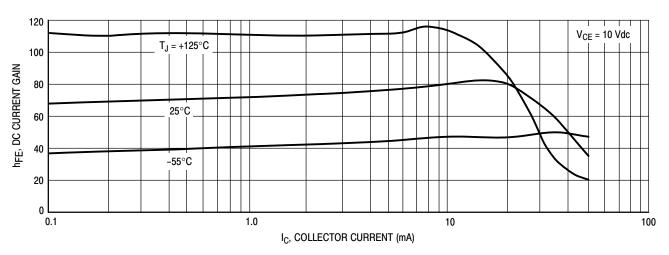


Figure 1. DC Current Gain

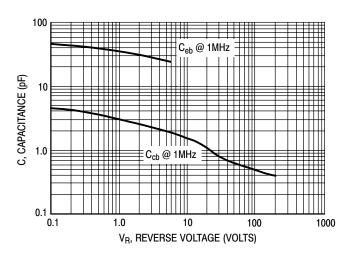


Figure 2. Capacitance

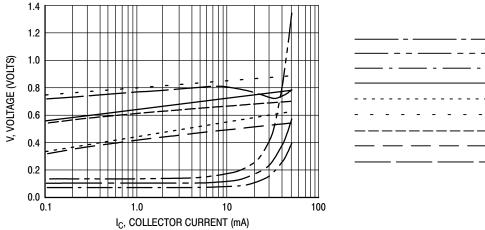
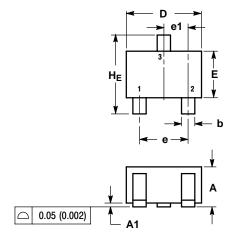
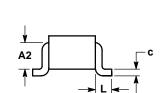


Figure 3. "ON" Voltages

PACKAGE DIMENSIONS

SC-70 (SOT-323) CASE 419-04 ISSUE M





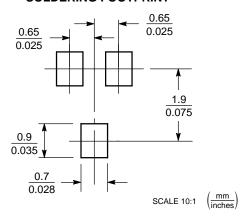
NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI
- 2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
Α	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2	0.7 REF			0.028 REF		
b	0.30	0.35	0.40	0.012	0.014	0.016
С	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.10	2.20	0.071	0.083	0.087
E	1.15	1.24	1.35	0.045	0.049	0.053
е	1.20	1.30	1.40	0.047	0.051	0.055
e1	0.65 BSC			0.026 BSC		
L	0.425 REF			0.017 REF		
HE	2.00	2.10	2.40	0.079	0.083	0.095

STYLE 3: PIN 1. BASE 2. EMITTER 3. COLLECTOR

SOLDERING FOOTPRINT*



*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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