Ordering number : ENN7488

PNP Epitaxial Planar Silicon Transistor

50A02MH

Low-Frequency General-Purpose Amplifier Applications

Applications

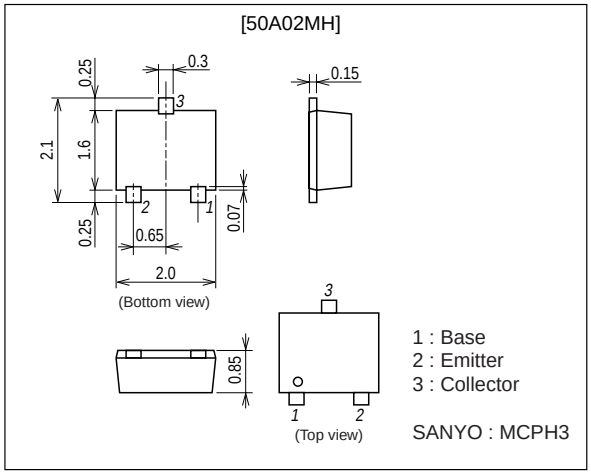
- Low-frequency Amplifier, high-speed switching, small motor drive, muting circuit.

Features

- Large current capacitance.
- Low collector-to-emitter saturation voltage (resistance). R_{CE}(sat) typ=210mΩ [I_C=0.5A, I_B=50mA].
- Small ON-resistance (Ron).

Package Dimensions

unit : mm
2194A



Specifications

Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	V_{CBO}		–50	V
Collector-to-Emitter Voltage	V_{CEO}		–50	V
Emitter-to-Base Voltage	V_{EBO}		–5	V
Collector Current	I_C		–500	mA
Collector Current (Pulse)	I_{CP}		–1.0	A
Collector Dissipation	P_C	Mounted on a ceramic board (600mm²×0.8mm)	600	mW
Junction Temperature	Tj		150	°C
Storage Temperature	Tstg		–55 to +150	°C

Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector Cutoff Current	I_{CBO}	V_{CB}=–40V, I_E=0			–100	nA
Emitter Cutoff Current	I_{EBO}	V_{EB}=–4V, I_C=0			–100	nA
DC Current Gain	h_{FE}	V_{CE}=–2V, I_C=–10mA	200		500	
Gain-Bandwidth Product	f_T	V_{CE}=–10V, I_C=–50mA		690		MHz
Output Capacitance	Cob	V_{CB}=–10V, f=1MHz		3.8		pF
Collector-to-Emitter Saturation Voltage	V_{CE}(sat)	I_C=–100mA, I_B=–10mA		–60	–120	mV
Base-to-Emitter Saturation Voltage	V_{BE}(sat)	I_C=–100mA, I_B=–10mA		–0.9	–1.2	V

Marking : AM

Continued on next page.

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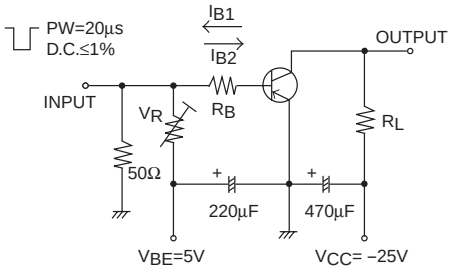
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

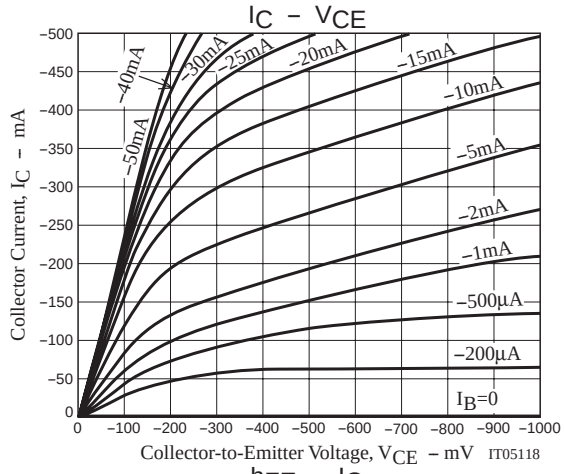
Continued from preceding page.

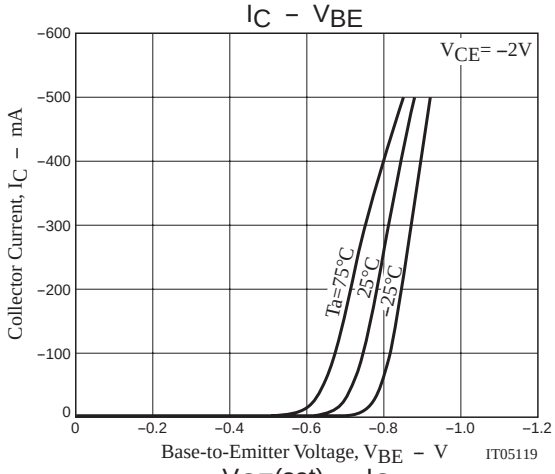
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=–10μA, I_E=0	–50			V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=–1mA, R_{BE}=∞	–50			V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E=–10μA, I_C=0	–5			V
Turn-ON Time	t_{on}	See specified Test Circuit.		30		ns
Storage Time	t_{stg}	See specified Test Circuit.		170		ns
Fall Time	t_f	See specified Test Circuit.		30		ns

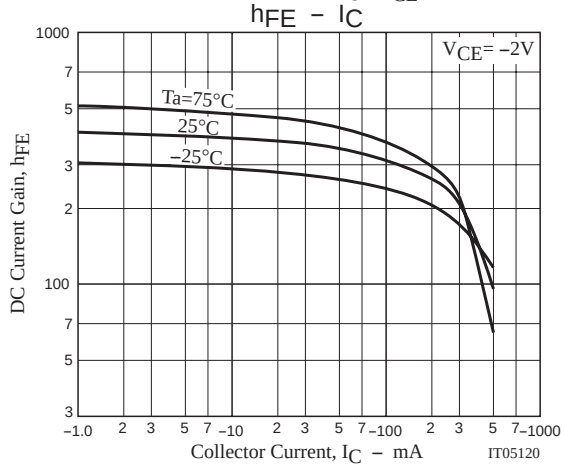
Switching Time Test Circuit

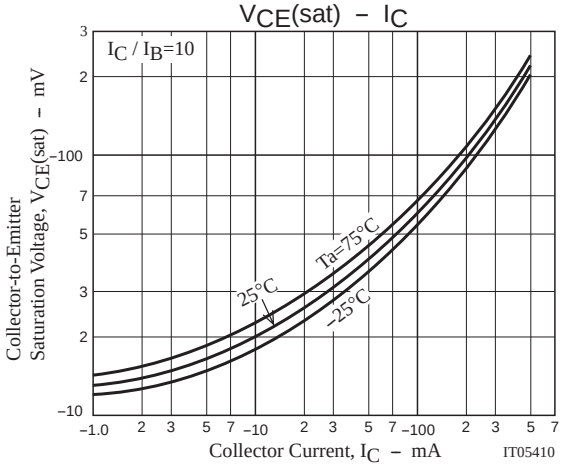


I_C=20I_{B1}= –20I_{B2}= –200mA

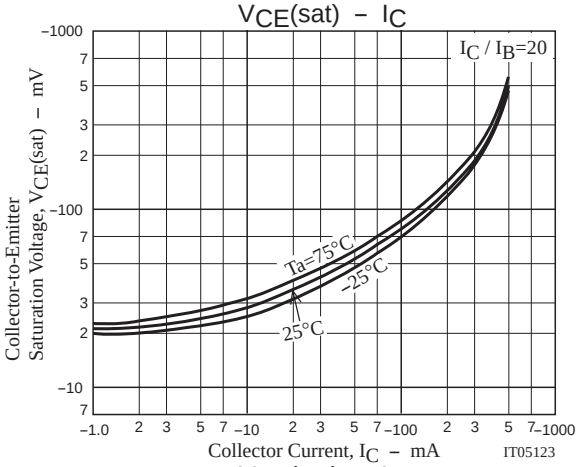




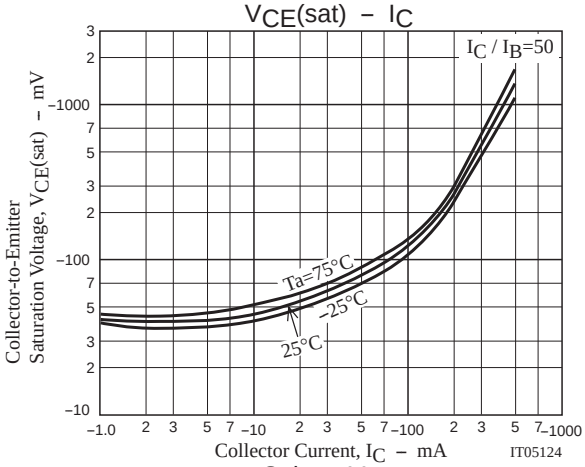




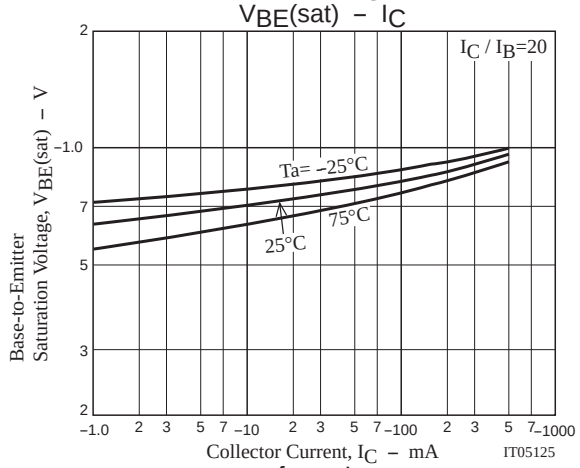
$V_{CE}(sat)$ – I_C



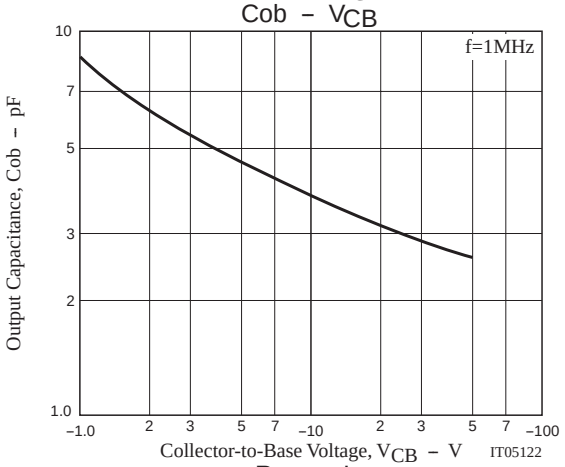
$V_{CE}(sat)$ – I_C



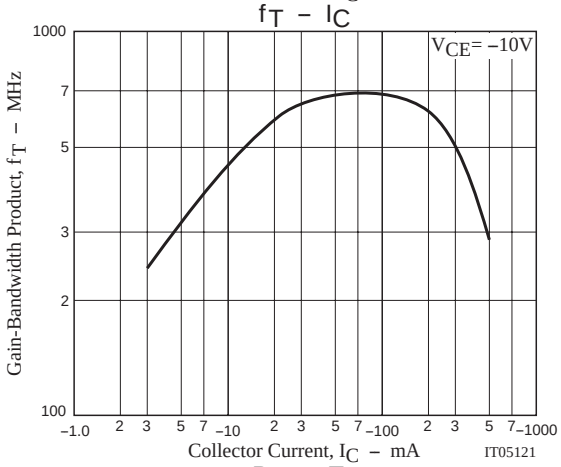
$V_{BE}(sat)$ – I_C



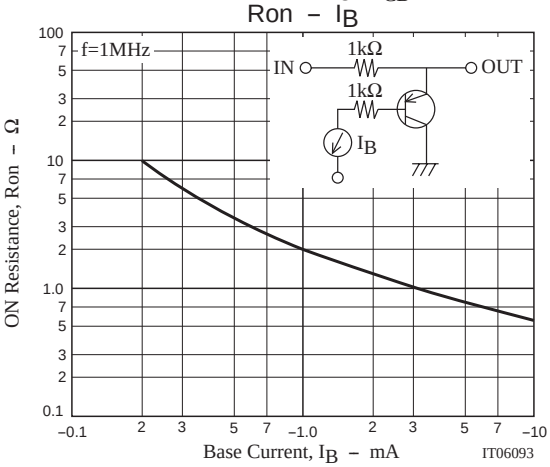
Cob – V_{CB}



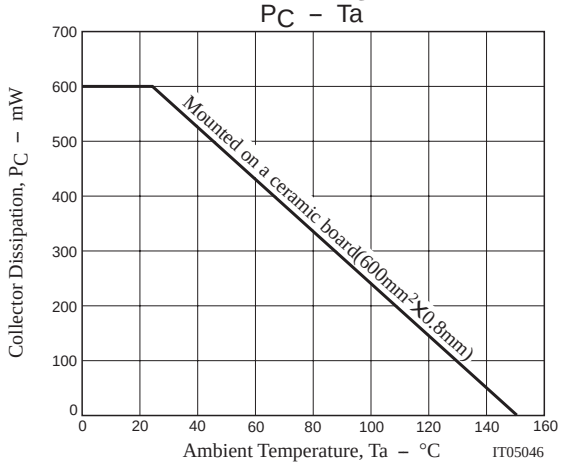
f_T – I_C



Ron – I_B



P_C – Ta



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