

# BUB323Z

## NPN Silicon Power Darlington

### High Voltage Autoprotected D<sup>2</sup>PAK for Surface Mount

The BUB323Z is a planar, monolithic, high-voltage power Darlington with a built-in active zener clamping circuit. This device is specifically designed for unclamped, inductive applications such as Electronic Ignition, Switching Regulators and Motor Control, and exhibit the following main features:

- Integrated High-Voltage Active Clamp
- Tight Clamping Voltage Window (350 V to 450 V) Guaranteed Over the -40°C to +125°C Temperature Range
- Clamping Energy Capability 100% Tested in a Live Ignition Circuit
- High DC Current Gain/Low Saturation Voltages Specified Over Full Temperature Range
- Design Guarantees Operation in SOA at All Times

#### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Sustaining Voltage	$V_{CEO}$	350	Vdc
Collector-Emitter Voltage	$V_{EBO}$	6.0	Vdc
Collector Current – Continuous	$I_C$	10	Adc
– Peak	$I_{CM}$	20	
Base Current – Continuous	$I_B$	3.0	Adc
– Peak	$I_{BM}$	6.0	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	$P_D$	150 1.0	Watts W/°C
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +175	°C

#### THERMAL CHARACTERISTICS

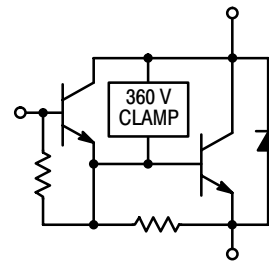
Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 5 Seconds	$T_L$	260	°C



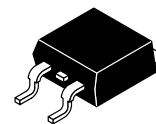
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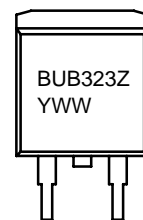
**AUTOPROTECTED  
DARLINGTON  
10 AMPERES  
360–450 VOLTS CLAMP  
150 WATTS**



#### MARKING DIAGRAM



**D<sup>2</sup>PAK  
CASE 418B  
STYLE 1**



BUB323Z = Specific Device Code  
Y = Year  
WW = Work Week

#### ORDERING INFORMATION

Device	Package	Shipping
BUB323Z	D <sup>2</sup> PAK	50 Units/Rail
BUB323ZT4	D <sup>2</sup> PAK	800/Tape & Reel

# BUB323Z

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b> (Note 1.)					
Collector–Emitter Clamping Voltage ( $I_C = 7.0\text{ A}$ ) ( $T_C = -40^\circ\text{C}$ to $+125^\circ\text{C}$ )	$V_{\text{CLAMP}}$	350	–	450	Vdc
Collector–Emitter Cutoff Current ( $V_{\text{CE}} = 200\text{ V}$ , $I_B = 0$ )	$I_{\text{CEO}}$	–	–	100	$\mu\text{Adc}$
Emitter–Base Leakage Current ( $V_{\text{EB}} = 6.0\text{ Vdc}$ , $I_C = 0$ )	$I_{\text{EBO}}$	–	–	50	$\text{mAdc}$

## ON CHARACTERISTICS (Note 1.)

Base–Emitter Saturation Voltage ( $I_C = 8.0\text{ Adc}$ , $I_B = 100\text{ mAdc}$ ) ( $I_C = 10\text{ Adc}$ , $I_B = 0.25\text{ Adc}$ )	$V_{\text{BE(sat)}}$	– –	– –	2.2 2.5	Vdc
Collector–Emitter Saturation Voltage ( $I_C = 7.0\text{ Adc}$ , $I_B = 70\text{ mAdc}$ )  ( $I_C = 8.0\text{ Adc}$ , $I_B = 0.1\text{ Adc}$ )  ( $I_C = 10\text{ Adc}$ , $I_B = 0.25\text{ Adc}$ )	$V_{\text{CE(sat)}}$	– – – –	– – – –	1.6 1.8 1.8 2.1 1.7	Vdc
Base–Emitter On Voltage ( $I_C = 5.0\text{ Adc}$ , $V_{\text{CE}} = 2.0\text{ Vdc}$ ) ( $I_C = 8.0\text{ Adc}$ , $V_{\text{CE}} = 2.0\text{ Vdc}$ )	$V_{\text{BE(on)}}$	1.1 1.3	– –	2.1 2.3	Vdc
Diode Forward Voltage Drop ( $I_F = 10\text{ Adc}$ )	$V_F$	–	–	2.5	Vdc
DC Current Gain ( $I_C = 6.5\text{ Adc}$ , $V_{\text{CE}} = 1.5\text{ Vdc}$ ) ( $I_C = 5.0\text{ Adc}$ , $V_{\text{CE}} = 4.6\text{ Vdc}$ )	$h_{\text{FE}}$	150 500	– –	– 3400	–

## DYNAMIC CHARACTERISTICS

Current Gain Bandwidth ( $I_C = 0.2\text{ Adc}$ , $V_{\text{CE}} = 10\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )	$f_T$	–	–	2.0	MHz
Output Capacitance ( $V_{\text{CB}} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 1.0\text{ MHz}$ )	$C_{\text{ob}}$	–	–	200	pF
Input Capacitance ( $V_{\text{EB}} = 6.0\text{ V}$ )	$C_{\text{ib}}$	–	–	550	pF

## CLAMPING ENERGY (see notes)

Repetitive Non–Destructive Energy Dissipated at turn–off: ( $I_C = 7.0\text{ A}$ , $L = 8.0\text{ mH}$ , $R_{\text{BE}} = 100\ \Omega$ ) (see Figures 2 and 4)	$W_{\text{CLAMP}}$	200	–	–	mJ
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## SWITCHING CHARACTERISTICS: Inductive Load ( $L = 10\text{ mH}$ )

Fall Time	$(I_C = 6.5\text{ A}$ , $I_{\text{B1}} = 45\text{ mA}$ , $V_{\text{BE(off)}} = 0$ , $R_{\text{BE(off)}} = 0$ , $V_{\text{CC}} = 14\text{ V}$ , $V_Z = 300\text{ V}$ )	$t_{\text{fi}}$	–	625	–	ns
Storage Time		$t_{\text{si}}$	–	10	30	$\mu\text{s}$
Cross–over Time		$t_c$	–	1.7	–	$\mu\text{s}$

1. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle = 2.0%.

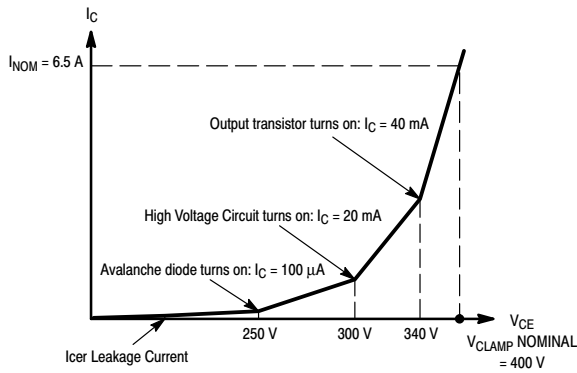


Figure 1.  $I_C = f(V_{CE})$  Curve Shape

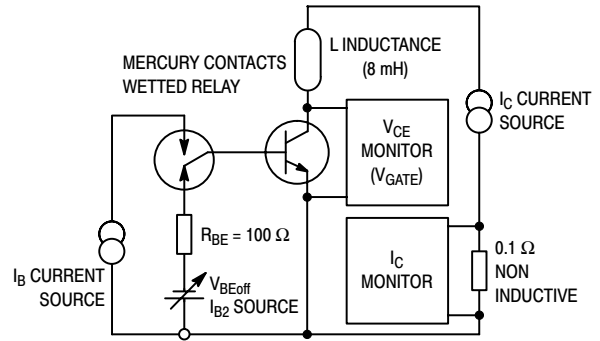


Figure 2. Basic Energy Test Circuit

By design, the BU323Z has a built-in avalanche diode and a special high voltage driving circuit. During an auto-protect cycle, the transistor is turned on again as soon as a voltage, determined by the zener threshold and the network, is reached. This prevents the transistor from going into a Reverse Bias Operating limit condition. Therefore, the device will have an extended safe operating area and will always appear to be in "FBSOA." Because of the built-in zener and associated network, the  $I_C = f(V_{CE})$  curve exhibits an unfamiliar shape compared to standard products as shown in Figure 1. .

The bias parameters,  $V_{CLAMP}$ ,  $I_{B1}$ ,  $V_{BE(off)}$ ,  $I_{B2}$ ,  $I_C$ , and the inductance, are applied according to the Device Under Test (DUT) specifications.  $V_{CE}$  and  $I_C$  are monitored by the test system while making sure the load line remains within the limits as described in Figure 4. .

Note: All BU323Z ignition devices are 100% energy tested, per the test circuit and criteria described in Figures 2. and 4. , to the minimum guaranteed repetitive energy, as specified in the device parameter section. The device can sustain this energy on a repetitive basis without degrading any of the specified electrical characteristics of the devices. The units under test are kept functional during the complete test sequence for the test conditions described:

$I_{C(peak)} = 7.0 \text{ A}$ ,  $I_{CH} = 5.0 \text{ A}$ ,  $I_{CL} = 100 \text{ mA}$ ,  $I_B = 100 \text{ mA}$ ,  $R_{BE} = 100 \text{ } \Omega$ ,  $V_{gate} = 280 \text{ V}$ ,  $L = 8.0 \text{ mH}$

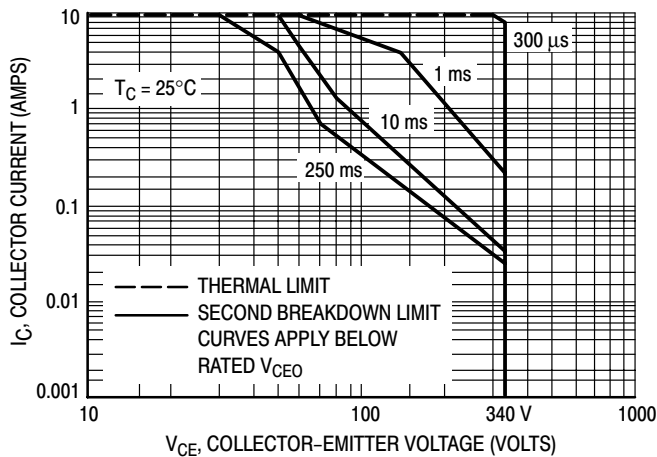
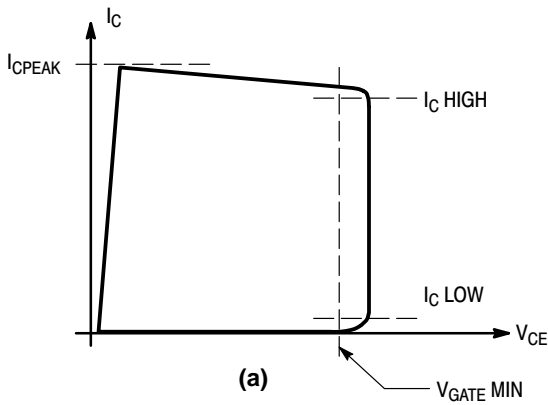
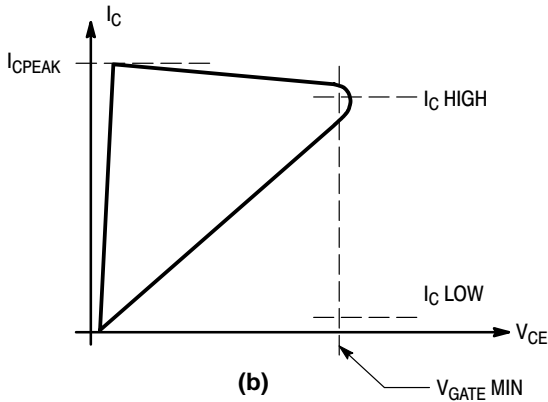


Figure 3. Forward Bias Safe Operating Area

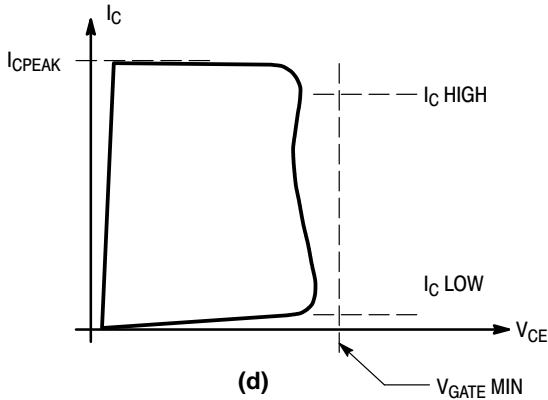
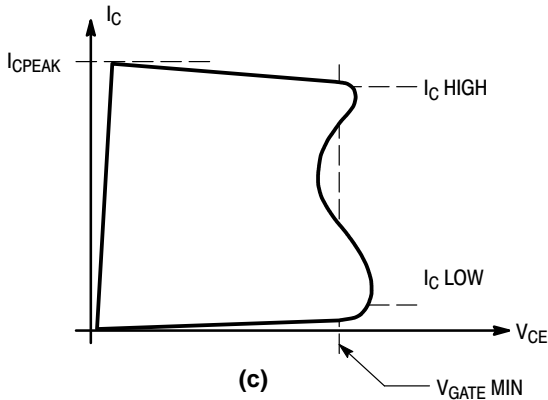


The shaded area represents the amount of energy the device can sustain, under given DC biases ( $I_C/I_B/V_{BE(off)}/R_{BE}$ ), without an external clamp; see the test schematic diagram, Figure 2. .

The transistor **PASSES** the Energy test if, for the inductive load and  $I_{CPEAK}/I_B/V_{BE(off)}$  biases, the  $V_{CE}$  remains outside the shaded area and greater than the  $V_{GATE}$  minimum limit, Figure 4. a.



The transistor **FAILS** if the  $V_{CE}$  is less than the  $V_{GATE}$  (minimum limit) at any point along the  $V_{CE}/I_C$  curve as shown on Figures 4. b, and 4. c. This assures that hot spots and uncontrolled avalanche are not being generated in the die, and the transistor is not damaged, thus enabling the sustained energy level required.



The transistor **FAILS** if its Collector/Emitter breakdown voltage is less than the  $V_{GATE}$  value, Figure 4. d.

Figure 4. Energy Test Criteria for BU323Z

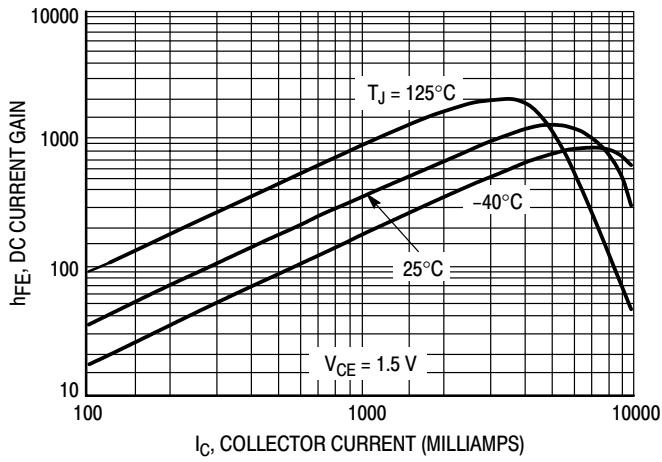


Figure 5. DC Current Gain

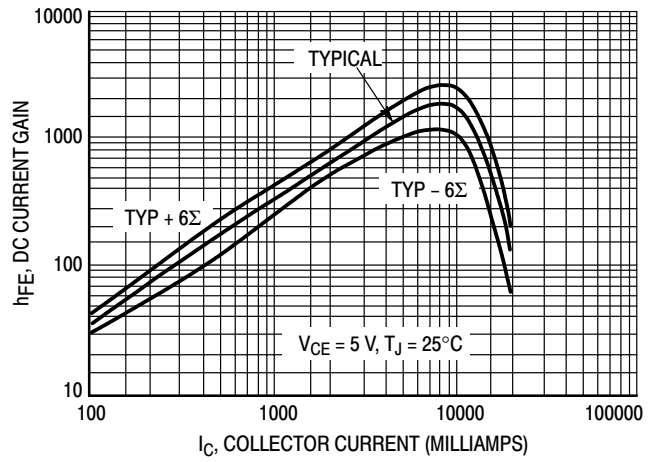


Figure 6. DC Current Gain

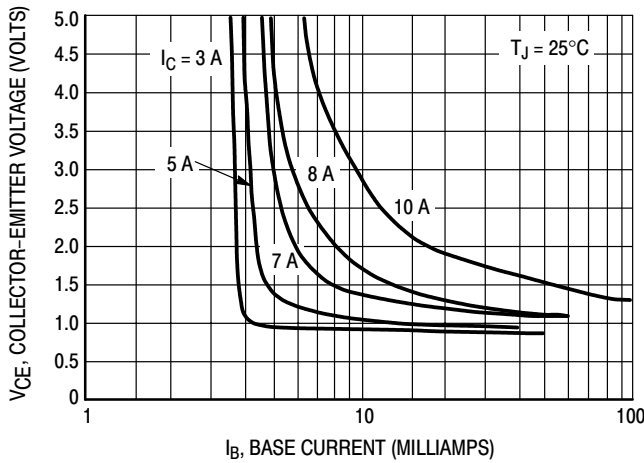


Figure 7. Collector Saturation Region

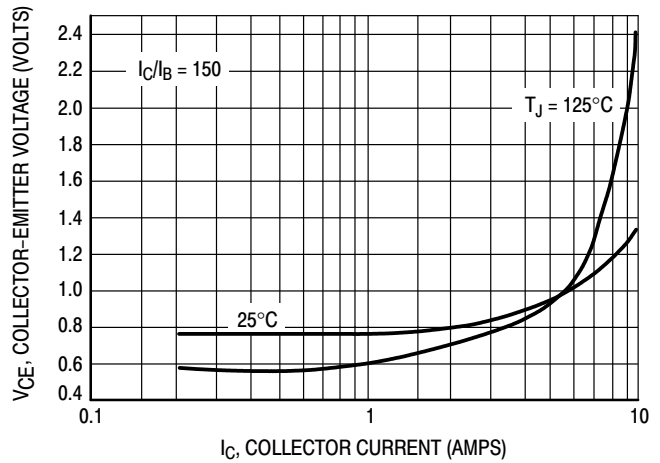


Figure 8. Collector–Emitter Saturation Voltage

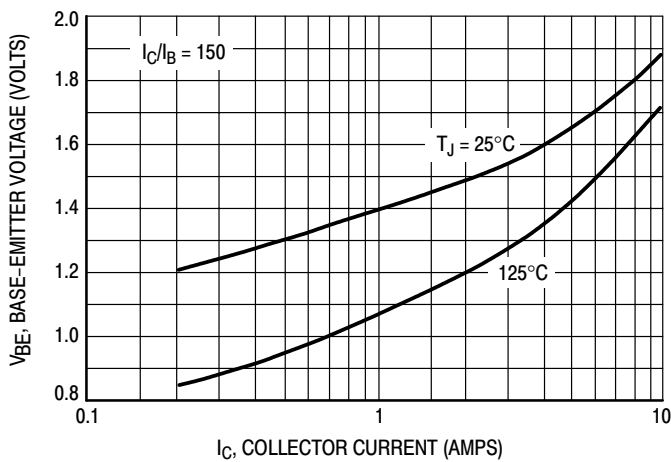


Figure 9. Base–Emitter Saturation Voltage

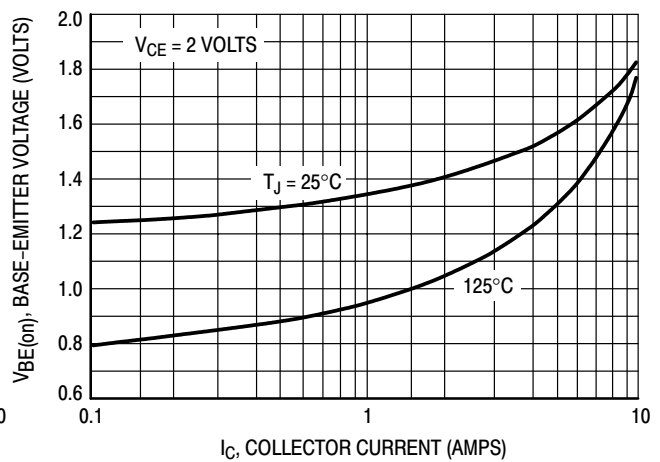


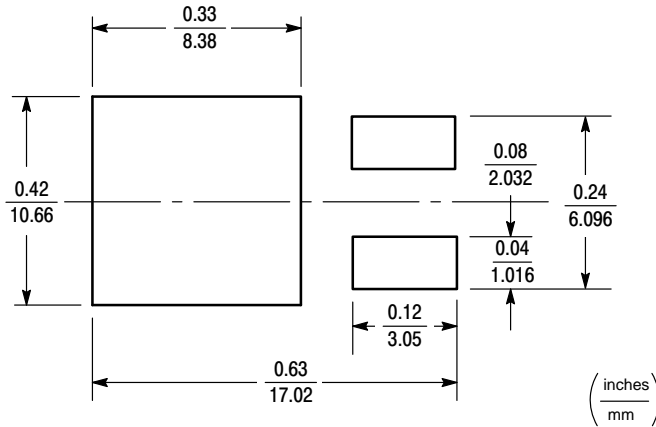
Figure 10. Base–Emitter "ON" Voltages

INFORMATION FOR USING THE D<sup>2</sup>PAK SURFACE MOUNT PACKAGE

RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection

interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the Collector pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by  $T_{J(max)}$ , the maximum rated junction temperature of the die,  $R_{\theta JA}$ , the thermal resistance from the device junction to ambient, and the operating temperature,  $T_A$ . Using the values provided on the data sheet,  $P_D$  can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature  $T_A$  of 25°C, one can calculate the power dissipation of the device. For a D<sup>2</sup>PAK device,  $P_D$  is calculated as follows.

$$P_D = \frac{150^\circ\text{C} - 25^\circ\text{C}}{50^\circ\text{C/W}} = 2.5 \text{ Watts}$$

The 50°C/W for the D<sup>2</sup>PAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.5 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the Collector pad. By increasing the area of the collection pad, the power dissipation can be increased.

Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of  $R_{\theta JA}$  versus Collector pad area is shown in Figure 11.

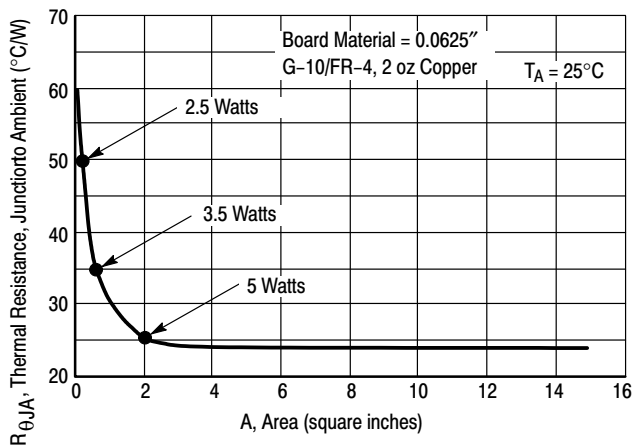


Figure 11. Thermal Resistance versus Collector Pad Area for the D<sup>2</sup>PAK Package (Typical)

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad<sup>®</sup>. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC-59, SC-70/SOT-323, SOD-123, SOT-23, SOT-143, SOT-223, SO-8, SO-14, SO-16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and D<sup>2</sup>PAK packages. If one uses a 1:1 opening to screen solder onto the Collector pad, misalignment and/or “tombstoning” may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 12. shows a

typical stencil for the DPAK and D<sup>2</sup>PAK packages. The pattern of the opening in the stencil for the Collector pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

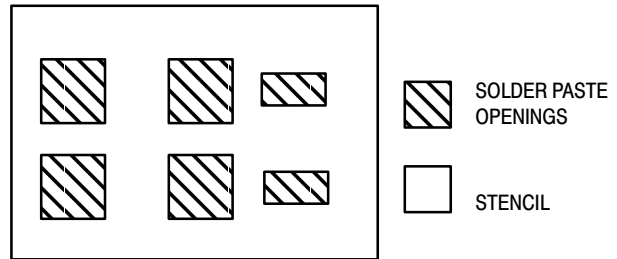


Figure 12. Typical Stencil for DPAK and D<sup>2</sup>PAK Packages

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.\*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.

- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

\* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

\* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the D<sup>2</sup>PAK is not recommended for wave soldering.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 13. shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time.

The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

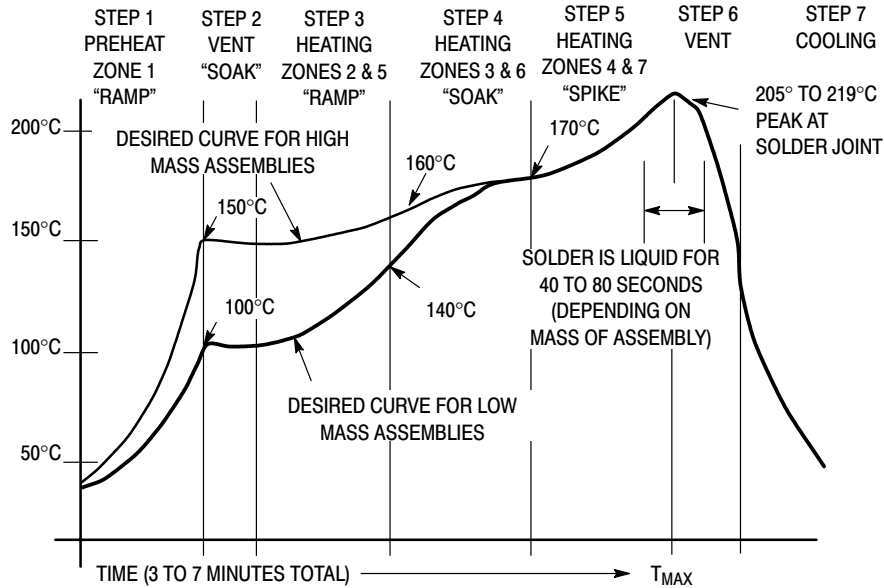


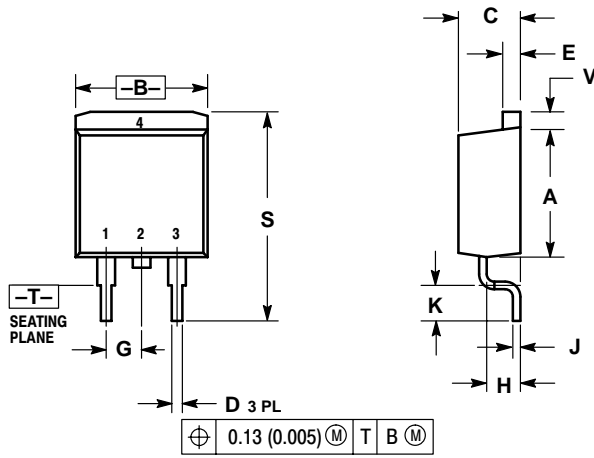
Figure 13. Typical Solder Heating Profile



# BUB323Z

## PACKAGE DIMENSIONS

D<sup>2</sup>PAK  
CASE 418B-03  
ISSUE D



- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

- STYLE 1:  
PIN 1. BASE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR

# Notes

# Notes

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