Driver for segmented LCD module with key input function

BU9768AK / BU9768AKV

The BU9768AK / BU9768AKV are man-machine interface ICs with key input, designed for portable multimedia terminals and other devices. They can be used as drivers for operation mode display LCD panels on portable terminals, household products, car stereos, and other appliances. Up to 126 cells can be displayed, and up to 30 keys can be input.
Also, a maximum of four outputs are possible using expansion pins. (The number of outputs for each pin can be changed using control codes.)

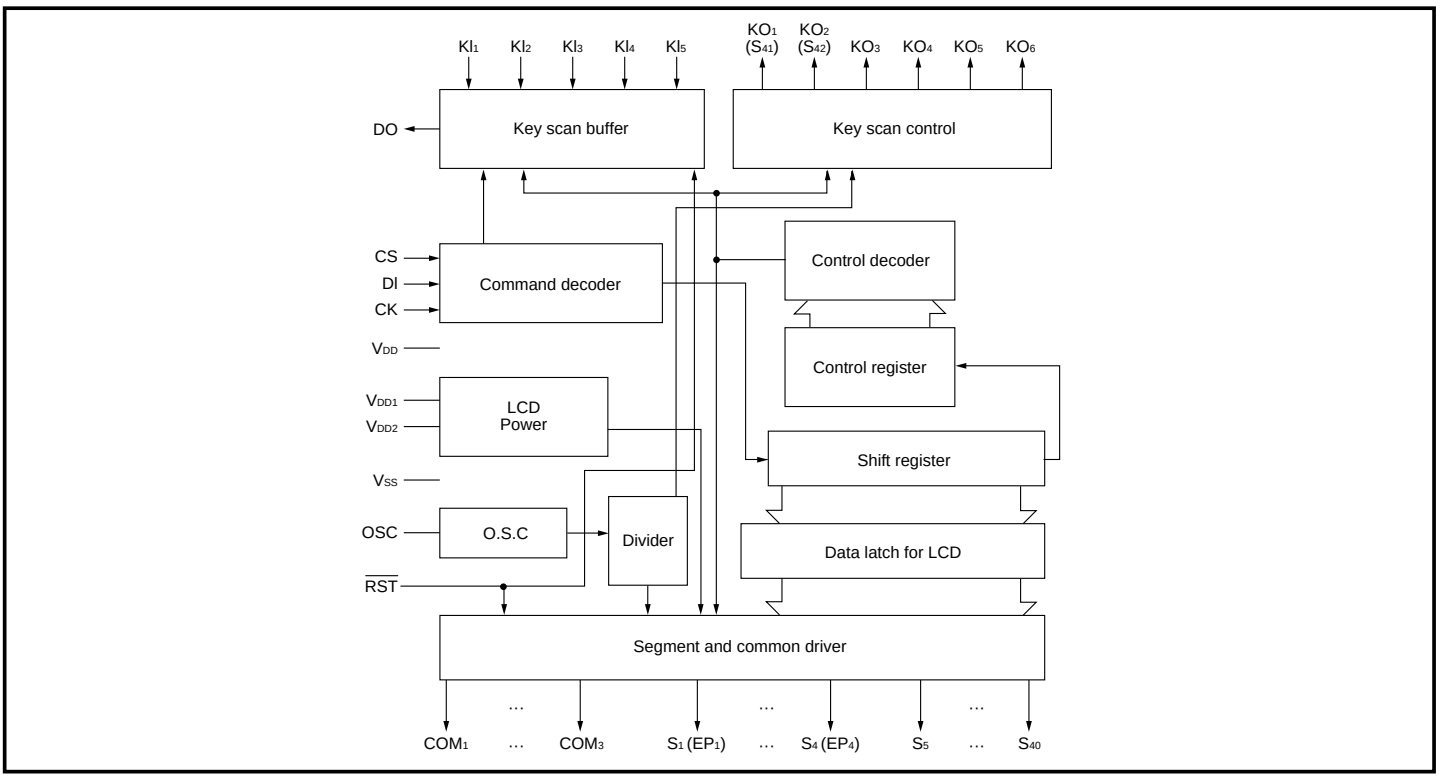
●Applications

Portable multi-media terminals, POS terminals, wireless radios, telephones, cameras, VCRs, movie projectors, car stereos, others

●Features

1) Drive of up to 42 segment outputs, three common outputs, and up to 126 cells is possible.
2) Up to 30 keys can be input.
3) A maximum of four pins can be used as output pins for expansion.
4) 1 / 3 duty drive.
5) A bias of 1 / 2 or 1 / 3 can be selected for the LCD display power supply.

●Block diagram



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●Pin assignments

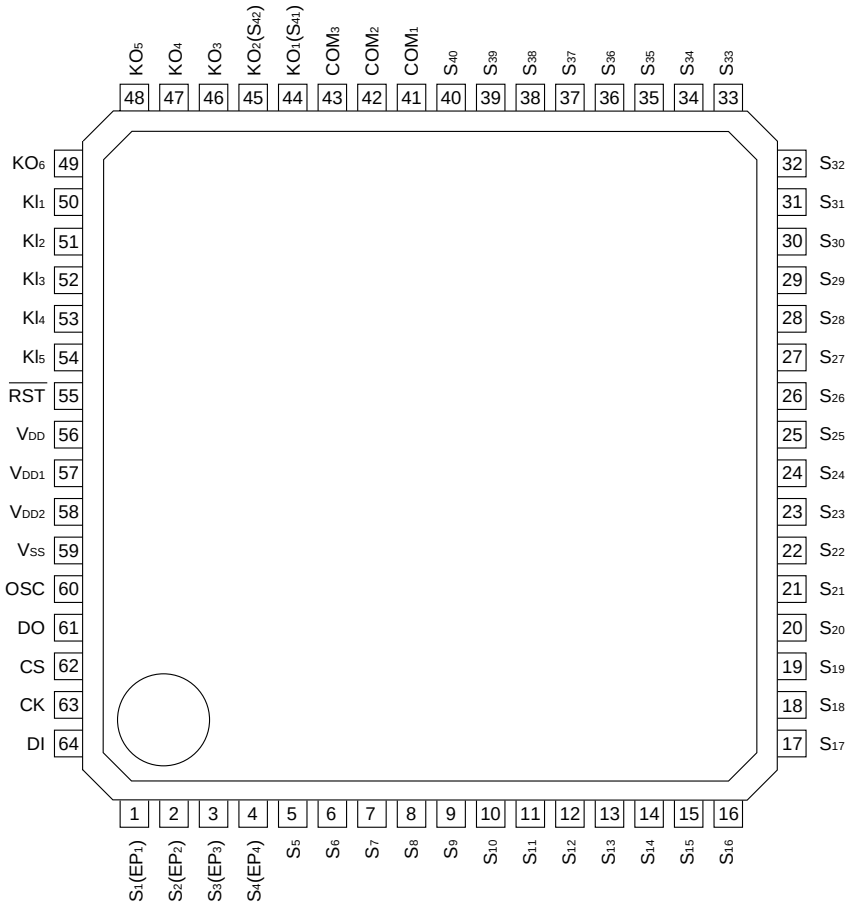

Fig.1

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●Pin descriptions

Pin No.	Pin name	I / O	Function	Processing if not used
1 ~ 4	S_1 (EP_1) ~ S_4 (EP_4)	O	Output pins for switching between segment output and expansion pin output. Switched using control codes P_0 and P_1. When expansion pins are used, these output set data (1 or 0).	OPEN
5 ~ 40	S_5 ~ S_{40}	O	Segment output pins. These output waveforms correspond to serial data input from DI.	OPEN
41 ~ 43	COM_1 ~ COM_3	O	Common output pins	OPEN
44, 45	KO_1 (S_{41}), KO_2 (S_{42})	O	Output pins for switching between key scan output and segment output. Switching is enabled using control codes K_0 and K_1.	OPEN
46 ~ 49	KO_3 ~ KO_6	O	Key scan output pins	OPEN
50 ~ 54	KI_1 ~ KI_5	I	Key scan input pins	OPEN
55	$\overline{RST}$	I	Reset input pin for Low Active state. Segment and common outputs are fixed at LOW level while $\overline{RST}$ is LOW, and all displays disappear. Data for LCD displays is not reset. All data in the key scan buffer is cleared.	V_{DD}
57	$V_{DD}1$	—	Internal reference voltage for LCD. When using in the 1 / 2 bias mode, this should be connected to V_{DD2}.	—
58	$V_{DD}2$	—	Internal reference voltage for LCD. When using in the 1 / 2 bias mode, this should be connected to V_{DD1}.	—
60	OSC	—	Oscillator pin for segment / common alternating waveforms	—
61	DO	O	Key buffer data output pin. After a key scan has been completed, if key input existed, this changes to LOW. Also, if the key data communications command is input, the contents of the key buffer are output as serial data. Since this is open drain output, it should be used with a pull-up resistor.	OPEN
62	CS	I	Chip select input pin	V_{SS}
63	CK	I	Synchronous clock input pin for data transmission	V_{SS}
64	DI	I	Data input pin for LCD display	V_{SS}

●Absolute maximum ratings (Ta = 25°C)

Parameter		Symbol	Pin	Limits	Unit
Power supply voltage		V_{DD}	V_{DD}	– 0.3 ~ + 7.0	V
Input voltage		V_{IN}	$\overline{RST}$, OSC, CS, CK, DI, KI_1 ~ KI_5	– 0.3 ~ V_{DD} + 0.3	V
Output voltage		V_{OUT}	OSC, DO, KO_1 ~ KO_6, EP_1 ~ EP_4	– 0.3 ~ V_{DD} + 0.3	V
Output current		I_{OUT} (1)	COM_1 ~ COM_3	3	mA
		I_{OUT} (2)	EP_1 ~ EP_4	5	mA
		I_{OUT} (3)	S_1 ~ S_{40}	300	µA
		I_{OUT} (4)	KO_1 ~ KO_6	1	mA
Power dissipation	BU9768AK	P_d	—	800	mW*
	BU9768AKV			750	
Storage temperature		T_{stg}	—	– 55 ~ + 125	°C

* This is the maximum voltage which may be applied to the V_{SS} pin.
Reduced by 8.0mW (AK) or 7.5mW (AKV) for each increase in Ta of 1°C over 25°C.

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●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Pin	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	V_{DD}	+ 4.5	—	+ 6.0	V
Operating temperature	Topr	—	– 40	—	+ 85	°C

●Electrical characteristics (unless otherwise noted, V_{DD} = 4.5V to 6.0V, Ta = 25°C)

Parameter	Symbol	Pin	Min.	Typ.	Max.	Unit	Conditions
Input high level voltage	V_{IH} (1)	$\overline{RST}$, CS, CK, DI	0.8V_{DD}	—	V_{DD}	V	
	V_{IH} (2)	KI_1 ~ KI_5	0.6V_{DD}	—	V_{DD}	V	
Input low level voltage	V_{IL} (1)	$\overline{RST}$, CS ,CK, DI	0	—	0.2V_{DD}	V	
	V_{IL} (2)	KI_1 ~ KI_5	0	—	0.2V_{DD}	V	
Input high level current	I_{IH}	$\overline{RST}$, CS, CK, DI	—	—	6.0	µA	$V_1 = V_{DD}$
Input low level current	I_{IL}	$\overline{RST}$, CS, CK, DI	—	—	6.0	µA	$V_1 = V_{SS}$
Input floating voltage	V_{IF}	KI_1 ~ KI_5	—	—	0.05V_{DD}	V	
Pull-down resistance	R_{PD}	KI_1 ~ KI_5	50	100	200	kΩ	V_{DD} = 5.0V
Output off leakage current	I_{OFFH}	DO	—	—	6.0	µA	$V_O = V_{DD}$
Output high level voltage	V_{OH} (1)	KO_1 ~ KO_6	V_{DD} – 2.0	V_{DD} – 1.0	V_{DD} – 0.5	V	I_O = – 1mA
	V_{OH} (2)	EP_1 ~ EP_4	V_{DD} – 1.5	—	—	V	I_O = – 300µA
	V_{OH} (3)	S_1 ~ S_{42}	—	V_{DD} – 1.0	—	V	I_O = – 20µA
	V_{OH} (4)	COM_1 ~ COM_3	—	V_{DD} – 1.0	—	V	I_O = – 100µA
Output low level voltage	V_{OL} (1)	KO_1 ~ KO_6	0.5	1.0	2.0	V	I_O = 50µA
	V_{OL} (2)	EP_1 ~ EP_4	—	—	1.0	V	I_O = 300µA
	V_{OL} (3)	S_1 ~ S_{42}	—	1.0	—	V	I_O = 20µA
	V_{OL} (4)	COM_1 ~ COM_3	—	1.0	—	V	I_O = 100µA
	V_{OL} (5)	DO	—	0.2 (200Ω)	0.5 (500Ω)	V	I_O = 1mA
Output intermediate level voltage	V_{MID} (1)	COM_1 ~ COM_3	1 / 2V_{DD} – 1.0	—	1 / 2V_{DD} + 1.0	V	1 / 2bias
	V_{MID} (2)	S_1 ~ S_{42}	2 / 3V_{DD} – 1.0	—	2 / 3V_{DD} + 1.0	V	1 / 3bias
	V_{MID} (3)	COM_1 ~ COM_3	2 / 3V_{DD} – 1.0	—	2 / 3V_{DD} + 1.0	V	1 / 3bias
	V_{MID} (4)	S_1 ~ S_{42}	1 / 3V_{DD} – 1.0	—	1 / 3V_{DD} + 1.0	V	1 / 3bias
	V_{MID} (5)	COM_1 ~ COM_3	1 / 3V_{DD} – 1.0	—	1 / 3V_{DD} + 1.0	V	1 / 3bias
Power supply current	I_{DD1}	—	—	30	70	µA	In sleep mode
	I_{DD2}	—	—	200	500	µA	f_{OSC} = 38kHz

○ Not designed for radiation resistance.

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●AC timing characteristics (V_{DD} = 4.5V to 6.0V, Ta = 25°C)

Parameter	Symbol	Pin	Min.	Typ.	Max.	Unit	
Rise time	t_u	CS, CK, DI	—	—	300	ns	
Fall time	t_d	CS, CK, DI	—	—	300	ns	
Data setup time	t_s (1)	CK, DI	100	—	—	ns	
Data hold time	t_h (1)	CK, DI	100	—	—	ns	
CS wait time	t_{CW}	CS, CK	100	—	—	ns	
CS setup time	t_s (2)	CS, CK	100	—	—	ns	
CS hold time	t_h (2)	CS, CK	100	—	—	ns	
CK HIGH level time	t_H	CK	100	—	—	ns	
CK LOW level time	t_L	CK	100	—	—	ns	
D0 output delay time	t_{dl}	DO	—	—	200 (Note 1)	ns	
Oscillation guaranteed range	f_{OSC}	OSC	19	38	76	kHz	(Note 2)

(Note 1) Since DO is open drain output, the output delay time varies depending on the pull-up resistance.
(Note 2) Values measured for attachments of R = 47kΩ, C = 1000pF.

●Application example
(1 / 2 bias mode)

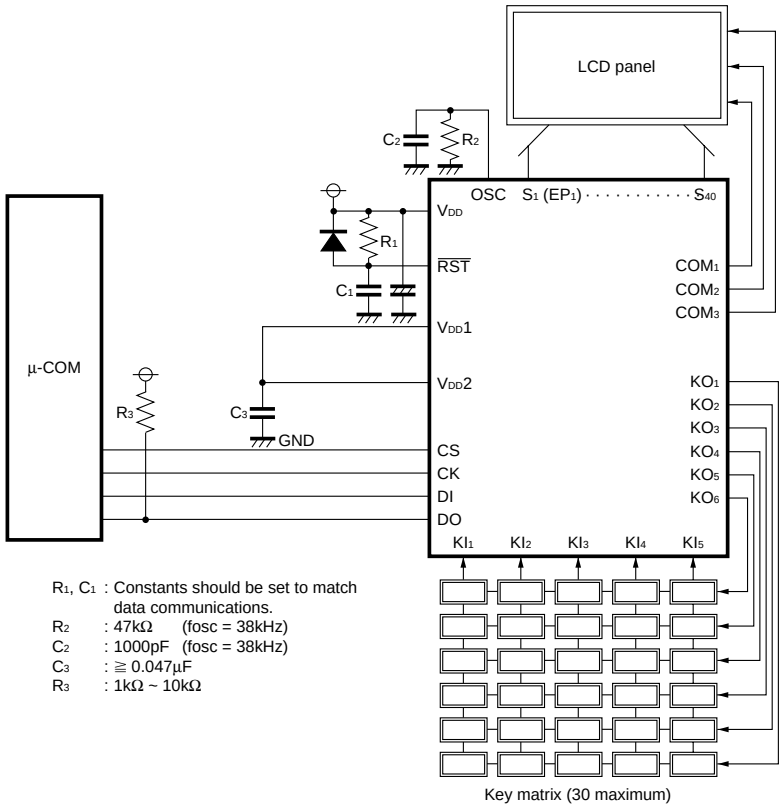

Fig. 2

∗ The pull-up resistor value should be set to a value so that the waveform is not destroyed by the wiring capacitance or other factors.

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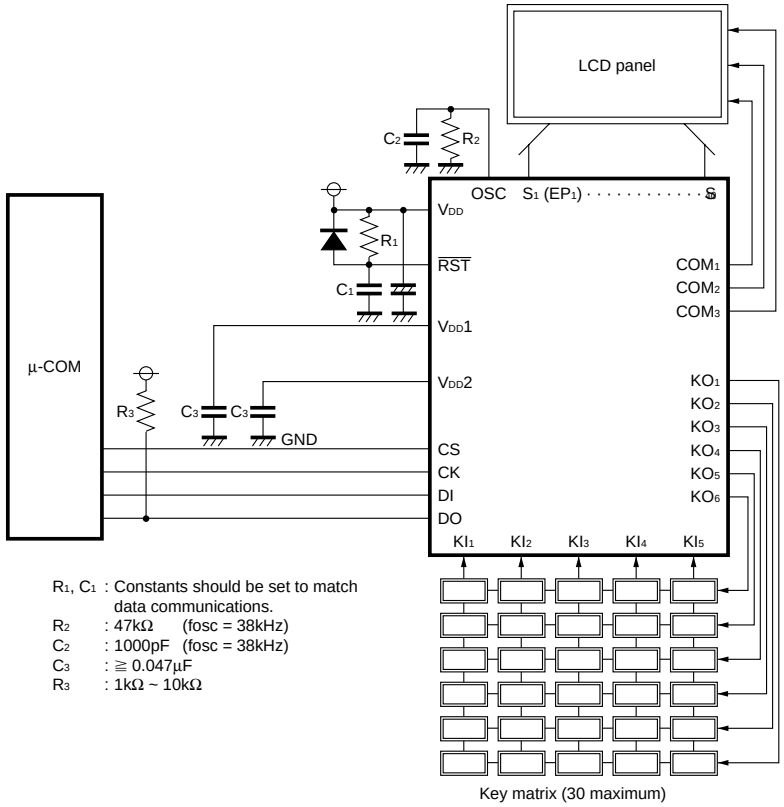
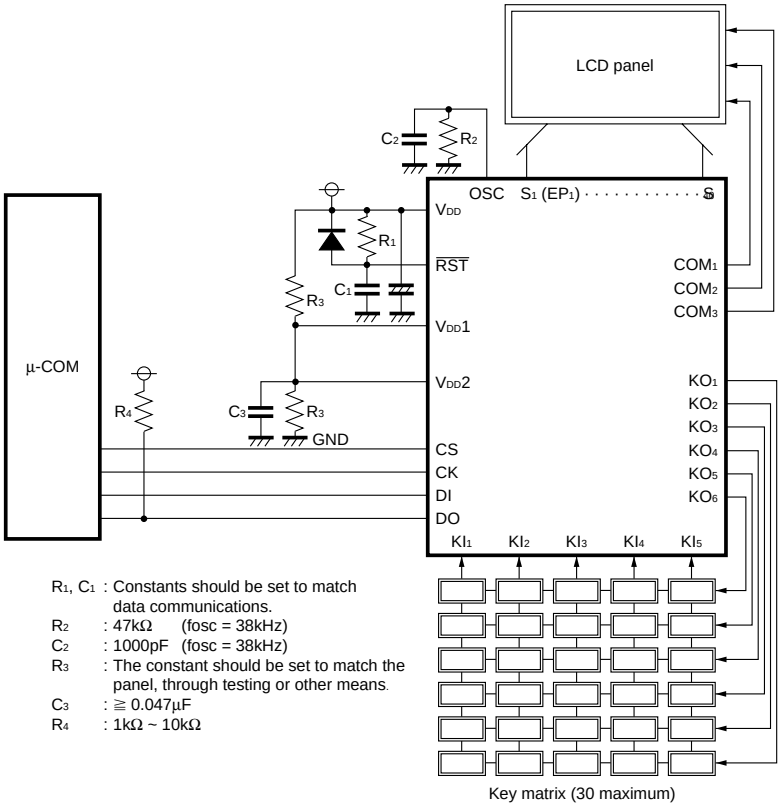
(1 / 3 bias mode)



R1, C1 : Constants should be set to match data communications.
R2 : 47kΩ (fosc = 38kHz)
C2 : 1000pF (fosc = 38kHz)
C3 : ≧ 0.047μF
R3 : 1kΩ ~ 10kΩ

Fig. 3

(1 / 2 bias mode)



R1, C1 : Constants should be set to match data communications.
R2 : 47kΩ (fosc = 38kHz)
C2 : 1000pF (fosc = 38kHz)
R3 : The constant should be set to match the panel, through testing or other means.
C3 : ≧ 0.047μF
R4 : 1kΩ ~ 10kΩ

Fig. 4

∗ The pull-up resistor value should be set to a value so that the waveform is not destroyed by the wiring capacitance or other factors.

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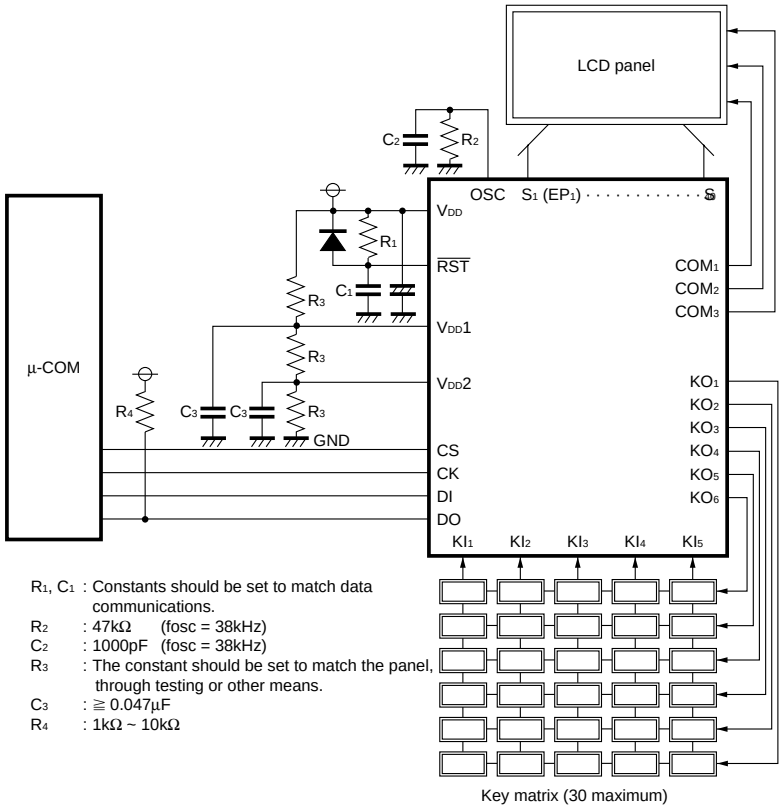
(1 / 3 bias mode)



R1, C1 : Constants should be set to match data communications.
R2 : 47kΩ (fosc = 38kHz)
C2 : 1000pF (fosc = 38kHz)
R3 : The constant should be set to match the panel, through testing or other means.
C3 : ≧ 0.047μF
R4 : 1kΩ ~ 10kΩ

Fig. 5

∗ The pull-up resistor value should be set to a value so that the waveform is not destroyed by the wiring capacitance or other factors.

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●Circuit operation

(1) Data communications

The BU9768AK / BU9768AKV are able to receive LCD display data output from the controller, as well as the results of key scans.

1) LCD display data output (from controller)

When LCD data is output, the command code “42” must be output at the beginning of the data. Fig. 6 shows an example of LCD display data output.

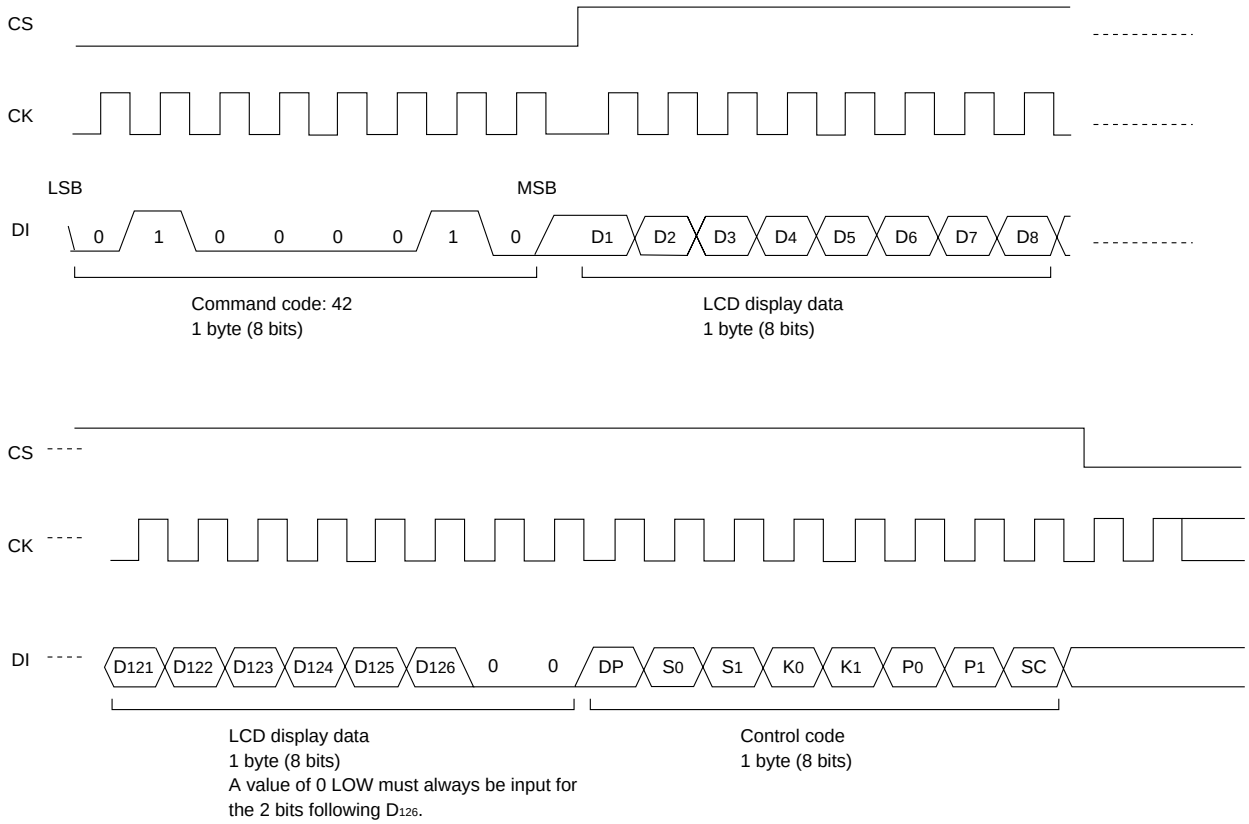

Fig. 6 Example of LCD display data transmission

① During the time that CS is LOW, the command code “42” is input synchronized to the CK clock, and CS is then set to HIGH before the rise of the next CK clock.

② The LCD data is sent, and 0 (LOW level) is input for the two bits following D_{126}.

③ An 8-bit control code is input, and CS is set to LOW.

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Segment data correspondence table

	COM_3	COM_2	COM_1
S_1 (EP_1)	D_1 (EP_1)	D_2	D_3
S_2 (EP_2)	D_4 (EP_2)	D_5	D_6
S_3 (EP_3)	D_7 (EP_3)	D_8	D_9
S_4 (EP_4)	D_{10} (EP_4)	D_{11}	D_{12}
S_5	D_{13}	D_{14}	D_{15}
S_6	D_{16}	D_{17}	D_{18}
S_7	D_{19}	D_{20}	D_{21}
S_8	D_{22}	D_{23}	D_{24}
S_9	D_{25}	D_{26}	D_{27}
S_{10}	D_{28}	D_{29}	D_{30}
S_{11}	D_{31}	D_{32}	D_{33}
S_{12}	D_{34}	D_{35}	D_{36}
S_{13}	D_{37}	D_{38}	D_{39}
S_{14}	D_{40}	D_{41}	D_{42}
S_{15}	D_{43}	D_{44}	D_{45}
S_{16}	D_{46}	D_{47}	D_{48}
S_{17}	D_{49}	D_{50}	D_{51}
S_{18}	D_{52}	D_{53}	D_{54}
S_{19}	D_{55}	D_{56}	D_{57}
S_{20}	D_{58}	D_{59}	D_{60}
S_{21}	D_{61}	D_{62}	D_{63}

	COM_3	COM_2	COM_1
S_{22}	D_{64}	D_{65}	D_{66}
S_{23}	D_{67}	D_{68}	D_{69}
S_{24}	D_{70}	D_{71}	D_{72}
S_{25}	D_{73}	D_{74}	D_{75}
S_{26}	D_{76}	D_{77}	D_{78}
S_{27}	D_{79}	D_{80}	D_{81}
S_{28}	D_{82}	D_{83}	D_{84}
S_{29}	D_{85}	D_{86}	D_{87}
S_{30}	D_{88}	D_{89}	D_{90}
S_{31}	D_{91}	D_{92}	D_{93}
S_{32}	D_{94}	D_{95}	D_{96}
S_{33}	D_{97}	D_{98}	D_{99}
S_{34}	D_{100}	D_{101}	D_{102}
S_{35}	D_{103}	D_{104}	D_{105}
S_{36}	D_{106}	D_{107}	D_{108}
S_{37}	D_{109}	D_{110}	D_{111}
S_{38}	D_{112}	D_{113}	D_{114}
S_{39}	D_{115}	D_{116}	D_{117}
S_{40}	D_{118}	D_{119}	D_{120}
KO_1 (S_{41})	D_{121}	D_{122}	D_{123}
KO_2 (S_{42})	D_{124}	D_{125}	D_{126}

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1. If there is an unused segment output

If there is segment output that is not used, depending on the panel, the transmission of the LCD display data can be simplified by deciding the pin or pins to be used starting from S_{40} (S_{42} if pins 44 and 45 are used as segment output, and S_{41} if only pin 44 is used as segment output).

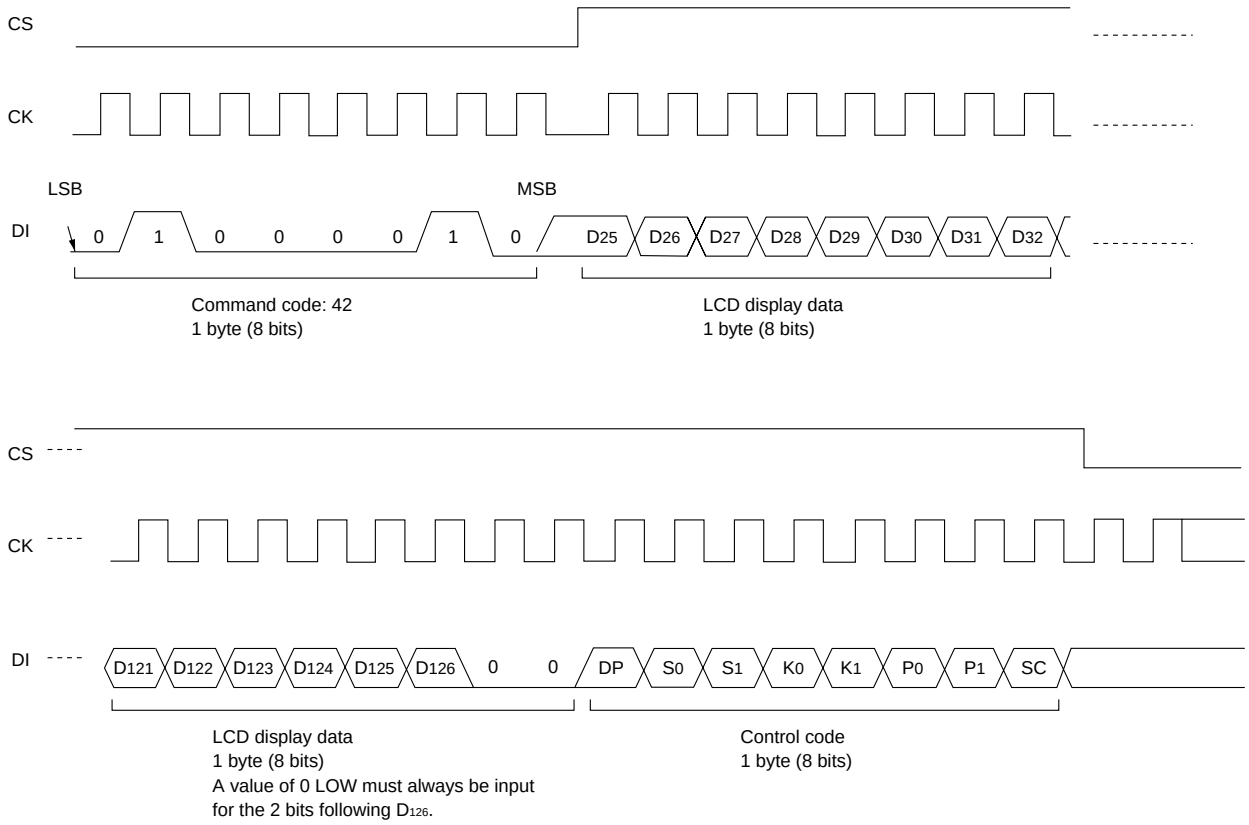

Fig. 7 Simplified data communication

This figure shows an example in which the 30 segment outputs from S_{11} to S_{40} are used, and assumes that communication is done in units of eight bits (one byte). For this reason, the data of S_9 and S_{10} (from D_{25} to D_{30}), which are not used, is input as dummy data. If the unit is not eight bits, this dummy data can be omitted, in which case the data should be input after the command code, starting from the data of D_{31}. However, even if Pins 44 and 45 are used as key scan output and not as segment output, the data for D_{121} to D_{126} cannot be omitted.

2. Control codes

The BU9768AK is designed to support various applications, depending on the combination of control codes used.

• DP: Display mode control

Depending on the type of display, either 1 / 2 bias drive or 1 / 3 bias drive may be selected.

1: 1 / 2 bias drive

0: 1 / 3 bias drive

• S_0 and S_1: Sleep mode control

In the sleep modes, all displays are turned off, and the oscillation of the OSC pin is stopped, enabling a lower power consumption. In sleep modes, although all of the displays are turned off, key scans are enabled. For information on key scans in the sleep modes, please refer to pages 15 to 22.

Various sleep modes can be selected, depending on the application.

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Control code		Mode	Segment / common output	OSC pin	Key scan output					
S_0	S_1				KO_1	KO_2	KO_3	KO_4	KO_5	KO_6
0	0	Normal	Output	Oscillating	H	H	H	H	H	H
0	1	Sleep	Fixed at LOW	Stopped	L	L	L	L	L	H
1	0	Sleep	Fixed at LOW	Stopped	L	L	L	L	H	H
1	1	Sleep	Fixed at LOW	Stopped	H	H	H	H	H	H

In the Sleep modes, oscillation of the OSC pin stops, but if a button is pressed while the key scan output is on the HIGH line, oscillation begins and a key scan is carried out. When the key scan has been completed, oscillation stops again.

- K_0, K_1: Control that switches between key scan and segment output
- P_0, P_1: Control that switches between segment and expansion pin output

The output can be switched to match a variety of applications, depending on the combination of the four bits.

Control code				Key scan / segment		Segment / expansion pin				Max. no. of display segments	Max. key input
K_0	K_1	P_0	P_1	44pin	45pin	1pin	2pin	3pin	4pin		
0	0	0	0	KO_1	KO_2	S_1	S_2	S_3	S_4	120	30
0	0	0	1	KO_1	KO_2	EP_1	EP_2	S_3	S_4	114	30
0	0	1	0	KO_1	KO_2	EP_1	EP_2	EP_3	S_4	111	30
0	0	1	1	KO_1	KO_2	EP_1	EP_2	EP_3	EP_4	108	30
0	1	0	0	S_{41}	KO_2	S_1	S_2	S_3	S_4	123	25
0	1	0	1	S_{41}	KO_2	EP_1	EP_2	S_3	S_4	117	25
0	1	1	0	S_{41}	KO_2	EP_1	EP_2	EP_3	S_4	114	25
0	1	1	1	S_{41}	KO_2	EP_1	EP_2	EP_3	EP_4	111	25
1	✻	0	0	S_{41}	S_{42}	S_1	S_2	S_3	S_4	126	20
1	✻	0	1	S_{41}	S_{42}	EP_1	EP_2	S_3	S_4	120	20
1	✻	1	0	S_{41}	S_{42}	EP_1	EP_2	EP_3	S_4	117	20
1	✻	1	1	S_{41}	S_{42}	EP_1	EP_2	EP_3	EP_4	114	20

✻ Don't Care

- SC: Control switching the LCD display on and off

  Switching the LCD display on and off can be done regardless of the input data.

  1: Display off

  0: Display on (when displayed, displays can be obtained in accordance with the input data.)

Note: When the power supply is turned on, the following settings are in effect for control codes. These initial settings for control codes should be changed to match the mode being used.

When the power supply is turned on:

(DP, S_0, S_1, K_0, K_1, P_0, P_1, SC) = (0, 0, 0, 1, 1, 0, 0, 0)

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2) Transmission of key data

A command code of “43” should be input in order to output the results of a key scan to the BU9768AK / BU9768AKV.

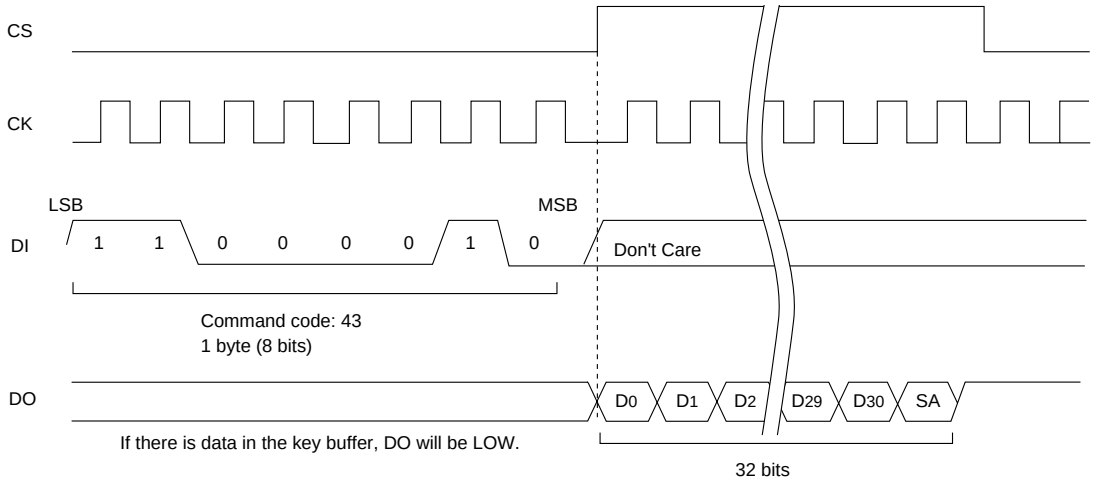

Fig. 8 Transmission of key data

If CS is changed to HIGH level after the command code is input, the data in the key buffer is output synchronized to the rise of CK.

Key data correspondence table

	KI_1	KI_2	KI_3	KI_4	KI_5
KO_1 (S_{41})	D_1	D_2	D_3	D_4	D_5
KO_2 (S_{42})	D_6	D_7	D_8	D_9	D_{10}
KO_3	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}
KO_4	D_{16}	D_{17}	D_{18}	D_{19}	D_{20}
KO_5	D_{21}	D_{22}	D_{23}	D_{24}	D_{25}
KO_6	D_{26}	D_{27}	D_{28}	D_{29}	D_{30}

- The data D_0, which is output synchronized to the rise of CS, is unstable and should not be used.
- The output SA of the 32nd bit is a state acknowledge signal and outputs the current BU9768AK / BU9768AKV mode.

SA: State acknowledge signal

In normal modes: SA = LOW

In sleep modes : SA = HIGH

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(2) Key scan operation

With the BU9768AK / BU9768AKV, up to 30 key inputs can be received.

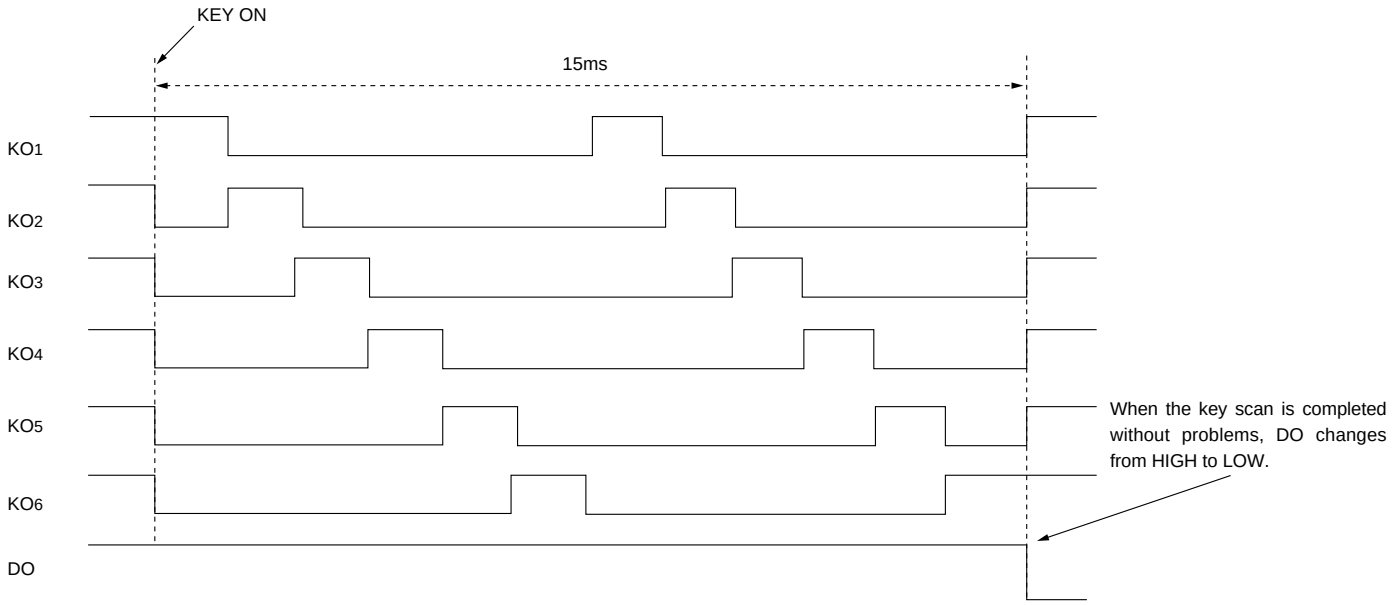

Fig. 9 Key scan operation

One key scan requires 15ms (if fosc = 38kHz, 582 / fosc (sec)). Key scans which are shorter than this time cannot be received. Also, in order to prevent chattering, the key scan waveform (KO output) reaches the HIGH level twice during one key scan. After scanning has been carried out twice, the data from the two scans is compared, and if the data for all of the keys does not match, an error occurs.

1) Key scans and key data communications

With the BU9768AK / BU9768AKV, if normal key input is received, DO changes from HIGH to LOW, so if DO is connected to the interrupt input pin of the controller, interrupt processing can be carried out based on the key input. Also, after DO changes to LOW following completion of a key scan, a new key scan cannot be carried out until all of the key data has been read.

If multiple keys are pressed at once, multiple key data is set for the various key inputs to be distinguished.

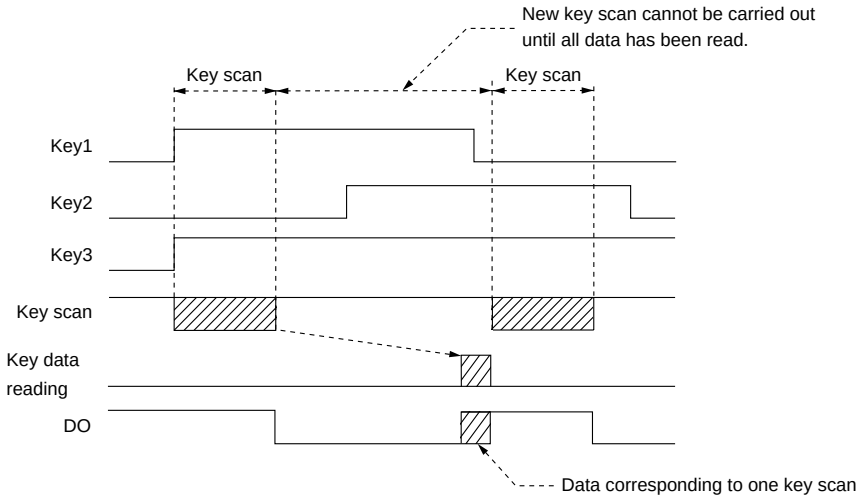

Fig. 10 Relationship between key scan and data communications

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2) Key scans in sleep modes

In sleep modes, depending on the mode, the key scan standby state of the KO pin is restricted.

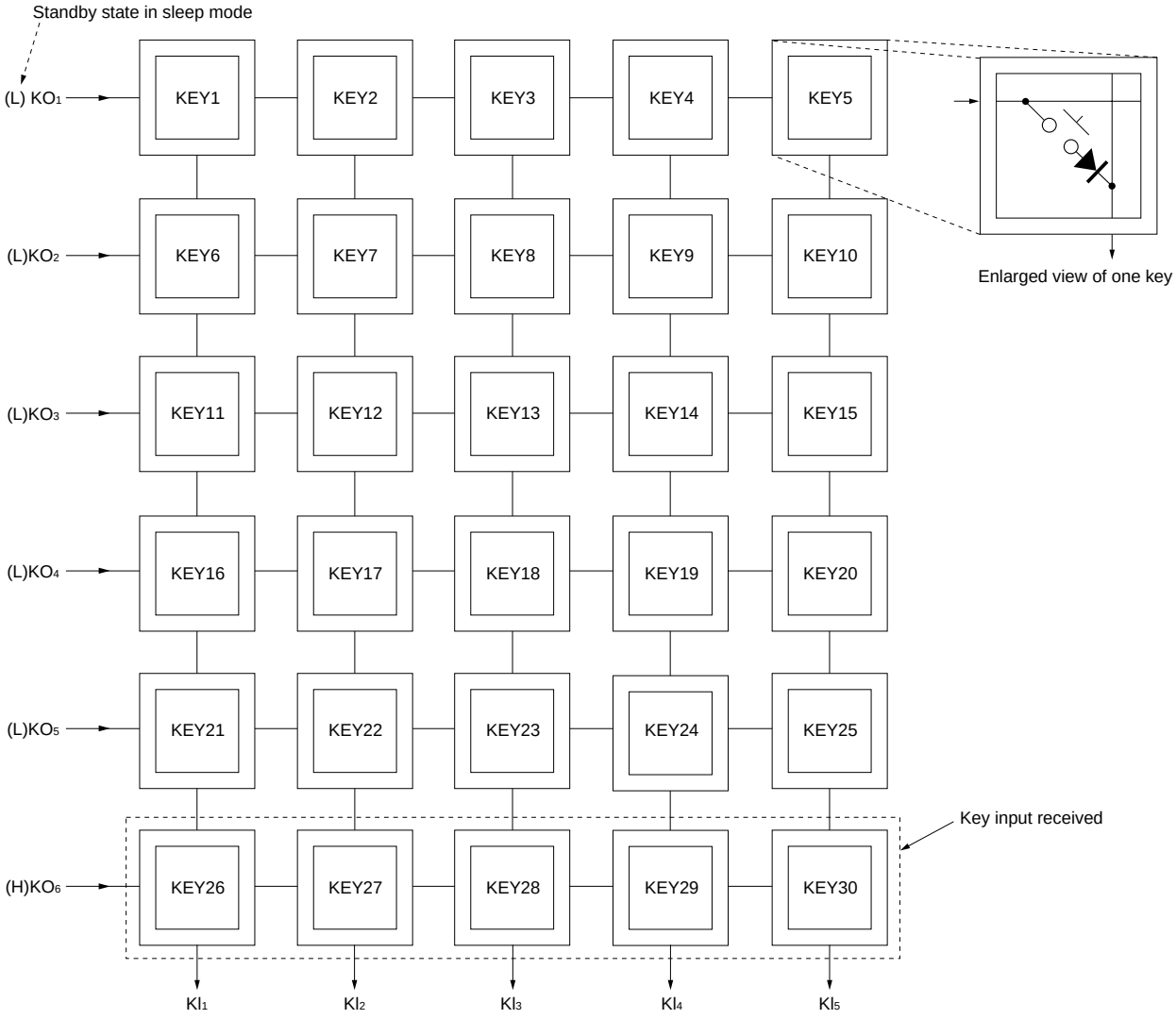

Fig. 11 Example of key matrix configuration

(The diodes installed on each key are to prevent erroneous recognition if multiple keys are pressed.)

The figure above assumes that the control codes S_0 and S_1 have been set to 0 and 1, respectively. In this case, if any key between key 26 and key 30 is pressed, an HIGH level is input on the KIn line, oscillation begins, and a key scan is carried out. If any key between key 1 and key 25 is pressed, all of the KIn lines remain at LOW level, and no key scan is carried out. Oscillation resumes when the key scan has been completed.

If key input in a sleep mode is to be used and interrupt processing carried out, a key on a KOn = HIGH line should be used.

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3) Operation flow in a key scan

The flow of operations taking place during a key scan is shown below.

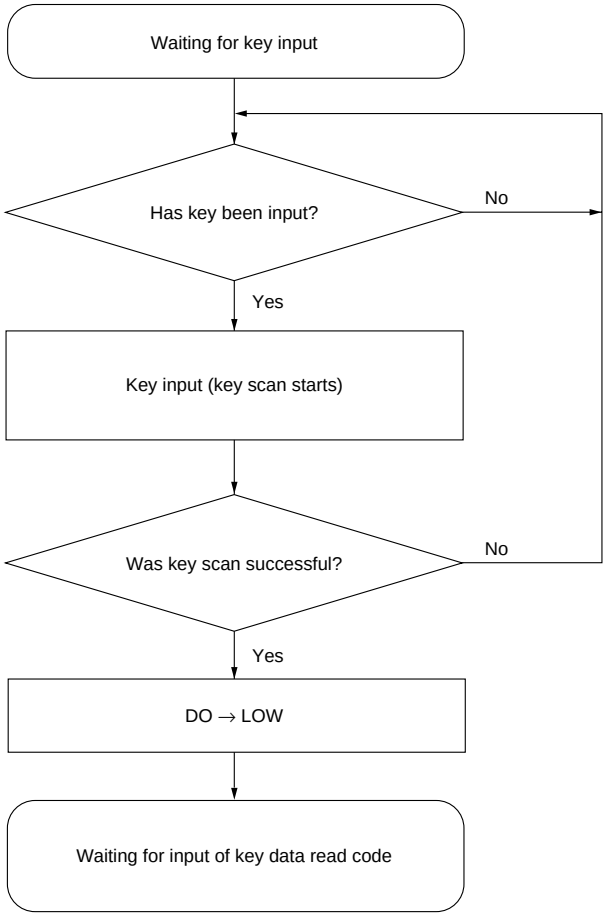

Fig. 12 Key scan flow

The “successful” judgment of the key scan shown in the illustration is based on the data from the two key scans matching for all of the keys, as described on page 13.

If an error occurs, the key scan is carried out once again after the first key scan has been completed if a key has remained pressed, and continues to be carried out as long as the key is pressed, until it is successfully completed.

After a key scan has been successfully completed, no new key scans can be carried out until reading of the key data has been completed.

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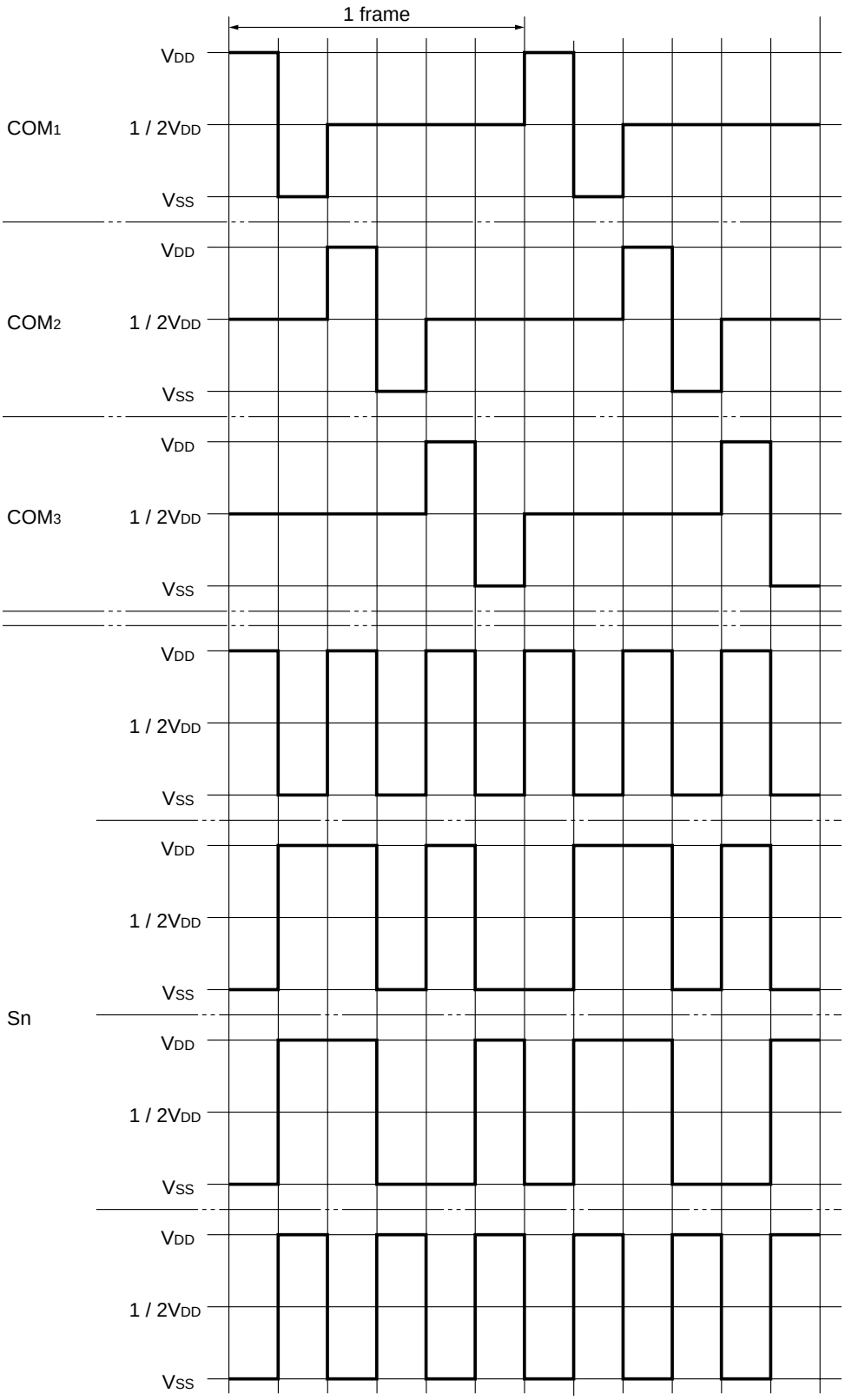
(3) Output waveforms

1) 1 / 2 bias mode (frame frequency = f_{OSC} / 384)



When Sn (D_{3n-2}, D_{3n-1}, D_{3n}) = (0, 0, 0):
Out for all COMs

When Sn (D_{3n-2}, D_{3n-1}, D_{3n}) = (0, 0, 1):
Lights between COM_1 and Sn only

When Sn (D_{3n-2}, D_{3n-1}, D_{3n}) = (1, 0, 1):
Out between COM_2 and Sn only

When Sn (D_{3n-2}, D_{3n-1}, D_{3n}) = (1, 1, 1):
Lights for all COMs

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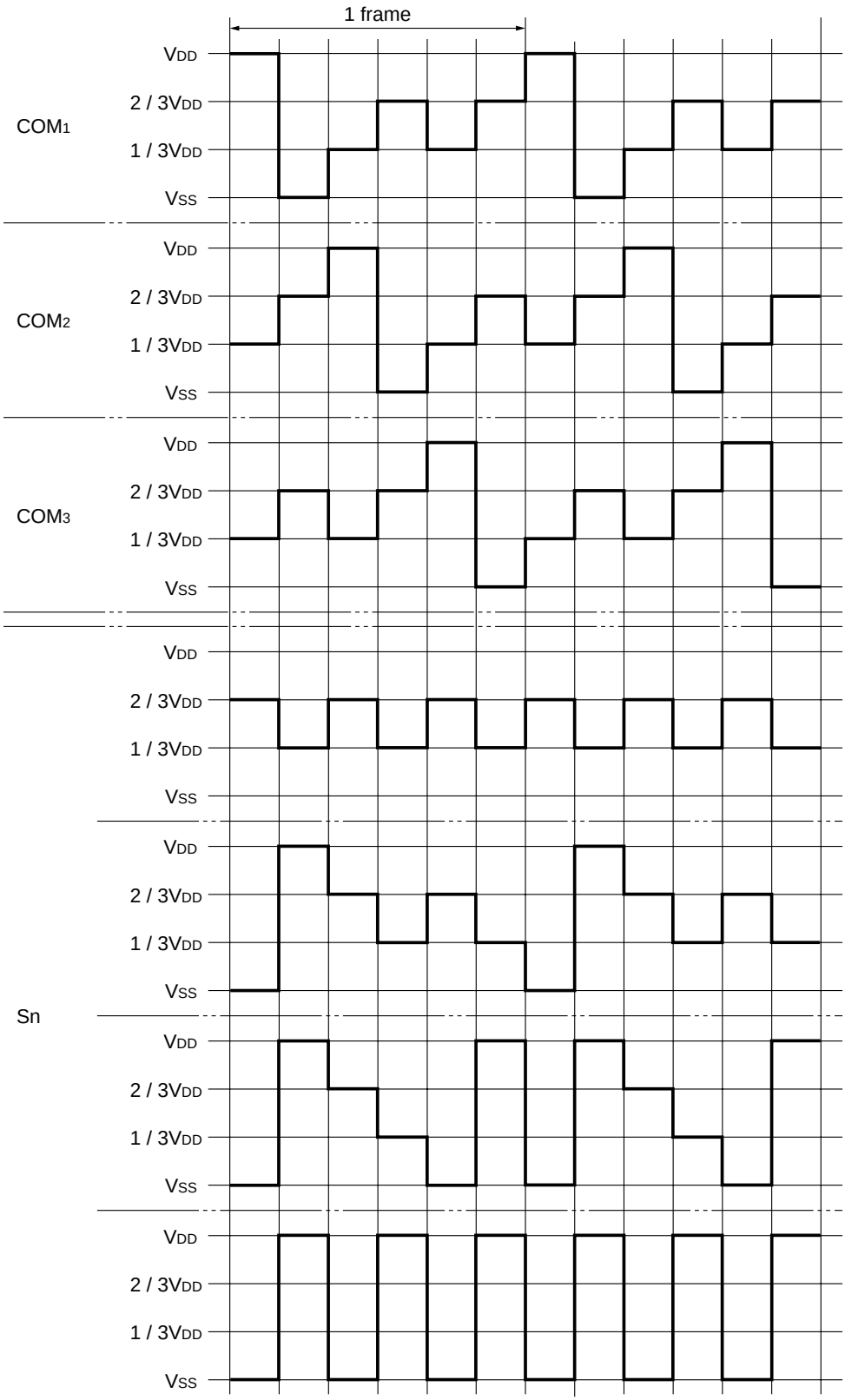
2) 1 / 3 bias mode (frame frequency = f_{OSC} / 384)



When Sn (D_{3n-2}, D_{3n-1}, D_{3n}) = (0, 0, 0):
Out for all COMs

When Sn (D_{3n-2}, D_{3n-1}, D_{3n}) = (0, 0, 1):
Lights between COM_1 and Sn only

When Sn (D_{3n-2}, D_{3n-1}, D_{3n}) = (1, 0, 1):
Out between COM_2 and Sn only

When Sn (D_{3n-2}, D_{3n-1}, D_{3n}) = (1, 1, 1):
Lights for all COMs

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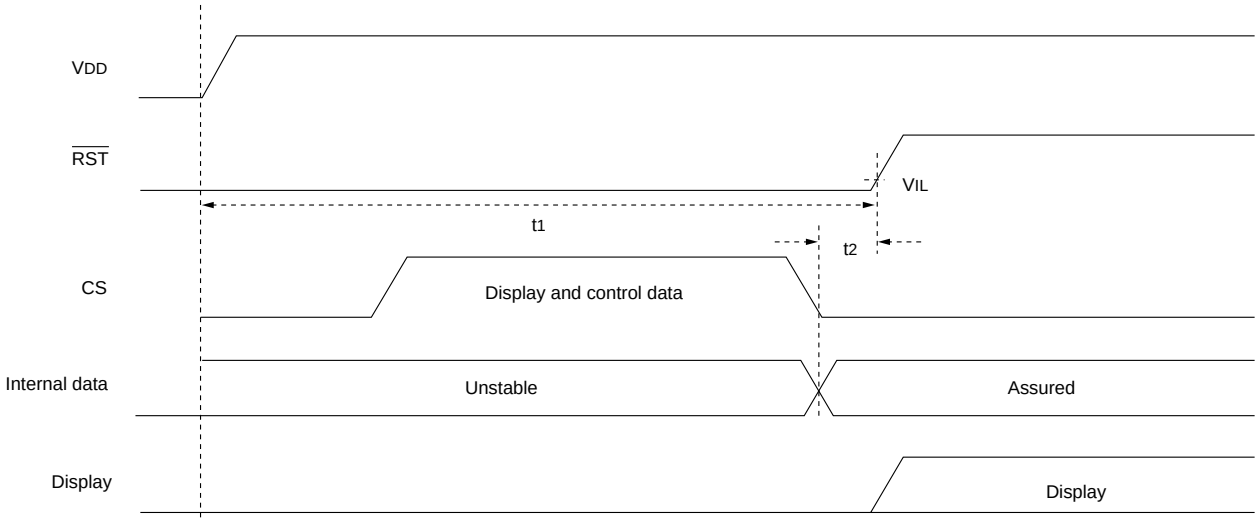
(4) $\overline{RST}$ and display control

After the power supply has been turned on, because the internal data of the BU9768AK / BU9768AKV (D_1 to D_{126}) is unstable, $\overline{RST}$ goes LOW at the same time that the power supply is turned on. While $\overline{RST}$ is LOW, data is transmitted using the microcomputer, and when data transmission has been completed, $\overline{RST}$ can be set to HIGH to prevent meaningless displays. (For the states of control codes when the power supply is turned on, see page 11.)



t1: Communication time
t2: 10µs min.

Fig. 13 Communication, display and $\overline{RST}$ timing

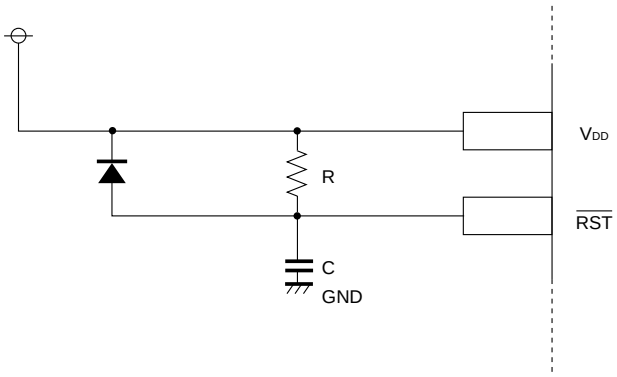


Fig. 14 Example of $\overline{RST}$ pin processing

In the circuit example shown above, the value of t1 is determined by the value of the capacitor and resistor. The value should be set in such a way that the constant determined by the capacitor and resistor is the initialized communication time + t2.

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●Operation notes

(1) Using the product with the synchronous clock stopped

If the synchronous clock is to be stopped during the period that data is not being transmitted, program the product so that the rise of CK is input at least twice after the fall of CS.

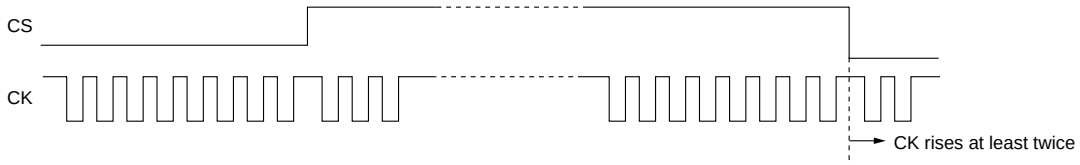

Fig. 15 When CK is stopped at HIGH

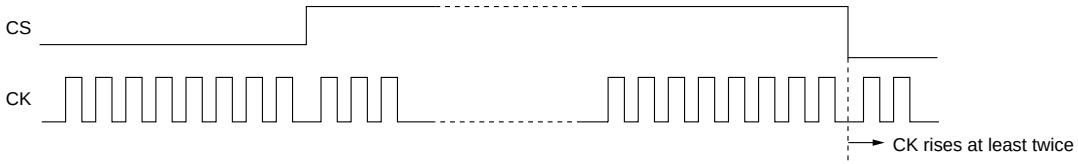

Fig. 16 When CK is stopped at LOW

(2) Precautions concerning key scans when the power supply is turned on

To carry out a key scan immediately after the power supply is turned on, without transmitting data, the parameters must be set so that the following conditions are met.

1) The rise of the synchronous clock pulse is input to the CK pin at least twice.
2) Since input can only be received from keys on the KO_3 to KO_6 line, other keys should not be used for functions such as interrupts. (For information on the status when the power supply is turned on, please see page 11.)

∗ If data is being transferred before a key scan is carried out, after the power supply is turned on, these precautions do not apply.

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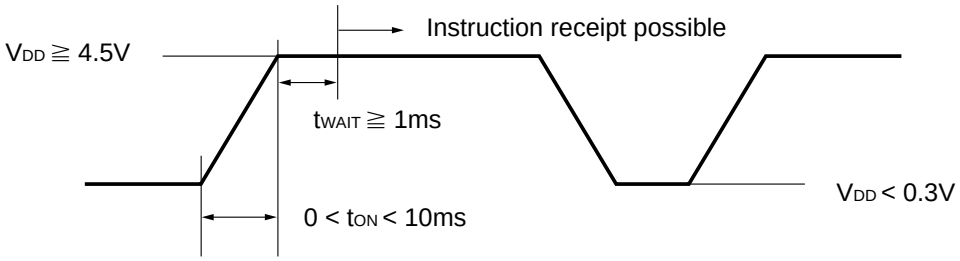
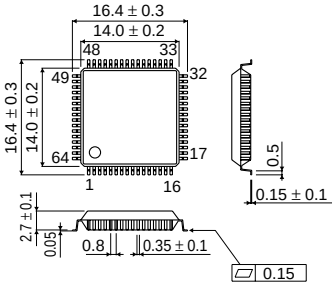
Make sure of the following when resetting when the power is on.

- When using the external reset terminal, make $\overline{RST}$ = “L” at 1ms or more with V_{DD} at 4.5V or more.
- When not using the external reset terminal, V_{DD} has to satisfy the following conditions.



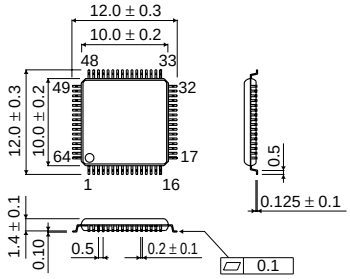
●External dimensions (Units: mm)

BU9768AK



QFP-A64

BU9768AKV



VQFP64

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