

- STRUCTURE** Silicon monolithic integrated circuit
- PRODUCTNAME** BU97931FV
- FUNCTION** LCD control driver for segment type LCD display
- FEATURE**
- LCD drive output : Common output : 4, Segment output : 28
 - Built-in Display data RAM (DDRAM) : RAM: 28*4 =112 bit
 - 3-wire Serial interface(SD, SCL, CSB)
 - Built-in Oscillator circuit
 - Built-in LCD Voltage Generator circuit: support 1/3 Bias, 1/3 or 1/4 Duty, 1/1 Bias, 1/1Duty (Static Driving)
 - Built-in Buffer AMP
 - Support Split Supply for Logic (VDD) and LCD (VLCD)
 - Support two output mode SEG/GPO (SEG23~27)
 - Built-in LED driver
 - Support PWM source select, external clock or internal clock (support 8bit mode)
 - Low power consumption
 - Support standby mode
 - Built-in Power-on Reset circuit
 - No external component
 - Support blink function (Blink frequency 1.6, 2.0, 2.6, 4.0Hz selectable)
 - Operating power supply: 1.8 ~ 3.6V
 - LCD drive power supply: 3.3 ~ 5.5V

○ **Absolute maximum ratings (VSS = 0V)**

Parameter	Symbol	Rated values	Unit	Remarks
Power supply voltage 1	VDD	-0.3 ~ +4.5	V	Power supply
Power supply voltage 2	VLCD	-0.5 ~ +7.0	V	Power supply for LCD
Allowable loss	Pd	0.8*1	W	
Input voltage range	VIN	-0.5 - VDD+0.5	V	
Operational temperature range	Topr	-30 ~ +75	°C	
Storage temperature range	Tstg	-55 ~ +125	°C	
Output current	Iout1	5	mA	SEG output
	Iout2	5	mA	COM output
	Iout3	10	mA	GPO output
	Iout4	50	mA	LED output

*1 When use more than Ta=25 degree, subtract 10.0mW per degree. (using ROHM standard board)
 (board size: 70mm×70mm×1.6mm material: FR4 board copper foil: land pattern only)

○ **Recommend operating conditions (Ta=-30 ~ +75degree, VSS = 0V)**

Parameter	Symbol	MIN	TYP	MAX	Unit	Remarks
Power supply voltage 1	VDD	1.8	-	3.6	V	Power supply
Power supply voltage 2	VLCD	2.7	-	5.5	V	Power supply for LCD

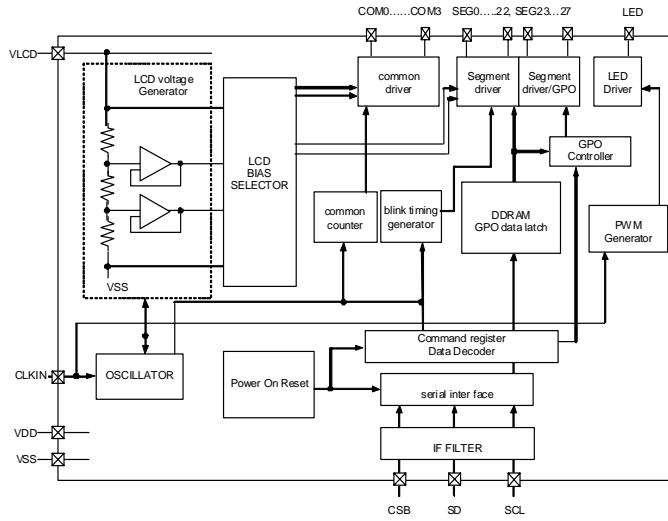
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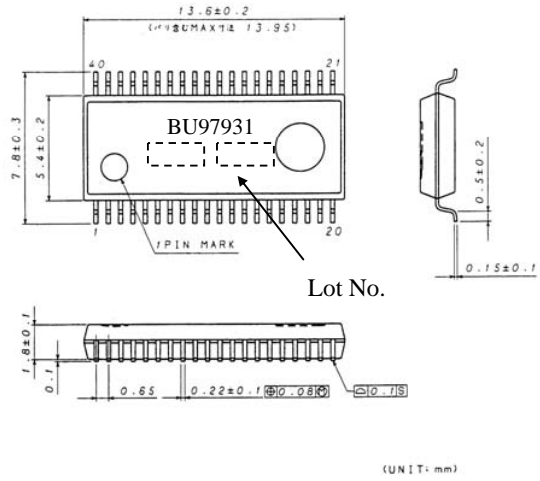
The Japanese version of this document is the formal specification. A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document, formal version takes priority.

○Block diagrams



○Outline drawing



Package :SSOP-B40

○ Electrical Characteristics (Ta=-30 ~ 75degree, VDD=1.8 ~ 3.6V, VLCD=2.7 ~ 5.5V, VSS=0 ; unless otherwise specified)

Parameter	Symbol	Limit			Unit	Condition
		MIN	TYP	MAX		
“H” level input voltage	VIH	0.8VDD	-	VDD	V	SD, SCL, CSB, CLKIN
“L” level input voltage	VIL	VSS	-	0.2VDD	V	SD, SCL, CSB, CLKIN
“H” level input current	I _{IH1}	-	-	5	uA	SD, SCL, CSB, CLKIN VI=3.6V
“L” level input current	I _{IL1}	-5	-	-	uA	SD, SCL, CSB, CLKIN VI=0V
“H” level output voltage (*2)	VOH1	VLCD -0.4	-	-	V	Iload=-50uA, VLCD=5.0V, SEG0~27
	VOH2	VLCD -0.4	-	-	V	Iload=-50uA, VLCD=5.0V, COM0~3
	VOH3	VLCD -0.6	-	-	V	Iload=-1mA, VLCD=5.0V, SEG23~27(GPO mode)
“L” level output voltage (*2)	VOL1	-	-	0.4	V	Iload= 50uA, VLCD=5.0V, SEG0~27
	VOL2	-	-	0.4	V	Iload= 50uA, VLCD=5.0V, COM0~3
	VOL3	-	-	0.5	V	Iload=1mA, VLCD=5.0V, VDD=3.3V SEG23~27(GPO mode), PWMOUT
	VOL4	-	0.34	0.5	V	Iload=20mA, VLCD=5.0V, LED
Supply current (*1)	IstVDD	-	3	10	uA	Input terminal ALL'L, Display off, Oscillation off
	IstVLCD	-	0.5	5	uA	Input terminal ALL'L, Display off, Oscillation off
	IVDD1	-	8	15	uA	VDD=3.3V, Ta=25degree, 1/3bias, fFR=64Hz, PWM generate off, All output pin open
	IVDD2	-	30	45	uA	VDD=3.3V, Ta=25degree, 1/3bias, fFR=64Hz, PWM Frequency=500Hz setting, output pin open
	IVLCD1	-	10	15	uA	VLCD=5.0V, Ta=25degree, 1/3bias, fFR=64Hz, PWM generate off, All output pin open
IVLCD2	-	30	48	uA	VLCD=5.0V, Ta=25degree, 1/3bias, fFR=64Hz, PWM Frequency=500Hz setting, All output pin open	

*1: In case, power save mode 1 and frame inversion setting

*2: Iload : In case, load current from only one port

○ Oscillation Frequency Characteristics (Ta=-30 ~ 75degree, VDD=1.8 ~ 3.6V, VLCD=2.7 ~ 5.5V, VSS=0 ; unless otherwise specified)

Parameter	Symbol	Limit			Unit	Condition
		MIN	TYP	MAX		
Frame frequency 1	fFR1	57.6	64	70.4	Hz	VDD=3.3V, Ta=25degree, fFR=64Hz setting
Frame frequency 2	fFR2	51.2	64	73.0	Hz	VDD=2.5~3.6V fFR=64Hz setting
Frame frequency 3	fFR3	45.0	-	64	Hz	VDD=1.8~2.5V fFR=64Hz setting

○ Load regulation (Ta=-30 ~ 75degree, VDD=1.8 ~ 3.6V, VLCD=2.7 ~ 5.5V, VSS=0 ; unless otherwise specified)

Parameter	Symbol	Limit			Unit	Condition
		MIN	TYP	MAX		
Input rise time	tr	-	-	50	ns	
Input fall time	tf	-	-	50	ns	
SCL cycle time	tSCYC	250	-	-	ns	
"H" SCL pulse width	tSHW	50	-	-	ns	
"L" SCL pulse width	tSLW	50	-	-	ns	
SD setup time	tSDS	50	-	-	ns	
SD hold time	tSDH	50	-	-	ns	
CSB setup time	tCSS	50	-	-	ns	
CSB hold time	tCSH	50	-	-	ns	
"H" CSB pulse width	tCHW	50	-	-	ns	

○ Terminal number/name

1	SEG5	9	SEG13	17	SEG21	25	VSS	33	COM1
2	SEG6	10	SEG14	18	SEG22	26	CSB	34	COM2
3	SEG7	11	SEG15	19	SEG23	27	SCL	35	COM3
4	SEG8	12	SEG16	20	SEG24	28	SD	36	SEG0
5	SEG9	13	SEG17	21	SEG25	29	VDD	37	SEG1
6	SEG10	14	SEG18	22	SEG26	30	CLKIN	38	SEG2
7	SEG11	15	SEG19	23	SEG27	31	VLCD	39	SEG3
8	SEG12	16	SEG20	24	LED	32	COM0	40	SEG4

Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, or the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.

Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) No Connecting input terminals

In terms of extremely high impedance of CMOS gate, to open the input terminals causes unstable state. And unstable state brings the inside gate voltage of p-channel or n-channel transistor into active. As a result, battery current may increase. And unstable state can also causes unexpected operation of IC. So unless otherwise specified, input terminals not being used should be connected to the power supply or GND line.

(13) Rush current

When power is first supplied to the CMOS IC, it is possible that the internal logic may be unstable and rush current may flow instantaneously. Therefore, give special condition to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

Notes

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