

## FEATURES

- Complete Solution Under 1.2mm
- Develops Three Outputs from a 3.3V or 5V Supply
- Externally Programmable  $V_{ON}$  Delay
- Fixed Frequency Low Noise Outputs
- All Ceramic Capacitors
- 3MHz Switching Frequency
- Fast Transient Response
- Few External Components Required
- 2.7V to 8V Input Range
- Adjustable  $AV_{DD}$  and  $V_{ON}$  Voltages
- Tiny 10-Lead MSOP and Thermally Enhanced 10-Lead MSOP Packages

## APPLICATIONS

- TFT-LCD Notebook Display Panels
- TFT-LCD Desktop Monitor Display Panels
- Digital Cameras
- Handheld Computers

## DESCRIPTION

The LT<sup>®</sup>1947 is a highly integrated multiple output DC/DC converter designed for use in TFT-LCD panels. The device contains two independent switching regulators. The main regulator has an adjustable output voltage with an internal 1.1A switch that can generate a boosted voltage as high as 30V. The second regulator's output is also adjustable up to 30V and can deliver 10mA for positive bias. A simple level-shift charge pump off the main switch node generates the negative bias voltage. An external capacitor sets the delay time from  $AV_{DD}$ 's final value to the rising edge at the  $V_{ON}$  pin. The 3MHz switching frequency allows the use of tiny low profile chip inductors and capacitors throughout, providing a low noise, low cost total solution with all components under 1.2mm in height. The device operates from an input range of 2.7V to 8V and is available in 10-lead MSOP and thermally enhanced 10-lead MSOP packages.

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## TYPICAL APPLICATION

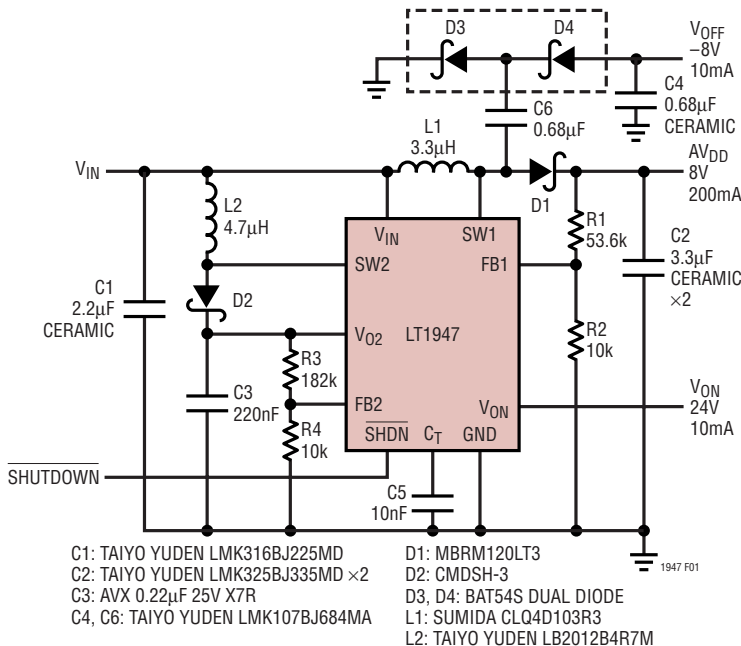
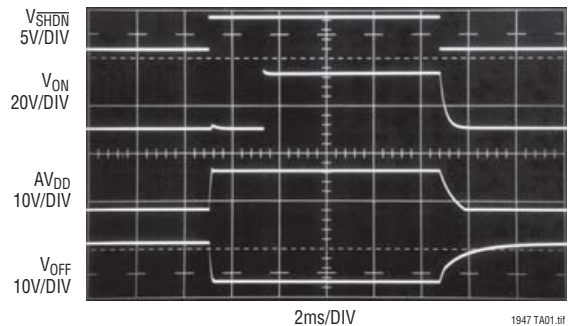


Figure 1. 3.3V Powered TFT-LCD Bias Generator

### Start-Up Waveforms



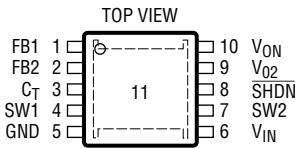
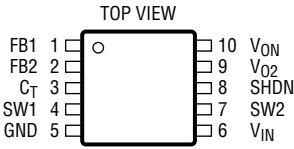
## ABSOLUTE MAXIMUM RATINGS

(Note 1)

$V_{IN}$ Voltage .....	8V
$C_T$ Voltage .....	6V
SW1, SW2 Voltage .....	36V
$V_{ON}$ , $V_{O2}$ Voltage .....	30V

FB1, FB2 .....	3V
SHDN .....	8V
Operating Temperature Range (Note 2) ..	-40°C to 85°C
Lead Temperature (Soldering, 10 sec) .....	300°C

## PACKAGE/ORDER INFORMATION

 <p>MSE PACKAGE 10-LEAD PLASTIC MSOP EXPOSED PAD (PIN 11) IS GND MUST BE SOLDERED TO PCB <math>T_{JMAX} = 125^{\circ}C</math>, <math>\theta_{JA} = 40^{\circ}C/W</math></p>	ORDER PART NUMBER	 <p>MS PACKAGE 10-LEAD PLASTIC MSOP <math>T_{JMAX} = 125^{\circ}C</math>, <math>\theta_{JA} = 120^{\circ}C/W</math></p>	ORDER PART NUMBER
	LT1947EMSE		LT1947EMS
	MSE PART MARKING		MS PART MARKING
	LTBQW		LTUE

**Order Options** Tape and Reel: Add #TR, Lead Free: Add #PBF, Lead Free Tape and Reel: Add #TRPBF

Lead Free Part Marking: <http://www.linear.com/leadfree/>

Consult LTC Marketing for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^{\circ}C$ .  $V_{IN} = 3.3V$ ,  $V_{SHDN} = 3.3V$  unless otherwise specified.

SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range		2.7		8	V
Supply Current	SHDN = 2.4V SHDN = 0V		9.5	12.5 1	mA $\mu A$
FB1 Voltage		● 1.240 1.225	1.26	1.280 1.295	V V
FB2 Voltage		● 1.225 1.210	1.26	1.295 1.310	V V
Reference Line Regulation	$V_{IN} = 2.7V$ to 8V		0.01	0.05	%/V

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{IN} = 3.3\text{V}$ ,  $V_{\overline{\text{SHDN}}} = 3.3\text{V}$  unless otherwise specified.

SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Error Amplifier Voltage Gain	EA1 and EA2		100		V/V
$C_T$ Current Source	$V_{\overline{\text{FB1}}} = 1.3\text{V}$	4	5.5	6.5	$\mu\text{A}$
$C_T$ Threshold to Turn On Q3		1.25	1.28	1.30	V
FB1 Voltage to Begin $C_T$ Charge		1.17	1.2	1.23	V
SW1 Current Limit	(Note 3)	1.1	1.4	2	A
SW2 Current Limit	(Note 3)	0.35	0.6	1	A
SW1 Saturation Voltage	$I_{\text{SW1}} = 800\text{mA}$		0.230	0.280	V
SW2 Saturation Voltage	$I_{\text{SW2}} = 300\text{mA}$		0.3	0.36	V
SW1 Maximum Duty Cycle		82			%
SW2 Maximum Duty Cycle			85		%
Oscillator Frequency		● 2.3	3	3.5	MHz
$V_{\text{ON}}$ Switch Drop	$I_{\text{Q3}} = 7\text{mA}$		160	200	mV
SW1 Leakage Current	Switch Off, $\text{SW1} = 3.3\text{V}$		0.01	5	$\mu\text{A}$
SW2 Leakage Current	Switch Off, $\text{SW2} = 3.3\text{V}$		0.01	5	$\mu\text{A}$
$\overline{\text{SHDN}}$ Pin Bias Current	$V_{\overline{\text{SHDN}}} = 2.4\text{V}$		10	25	$\mu\text{A}$
$\overline{\text{SHDN}}$ Pin High	Active Mode	2.4			V
$\overline{\text{SHDN}}$ Pin Low	Shutdown Mode			0.4	V

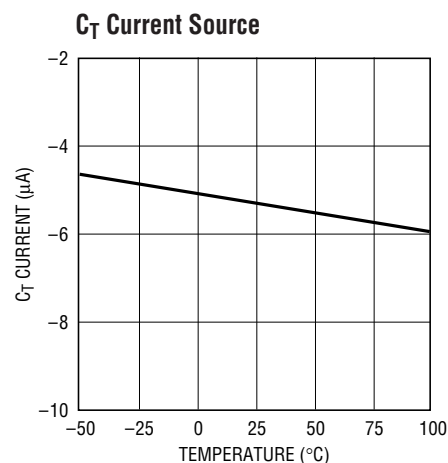
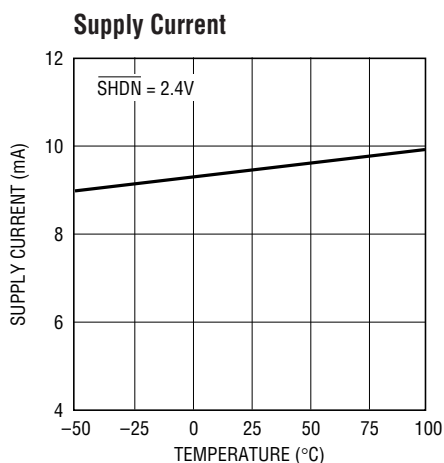
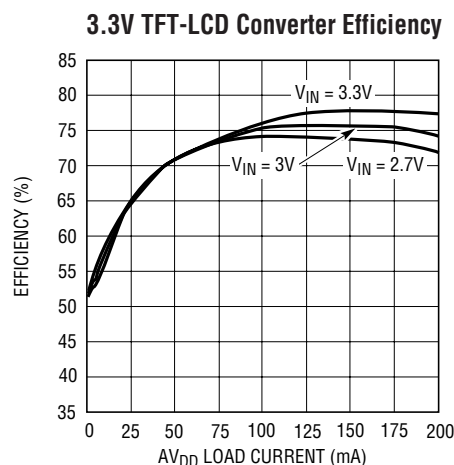
**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** The LT1947 is guaranteed to meet performance specifications from  $0^\circ\text{C}$  to  $70^\circ\text{C}$ . Specifications over the  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  operating

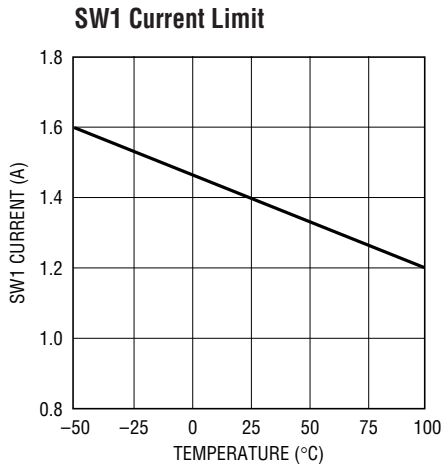
temperature range are assured by design, characterization and correlation with statistical process controls.

**Note 3:** Switch current limit guaranteed by design and/or correlation to static tests.

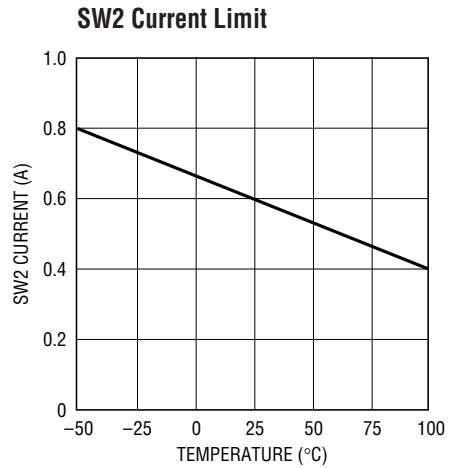
## TYPICAL PERFORMANCE CHARACTERISTICS



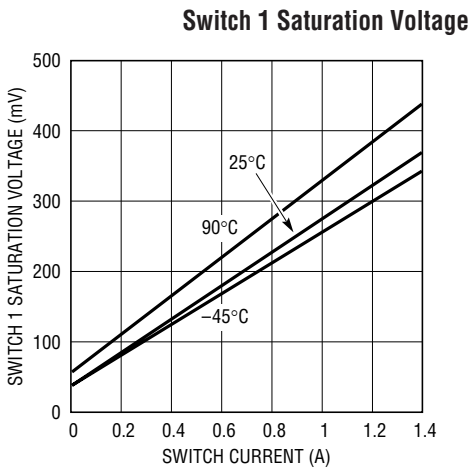
# TYPICAL PERFORMANCE CHARACTERISTICS



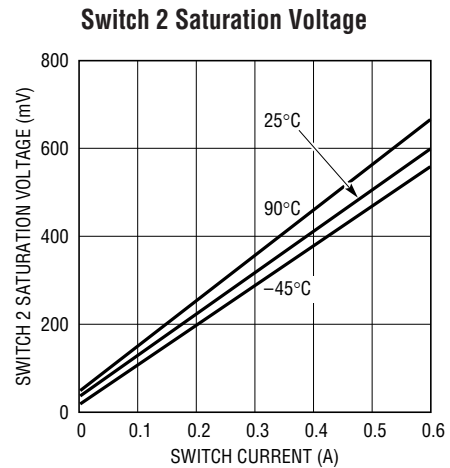
1947 G04



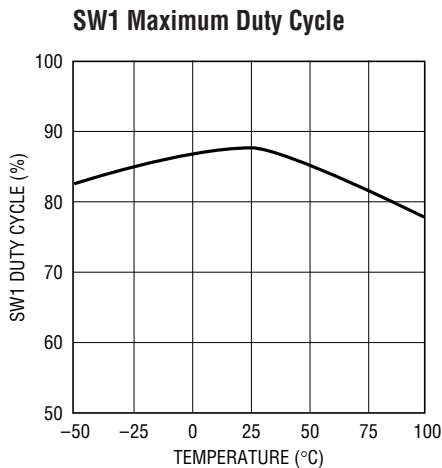
1947 G05



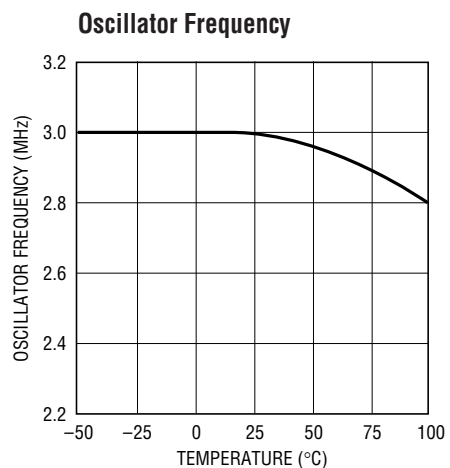
1947 G06



1947 G07



1947 G08



1947 G09

## PIN FUNCTIONS

**FB1 (Pin 1):** Feedback Pin for First Switcher. Connect resistor divider tap here. Set  $AV_{DD}$  according to:  $AV_{DD} = 1.26V(1 + R1/R2)$ .

**FB2 (Pin 2):** Feedback Pin for Second Switcher. Connect resistor divider 2 here and set  $V_{ON}$  using:  $V_{ON} = 1.26V(1 + R3/R4) - 160mV$ .

**$C_T$  (Pin 3):** Timing Capacitor Pin. Connect a 10nF capacitor from  $C_T$  to ground to program a 2.3ms delay from FB1 reaching 1.26V to  $V_{ON}$  turning on.

**SW1 (Pin 4):**  $AV_{DD}$  Switch Node. Connect L1 and D1 here (see Figure 1). Minimize trace area at this pin to keep EMI down.

**GND (Pin 5):** Ground. Connect directly to local ground plane.

**$V_{IN}$  (Pin 6):** Input Supply Pin. Must be bypassed with a ceramic capacitor close to the pin.

**SW2 (Pin 7):**  $V_{O2}$  Switch Node. Connect L2 and D2 here. Minimize trace area at this pin to keep EMI down.

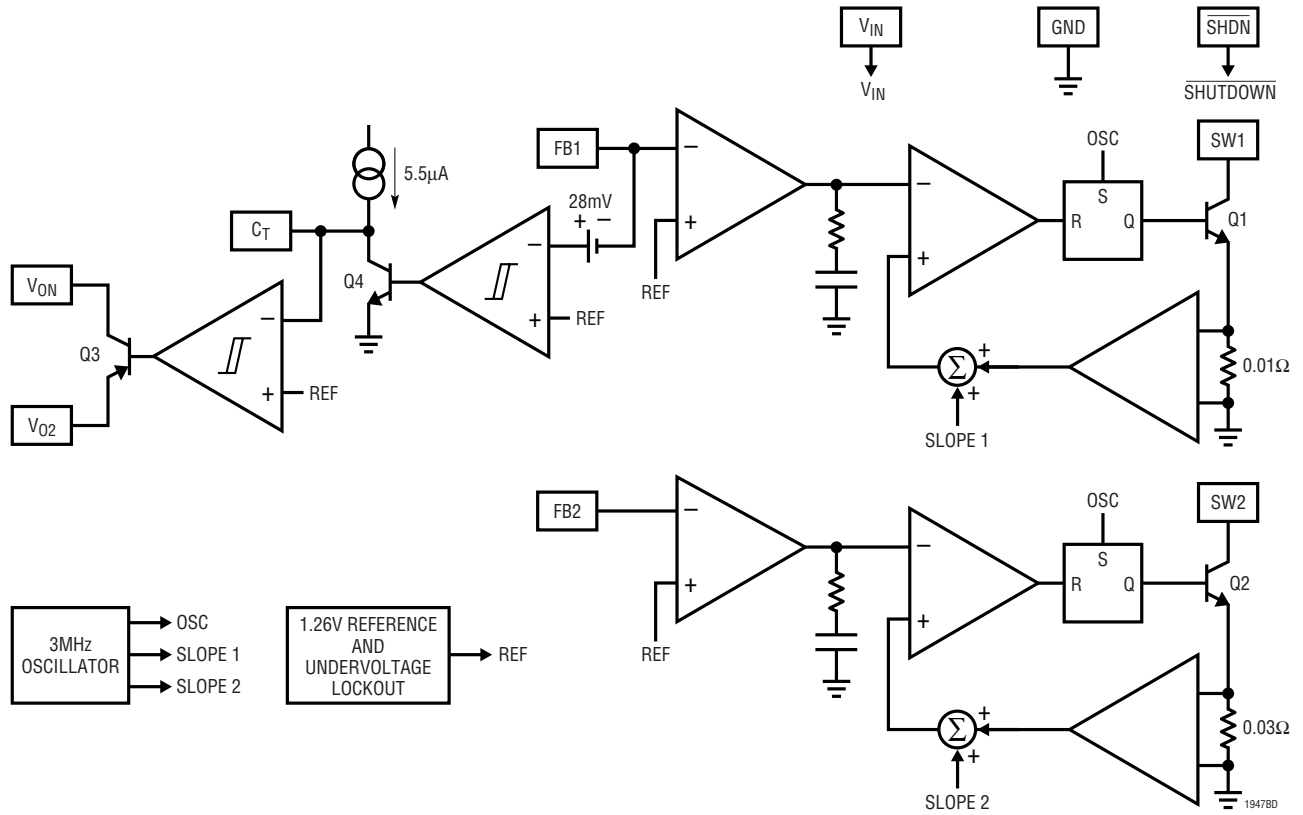
**$\overline{SHDN}$  (Pin 8):** Pull this pin low for shutdown mode. For normal operation, tie to a voltage between 2.4V and 8V.

**$V_{O2}$  (Pin 9):** SW2 Output. This node is also internally connected to the emitter of Q3 (see Block Diagram), the high side switch between  $V_{O2}$  and  $V_{ON}$ .

**$V_{ON}$  (Pin 10):** This is the delayed output for second Switcher.  $V_{ON}$  reaches its programmed voltage after the internal timer times out.

**Exposed Pad (Pin 11):** Ground (MSE package only). The exposed pad must be soldered to the PCB and electrically connected to ground.

**BLOCK DIAGRAM**



## OPERATION

To best understand operation of the LT1947, please refer to the LT1947 Block Diagram. The device contains two switching regulators, a timer and a high side switch. Three outputs can be generated: an adjustable  $AV_{DD}$  output, a charge-pumped inversion of the  $AV_{DD}$  output called  $V_{OFF}$ , and a time delayed adjustable output called  $V_{ON}$ . Q3 keeps  $V_{ON}$  off for an externally set time interval, set by a capacitor connected to the  $C_T$  pin.

The switching frequency of both switchers is 3MHz, set internally. The switchers are current mode and are internally compensated. The main  $AV_{DD}$  switcher is current limited at 1.1A, while the second  $V_{ON}$  switcher is limited to 350mA. They share the same 1.26V reference voltage. When the input voltage is below approximately 2.7V, an undervoltage lockout circuit disables switching.

When  $AV_{DD}$  is less than its final voltage, Q4 is turned on, holding the  $C_T$  pin at ground. When  $AV_{DD}$  reaches final value, Q4 lets go of the  $C_T$  pin, allowing the 5.5 $\mu$ A current source to charge the external capacitor,  $C_T$ . When the voltage on the  $C_T$  pin reaches 1.28V, Q3 turns on, connecting  $V_{O2}$  to  $V_{ON}$ . Capacitor value can be calculated using the following formula:

$$C = (5.5\mu A \cdot t_{DELAY})/1.28V$$

A 10nF capacitor results in approximately 2.3ms of delay.

### Layout Hints

The high speed operation of the LT1947 mandates careful attention to layout for proper performance. Be sure to keep input capacitor C1 as close as possible to the IC and minimize trace area and length at the SW and FB pins. Always use a ground plane under the switching regulator to minimize interplane coupling. Figure 2 shows the recommended component placement.

The exposed pad of the MSE package must be soldered to the PCB and electrically connected to ground. Thermal vias to a large ground plane will lower the thermal resistance.

### Soft-Start

For applications requiring soft-start, a circuit consisting of  $R_{SS}$  and  $C_{SS}$  tied to the SHDN pin can be used, as shown in Figure 3. For a combination of 33.2k/33nF,  $AV_{DD}$  rises to its final value in approximately 3ms.

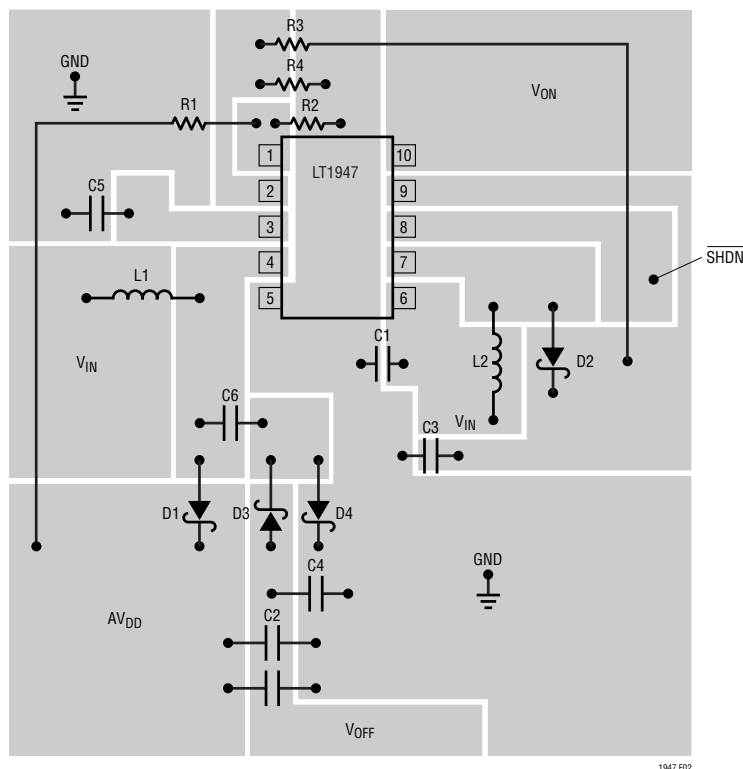


Figure 2. Recommended Component Placement

1947 F02

OPERATION

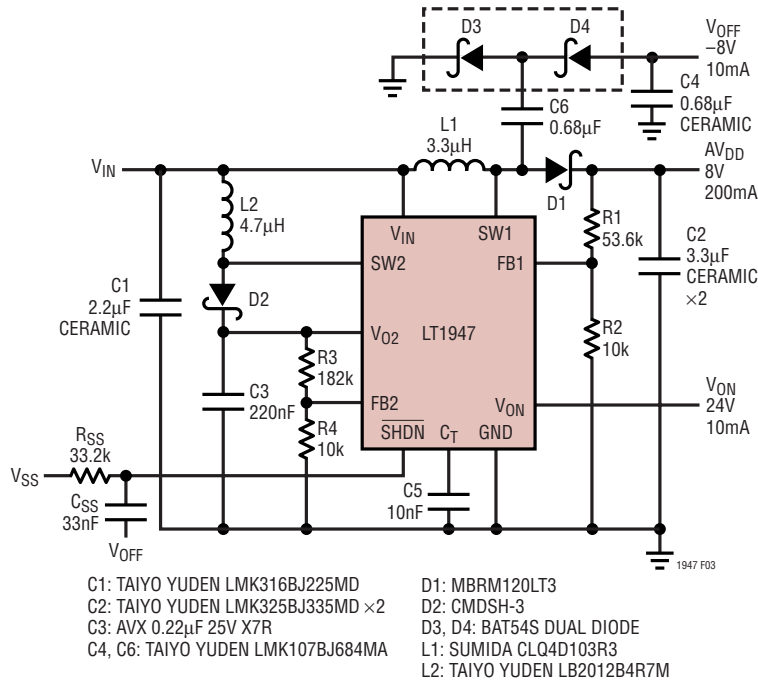


Figure 3. R<sub>SS</sub> and C<sub>SS</sub> at SHDN Pin Provide Soft-Start

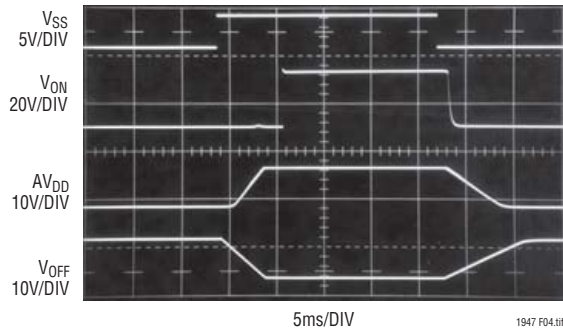
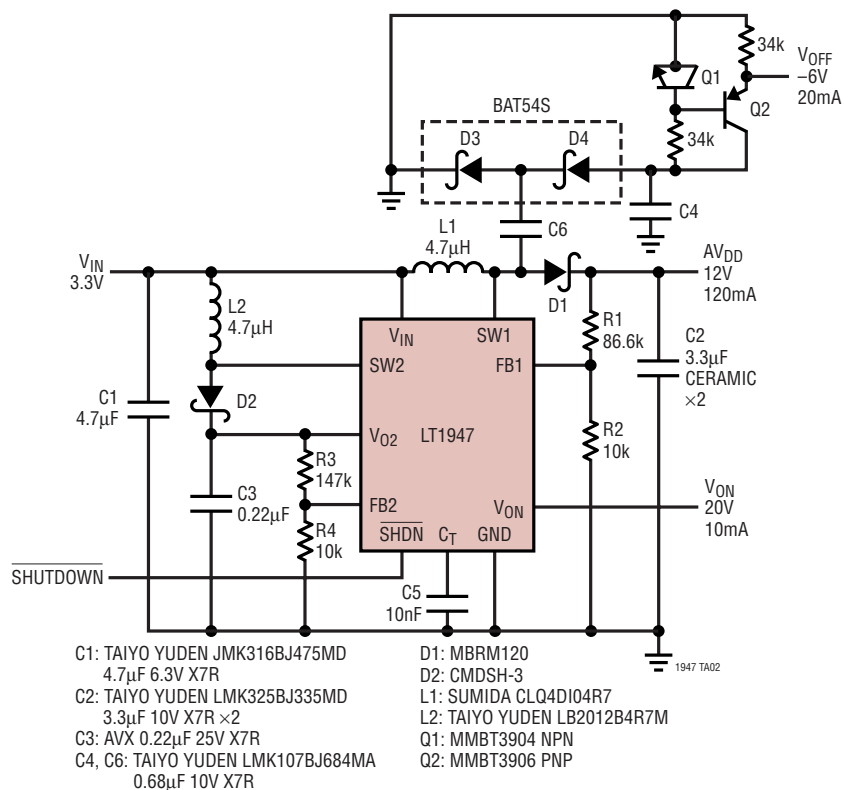


Figure 4. Start-Up Waveforms with Soft-Start Circuit Added

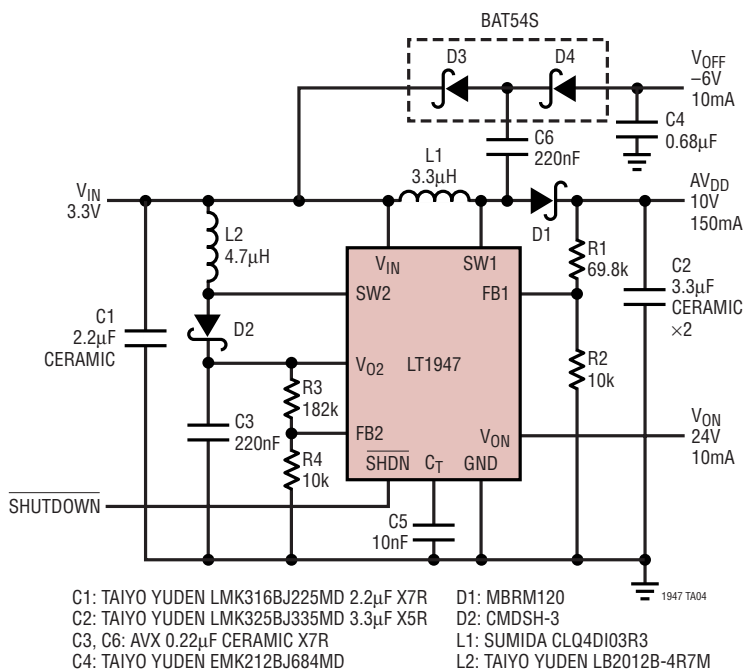


# TYPICAL APPLICATIONS

TFT-LCD Bias Generator: 12V, 20V, -6V Output

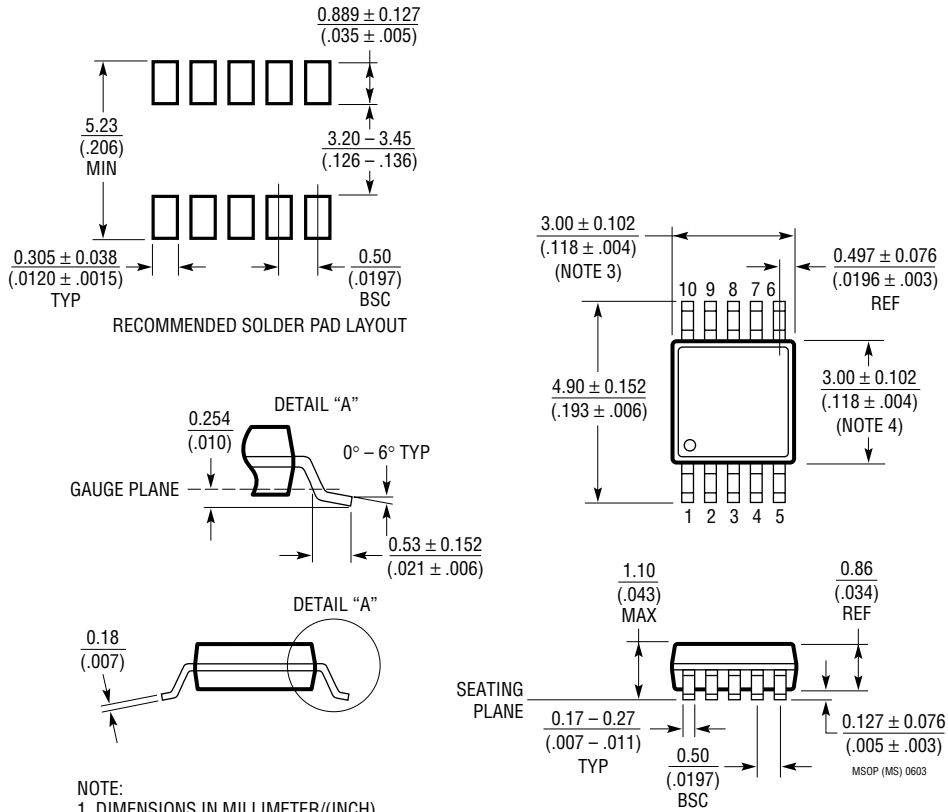


TFT-LCD Bias Generator: 10V, 24V, -6V Output



# PACKAGE DESCRIPTION

**MS Package**  
**10-Lead Plastic MSOP**  
 (Reference LTC DWG # 05-08-1661)



- NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
  2. DRAWING NOT TO SCALE
  3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.  
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
  4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.  
INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
  5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX



