32MHz, 1000V/µs Gain Selectable Amplifier

FEATURES

- **Internal Gain Setting Resistors**
- **Pin Configurable as a Difference Amplifier, Inverting and Noninverting Amplifier**
- **Difference Amplifier:**
  Gain Range 1 to 7
  CMRR > 65dB
- **Noninverting Amplifier:**
  Gain Range 1 to 8
- **Inverting Amplifier:**
  Gain Range –1 to –7
- **Gain Error: <0.2%**
- Slew Rate: 1000V/µs
- Bandwidth: 32MHz (Gain = 1)
- Op Amp Input Offset Voltage: 2.5mV Max
- Quiescent Current: 9mA Max
- Wide Supply Range: ±2.5V to ±15V
- Available in 10-Lead MSOP and 10-Lead (3mm × 3mm) DFN Packages

APPLICATIONS

- Instrumentation Amplifier
- Current Sense Amplifier
- Video Difference Amplifier
- Automatic Test Equipment

DESCRIPTION

The LT®1995 is a high speed, high slew rate, gain selectable amplifier with excellent DC performance. Gains from –7 to 8 with a gain accuracy of 0.2% can be achieved using no external components. The device is particularly well suited for use as a difference amplifier, where the excellent resistor matching results in a typical common mode rejection ratio of 79dB.

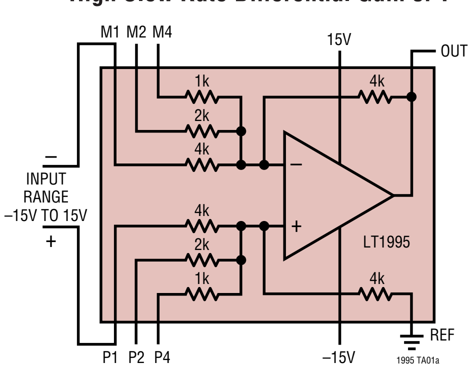
The amplifier is a single gain stage design similar to the LT1363 and features superb slewing and settling characteristics. Input offset of the internal operational amplifier is less than 2.5mV and the slew rate is 1000V/µs. The output can drive a 150Ω load to ±2.5V on ±5V supplies, making it useful in cable driver applications.

The resistors have excellent matching, 0.2% maximum at room temperature and 0.3% from –40°C to 85°C. The temperature coefficient of the resistors is typically –30ppm/°C. The resistors are extremely linear with voltage, resulting in a gain nonlinearity of 10ppm.

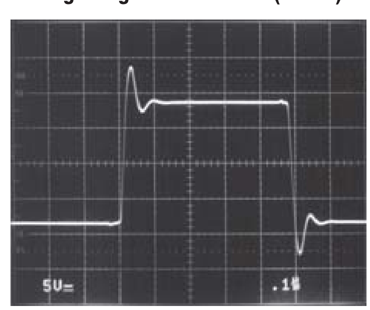
The LT1995 is fully specified at ±2.5V, ±5V and ±15V supplies and from –40°C to 85°C. The device is available in space saving 10-lead MSOP and 10-Lead (3mm × 3mm) DFN packages. For a micropower precision amplifier with precision resistors, see the LT1991 and LT1996.

TYPICAL APPLICATION

High Slew Rate Differential Gain of 1



Large-Signal Transient (G = 1)



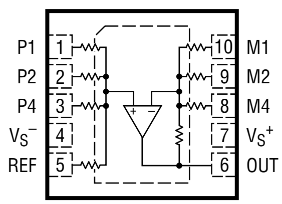
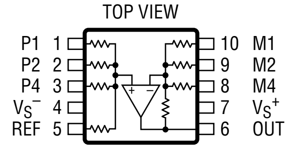
1995 TA01b

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 36V
Input Current (Note 2) .... ±10mA
Output Short-Circuit Duration (Note 3) .... Indefinite
Operating Temperature Range (Note 4) .. –40°C to 85°C
Specified Temperature Range (Note 5) ... –40°C to 85°C

Storage Temperature Range
MS Package .... –65°C to 150°C
DD Package .... –65°C to 125°C
Maximum Junction Temperature
MS Package .... 150°C
DD Package .... 125°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION

DD Package	ORDER PART NUMBER	MS Package	ORDER PART NUMBER
TOP VIEW  DD PACKAGE 10-LEAD (3mm × 3mm) PLASTIC DFN T_{JMAX} = 125°C, θ_{JA} = 160°C/W (NOTE 6) EXPOSED PAD INTERNALLY CONNECTED TO V_S^- PCB CONNECTION OPTIONAL	LT1995CDD LT1995IDD	TOP VIEW  MS PACKAGE 10-LEAD PLASTIC MSOP T_{JMAX} = 150°C, θ_{JA} = 160°C/W (NOTE 6)	LT1995CMS LT1995IMS
	DD PART MARKING*		MS PART MARKING*
	LBJF LBJF		LTBJD LTBJD

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grades are identified by a label on the shipping container.

ELECTRICAL CHARACTERISTICS

Difference Amplifier Configuration. T_A = 25°C, V_{REF} = V_{CM} = 0V and unused gain pins are unconnected, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
GE	Gain Error	V_{OUT} = ±12V, R_L = 1k, G = 1	±15V		0.05	0.2	%
		V_{OUT} = ±12V, R_L = 1k, G = 2	±15V		0.05	0.2	%
		V_{OUT} = ±12V, R_L = 1k, G = 4	±15V		0.05	0.2	%
		V_{OUT} = ±5V, R_L = 150Ω, G = 1	±15V		0.05	0.25	%
		V_{OUT} = ±2.5V, R_L = 500Ω, G = 1	±5V		0.05	0.2	%
		V_{OUT} = ±2.5V, R_L = 150Ω, G = 1	±5V		0.05	0.25	%
GNL	Gain Nonlinearity	V_{OUT} = ±12V, R_L = 1k, G = 1	±15V		10		ppm
V_{OS}	Input Offset Voltage Referred to Input (Note 7)	G = 1 (MS10)	±15V		1	5	mV
		G = 1 (DD10)	±15V		1.5	9	mV
		G = 2 (MS10)	±15V		0.7	4	mV
		G = 2 (DD10)	±15V		1.2	6.8	mV
		G = 4 (MS10)	±15V		0.6	3.75	mV
		G = 4 (DD10)	±15V		0.9	5.6	mV
		G = 1 (MS10)	±5V		1	5	mV
		G = 1 (DD10)	±5V		1.4	9	mV
		G = 1 (MS10)	±2.5V		1	5	mV
		G = 1 (DD10)	±2.5V		1.3	9	mV

ELECTRICAL CHARACTERISTICS

Difference Amplifier Configuration. T_A = 25°C, V_{REF} = V_{CM} = 0V and unused gain pins are unconnected, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS_OA}	Op Amp Input Offset Voltage (Note 10)	G = 1 (MS10) G = 1 (DD10)	±2.5V, ±5V, ±15V ±2.5V, ±5V, ±15V		0.5 0.75	2.5 4.5	mV mV
e_n	Input Noise Voltage	G = 1, f = 10kHz G = 2, f = 10kHz G = 4, f = 10kHz	±2.5V to ±15V ±2.5V to ±15V ±2.5V to ±15V		27 18 14		nV/√Hz nV/√Hz nV/√Hz
R_{IN}	Common Mode Input Resistance	V_{CM} = ±15V, G = 1	±15V		4		kΩ
C_{IN}	Input Capacitance		±15V		2.5		pF
	Input Voltage Range	G = 1	±15V ±5V ±2.5V	±15 ±5 ±1	±15.5 ±5.5 ±1.5		V V V
CMRR	Common Mode Rejection Ratio Referred to Input	G = 1, V_{CM} = ±15V G = 2, V_{CM} = ±15V G = 4, V_{CM} = ±15V G = 1, V_{CM} = ±5V G = 1, V_{CM} = ±1V	±15V ±15V ±15V ±5V ±2.5V	65 71 75 65 61	79 84 87 73 68		dB dB dB dB dB
PSRR	Power Supply Rejection Ratio	P1 = M1 = 0V, G = 1, V_S = ±2.5V to ±15V		78	87		dB
V_{OUT}	Output Voltage Swing	R_L = 1k R_L = 500Ω R_L = 500Ω R_L = 500Ω	±15V ±15V ±5V ±2.5V	±13.5 ±13 ±3.5 ±1.3	±14 ±13.5 ±4 ±2		V V V V
I_{SC}	Short-Circuit Current	G = 1	±15V	±70	±120		mA
SR	Slew Rate	G = –2, V_{OUT} = ±12V, P2 = 0V Measured at V_{OUT} = ±10V G = –2, V_{OUT} = ±3.5V, P2 = 0V Measured at V_{OUT} = ±2V	±15V ±5V	750	1000 450		V/µs V/µs
FPBW	Full Power Bandwidth	10V Peak, G = –2 (Note 8) 3V Peak, G = –2 (Note 8)	±15V ±5V		16 24		MHz MHz
HD	Total Harmonic Distortion	G = 1, f = 1MHz, R_L = 1k, V_{OUT} = $2V_{P-P}$	±15V		–81		dB
	–3dB Bandwidth	G = 1	±15V ±5V ±2.5V		32 25 21		MHz MHz MHz
t_r, t_f	Rise Time, Fall Time	10% to 90%, 0.1V, G = 1	±15V ±5V		10 15		ns ns
OS	Overshoot	0.1V, G = 1, C_L = 10pF	±15V ±5V		30 30		% %
t_{pd}	Propagation Delay	50% V_{IN} to 50% V_{OUT}, 0.1V, G = 1	±15V ±5V		9 11		ns ns
t_s	Settling Time	10V Step, 0.1%, G = 1 5V Step, 0.1%, G = 1	±15V ±5V		100 110		ns ns
ΔG	Differential Gain	G = 2, R_L = 150Ω	±15V		0.06		%
Δθ	Differential Phase	G = 2, R_L = 150Ω	±15V		0.15		Deg
R_{OUT}	Output Resistance	f = 1MHz, G = 1	±15V		1.5		Ω
I_S	Supply Current	G = 1	±15V ±5V		7.1 6.7	9.0 8.5	mA mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the 0°C ≤ T_A ≤ 70°C. Difference Amplifier Configuration. V_{REF} = V_{CM} = 0V and unused gain pins are unconnected, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
GE	Gain Error	V_{OUT} = ±12V, R_L = 1k, G = 1	±15V	●		0.05	0.25	%
		V_{OUT} = ±12V, R_L = 1k, G = 2	±15V	●		0.05	0.25	%
		V_{OUT} = ±12V, R_L = 1k, G = 4	±15V	●		0.05	0.25	%
		V_{OUT} = ±2.5V, R_L = 500Ω, G = 1	±5V	●		0.05	0.25	%
		V_{OUT} = ±2.5V, R_L = 150Ω, G = 1	±5V	●		0.05	0.35	%
V_{OS}	Input Offset Voltage Referred to Input (Note 7)	G = 1 (MS10)	±15V	●		1.1	6.5	mV
		G = 1 (DD10)	±15V	●		1.5	11.5	mV
		G = 2 (MS10)	±15V	●		0.8	5.5	mV
		G = 2 (DD10)	±15V	●		1.2	9	mV
		G = 4 (MS10)	±15V	●		0.7	5	mV
		G = 4 (DD10)	±15V	●		0.9	7.5	mV
		G = 1 (MS10)	±5V	●		1	6.5	mV
		G = 1 (DD10)	±5V	●		1.4	11.5	mV
		G = 1 (MS10)	±2.5V	●		1	6.5	mV
		G = 1 (DD10)	±2.5V	●		1.3	11.5	mV
V_{OS} TC	Input Offset Voltage Drift Referred to Input (Note 9)	G = 1 (MS10)	±15V	●		10	26	μV/°C
		G = 1 (DD10)	±15V	●		10	35	μV/°C
V_{OS_OA}	Op Amp Input Offset Voltage (Note 10)	G = 1 (MS10)	±2.5V, ±5V, ±15V	●		0.55	3.25	mV
		G = 1 (DD10)	±2.5V, ±5V, ±15V	●		0.75	5.75	mV
	Input Voltage Range	G = 1	±15V	●	±15	±15.5		V
			±5V	●	±5	±5.5		V
			±2.5V	●	±1	±1.5		V
CMRR	Common Mode Rejection Ratio Referred to Input	V_{CM} = ±15V, G = 1	±15V	●	63	77		dB
		V_{CM} = ±15V, G = 2	±15V	●	69	83		dB
		V_{CM} = ±15V, G = 4	±15V	●	73	86		dB
		V_{CM} = ±5V, G = 1	±5V	●	62	72		dB
		V_{CM} = ±1V, G = 1	±2.5V	●	59	66		dB
PSRR	Power Supply Rejection Ratio	P1 = M1 = 0V, G = 1, V_S = ±2.5V to ±15V		●	76	86		dB
V_{OUT}	Output Voltage Swing	R_L = 1k	±15V	●	±13.1	±14		V
		R_L = 500Ω	±15V	●	±12.6	±13.5		V
		R_L = 500Ω	±5V	●	±3.4	±4		V
		R_L = 500Ω	±2.5V	●	±1.2	±2		V
I_{SC}	Short-Circuit Current	G = 1	±15V	●	±55	±115		mA
SR	Slew Rate	G = –2, V_{OUT} = ±12V, P2 = 0V Measured at V_{OUT} = ±10V	±15V	●	600	900		V/μs
I_S	Supply Current	G = 1	±15V	●		7.9	10.5	mA
			±5V	●		7.4	9.9	mA

The ● denotes the specifications which apply over the –40°C ≤ T_A ≤ 85°C. Difference Amplifier Configuration. V_{REF} = V_{CM} = 0V and unused gain pins are unconnected, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
GE	Gain Error	V_{OUT} = ±12V, R_L = 1k, G = 1	±15V	●		0.05	0.3	%
		V_{OUT} = ±12V, R_L = 1k, G = 2	±15V	●		0.05	0.35	%
		V_{OUT} = ±12V, R_L = 1k, G = 4	±15V	●		0.05	0.35	%
		V_{OUT} = ±2.5V, R_L = 500Ω, G = 1	±5V	●		0.05	0.3	%
		V_{OUT} = ±2.5V R_L = 150Ω, G = 1	±5V	●		0.05	0.5	%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the –40°C ≤ T_A ≤ 85°C. Difference Amplifier Configuration. V_{REF} = V_{CM} = 0V and unused gain pins are unconnected, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	G = 1 (MS10)	±15V	●		1.2	7.5	mV
	Referred to Input (Note 7)	G = 1 (DD10)	±15V	●		1.6	13	mV
		G = 2 (MS10)	±15V	●		0.9	6	mV
		G = 2 (DD10)	±15V	●		1.2	10	mV
		G = 4 (MS10)	±15V	●		0.7	5.5	mV
		G = 4 (DD10)	±15V	●		0.9	8.5	mV
		G = 1 (MS10)	±5V	●		1.1	7.5	mV
		G = 1 (DD10)	±5V	●		1.4	13	mV
		G = 1 (MS10)	±2.5V	●		1.1	7.5	mV
		G = 1 (DD10)	±2.5V	●		1.5	13	mV
V_{OS} TC	Input Offset Voltage Drift	G = 1 (MS10)	±15V	●		10	26	µV/°C
	Referred to Input (Note 9)	G = 1 (DD10)	±15V	●		10	35	µV/°C
V_{OS_OA}	Op Amp Input Offset Voltage	G = 1 (MS10)	±2.5V, ±5V, ±15V	●		0.6	3.75	mV
	(Note 10)	G = 1 (DD10)	±2.5V, ±5V, ±15V	●		0.8	6.5	mV
	Input Voltage Range	G = 1	±15V	●	±15	±15.5		V
			±5V	●	±5	±5.5		V
			±2.5V	●	±1	±1.5		V
CMRR	Common Mode Rejection Ratio	V_{CM} = ±15V, G = 1	±15V	●	62	77		dB
	Referred to Input	V_{CM} = ±15V, G = 2	±15V	●	68	83		dB
		V_{CM} = ±15V, G = 4	±15V	●	72	86		dB
		V_{CM} = ±5V, G = 1	±5V	●	61	72		dB
		V_{CM} = ±1V, G = 1	±2.5V	●	57	66		dB
PSRR	Power Supply Rejection Ratio	P1 = M1 = 0V, G = 1, V_S = ±2.5V to ±15V		●	74	86		dB
V_{OUT}	Output Voltage Swing	R_L = 1k	±15V	●	±13	±14		V
		R_L = 500Ω	±15V	●	±12.5	±13.5		V
		R_L = 500Ω	±5V	●	±3.3	±4		V
		R_L = 500Ω	±2.5V	●	±1.1	±2		V
I_{SC}	Short-Circuit Current	G = 1	±15V	●	±50	±105		mA
SR	Slew Rate	G = –2, V_{OUT} = ±12V, P2 = 0V Measured at V_{OUT} = ±10V	±15V	●	550	900		V/µs
I_S	Supply Current	G = 1	±15V	●		8.0	11.0	mA
			±5V	●		7.6	10.4	mA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The inputs are protected by diodes connected to V_S^+ and $V_S^–$. If an input goes beyond the supply range, the input current should be limited to 10mA.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum.

Note 4: The LT1995C and LT1995I are guaranteed functional over the operating temperature range of –40°C to 85°C.

Note 5: The LT1995C is guaranteed to meet specified performance from 0°C to 70°C. The LT1995C is designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LT1995I is guaranteed to meet specified performance from –40°C to 85°C.

Note 6: Thermal resistance (θ_{JA}) varies with the amount of PC board metal connected to the leads. The specified values are for short traces connected to the leads. If desired, the thermal resistance can be reduced slightly in the MS package to about 130°C/W by connecting the used leads to a larger metal area. A substantial reduction in thermal resistance down to about 50°C/W can be achieved by connecting the Exposed Pad on the bottom of the DD package to a large PC board metal area which is either open-circuited or connected to $V_S^–$.

Note 7: Input offset voltage is pulse tested and is exclusive of warm-up drift. V_{OS} and V_{OS} TC refer to the input offset of the difference amplifier configuration. The equivalent input offset of the internal op amp can be calculated from $V_{OS\_OA} = V_{OS} \bullet G/(G+1)$.

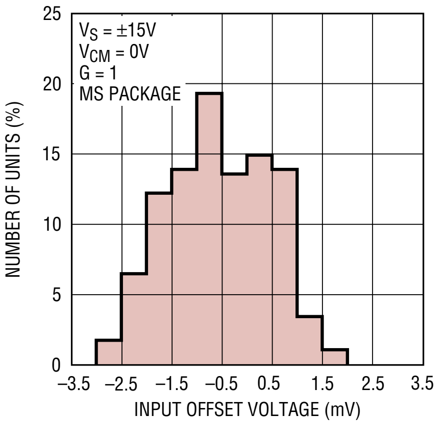
Note 8: Full Power bandwidth is calculated from the slew rate measurement: $FPBW = SR/2\pi V_P$.

Note 9: This parameter is not 100% tested.

Note 10: The input offset of the internal op amp is calculated from the input offset voltage: $V_{OS\_OA} = V_{OS} \bullet G/(G+1)$.

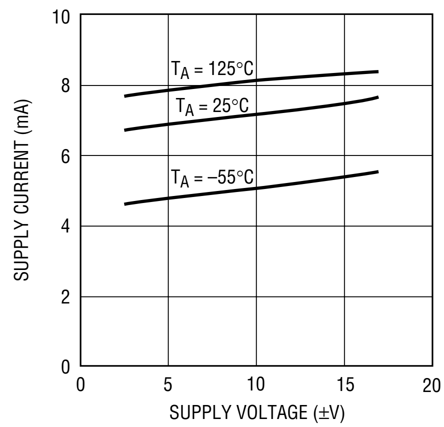
TYPICAL PERFORMANCE CHARACTERISTICS (Difference Amplifier Configuration)

V_{OS} Distribution



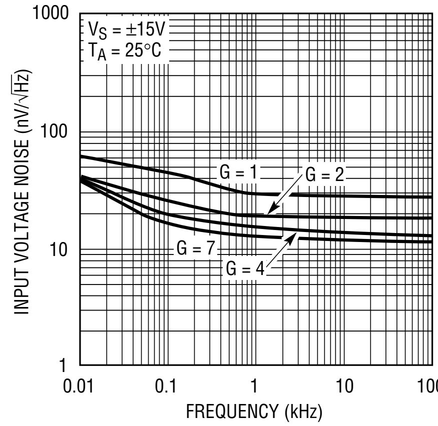
1995 G01

Supply Current vs Supply Voltage and Temperature



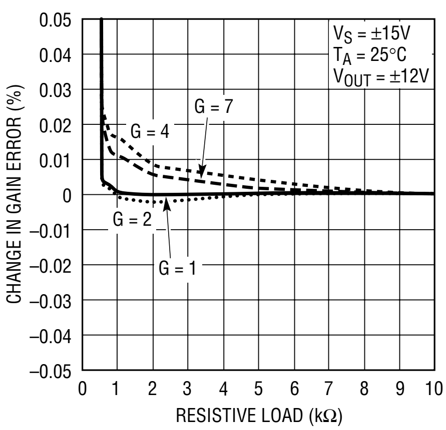
1995 G02

Input Noise Spectral Density



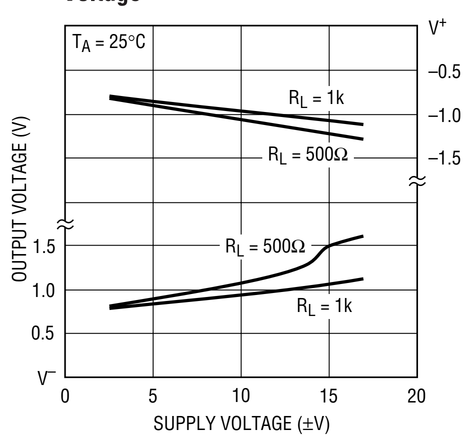
1995 G03

Change in Gain Error vs Resistive Load



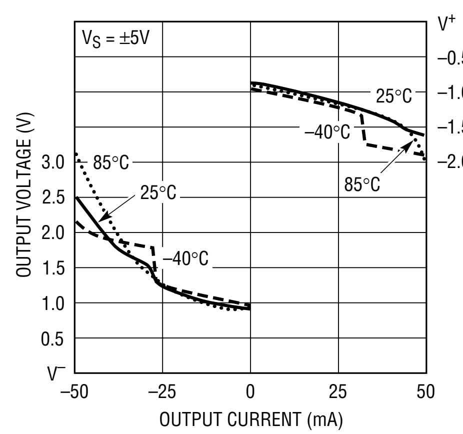
1995 G04

Output Voltage Swing vs Supply Voltage



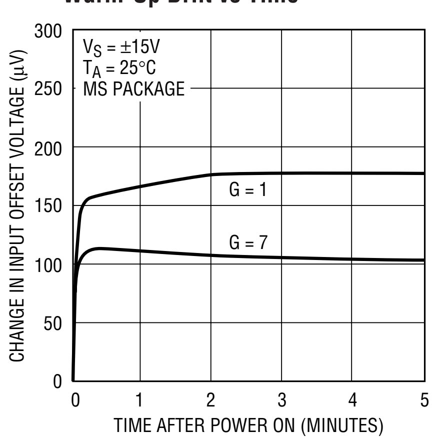
1995 G05

Output Voltage Swing vs Load Current



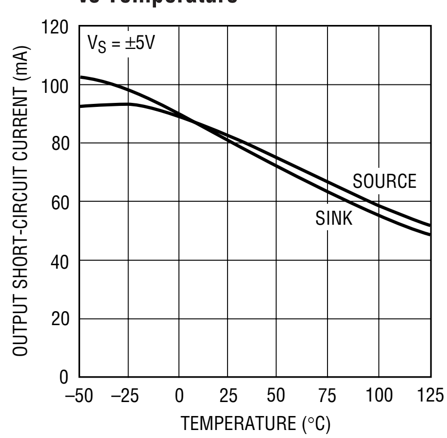
1995 G06

Warm-Up Drift vs Time



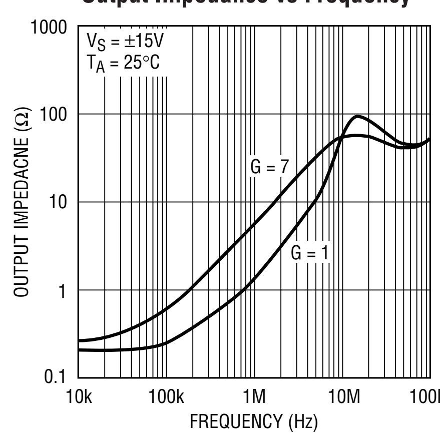
1995 G07

Output Short-Circuit Current vs Temperature



1995 G08

Output Impedance vs Frequency



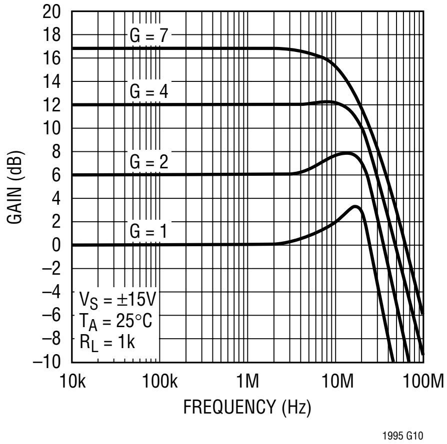
1995 G09

1995fb

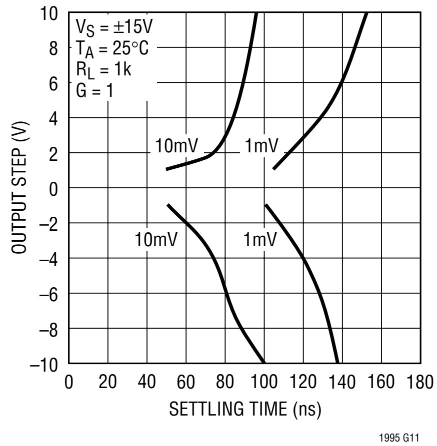
LINEAR TECHNOLOGY

TYPICAL PERFORMANCE CHARACTERISTICS (Difference Amplifier Configuration)

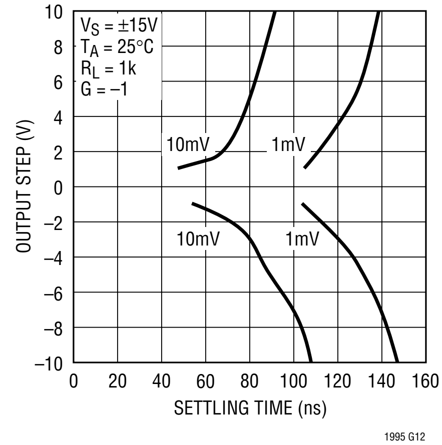
Gain vs Frequency



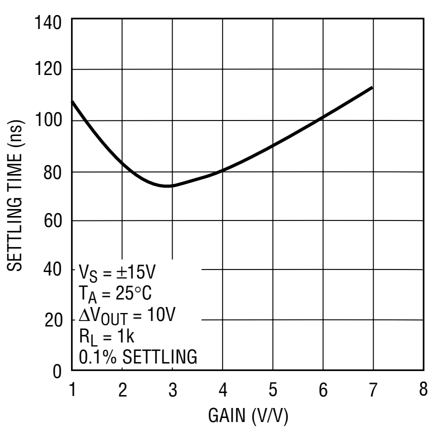
Settling Time vs Output Step (Non-Inverting)



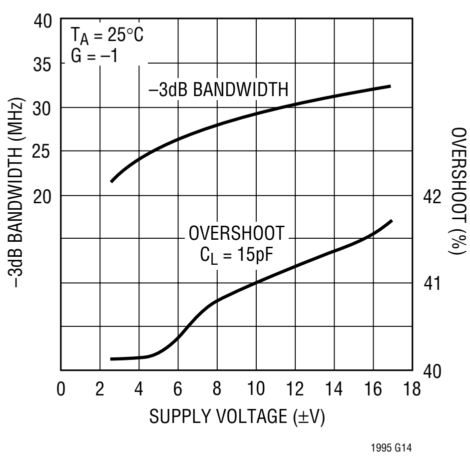
Settling Time vs Output Step (Inverting)



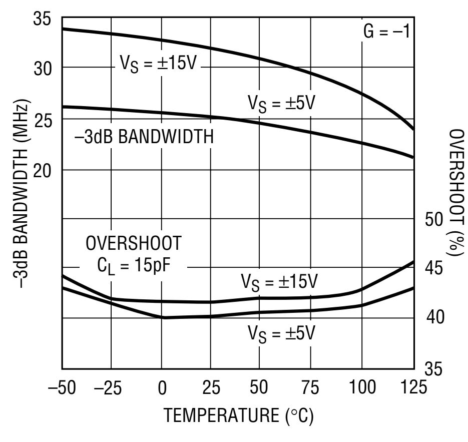
Settling Time vs Gain (Non-Inverting)



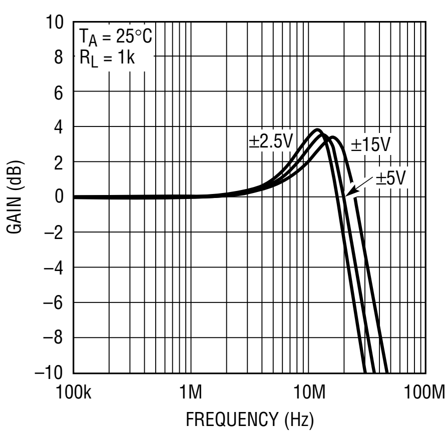
–3dB Bandwidth and Overshoot vs Supply Voltage



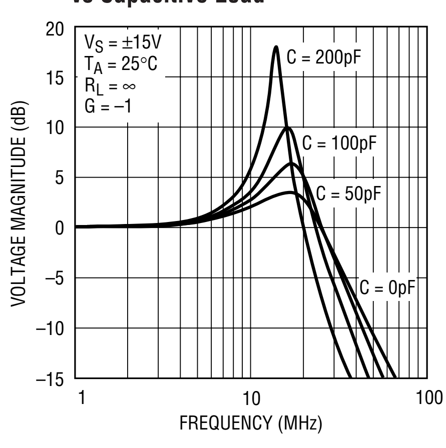
–3dB Bandwidth and Overshoot vs Temperature



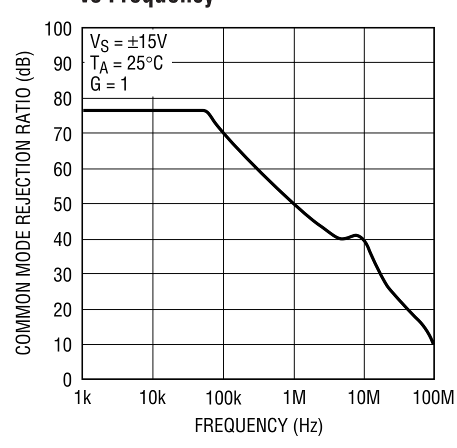
Frequency Response vs Supply Voltage (G = 1, G = –1)



Frequency Response vs Capacitive Load

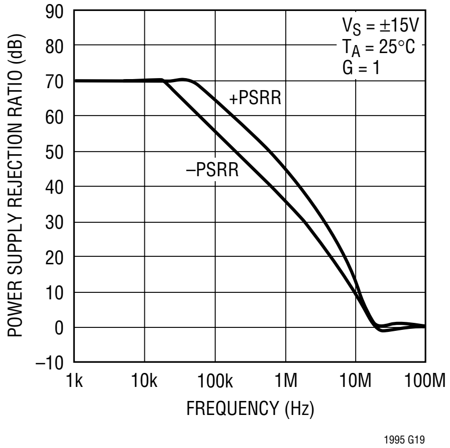


Common Mode Rejection Ratio vs Frequency

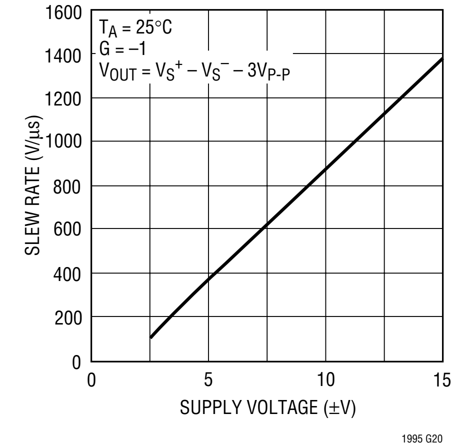


TYPICAL PERFORMANCE CHARACTERISTICS (Difference Amplifier Configuration)

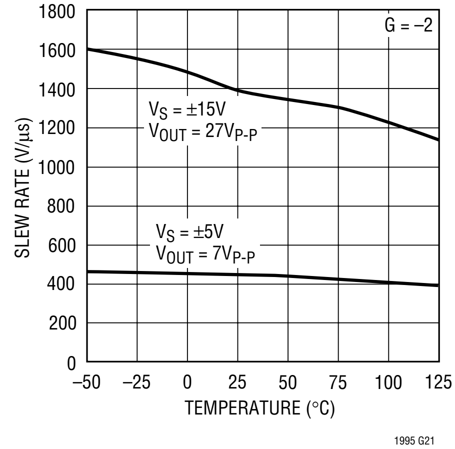
Power Supply Rejection Ratio vs Frequency



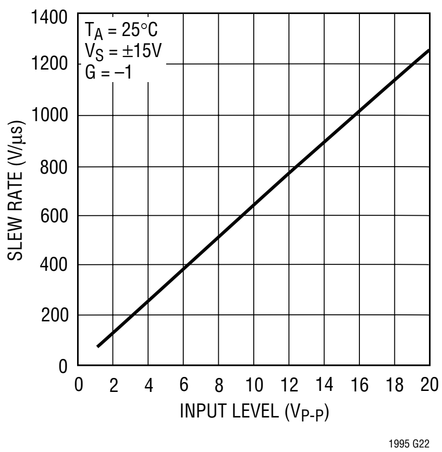
Slew Rate vs Supply Voltage



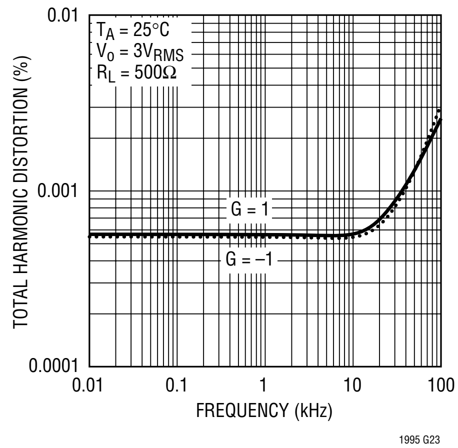
Slew Rate vs Temperature



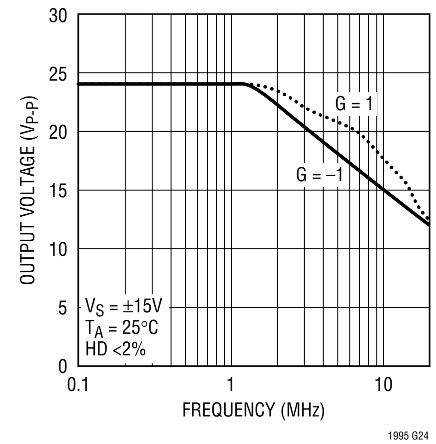
Slew Rate vs Input Level



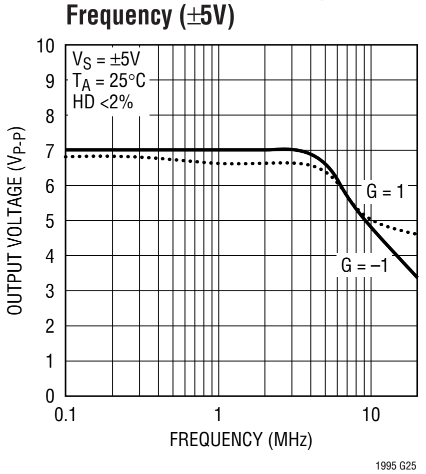
Total Harmonic Distortion vs Frequency



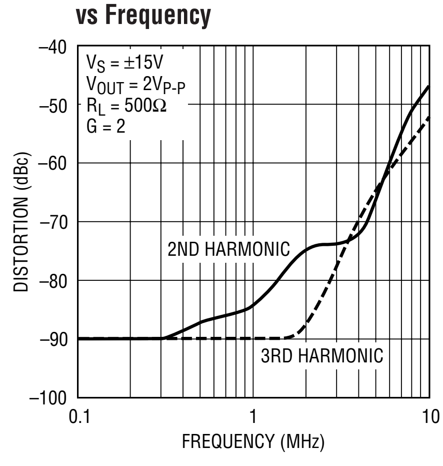
Undistorted Output Swing vs Frequency (±15V)



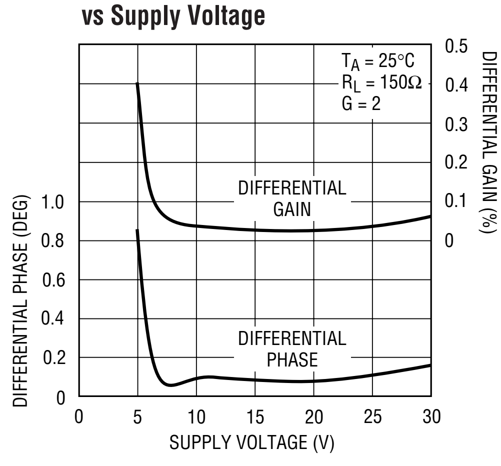
Undistorted Output Swing vs Frequency (±5V)



2nd and 3rd Harmonic Distortion vs Frequency



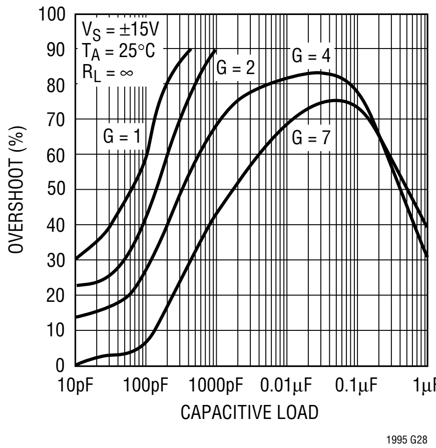
Differential Gain and Phase vs Supply Voltage



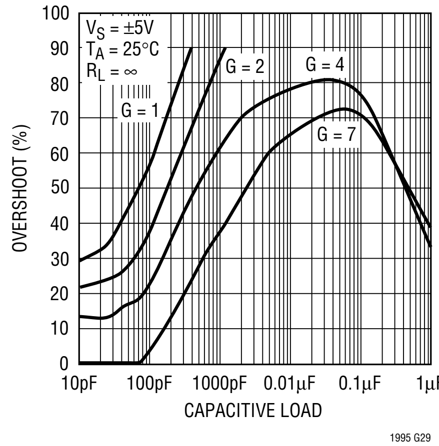
1995fb

TYPICAL PERFORMANCE CHARACTERISTICS (Difference Amplifier Configuration)

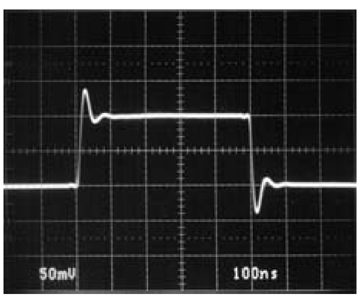
Capacitive Load Handling



Capacitive Load Handling

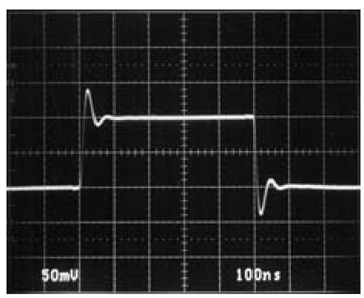


Small-Signal Transient (G = 1)



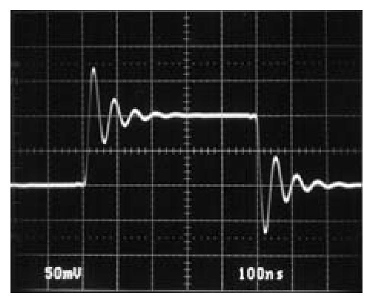
V_S = ±15V 100ns/DIV 1995 G30
R_L = 1k

Small-Signal Transient (G = –1)



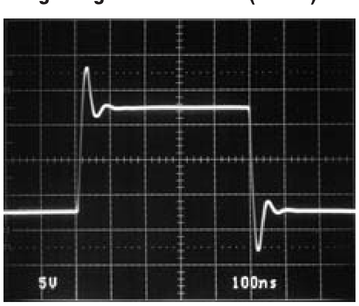
V_S = ±15V 100ns/DIV 1995 G31
R_L = 1k

Small-Signal Transient (Noninverting, G = 1, C_L = 100pF)



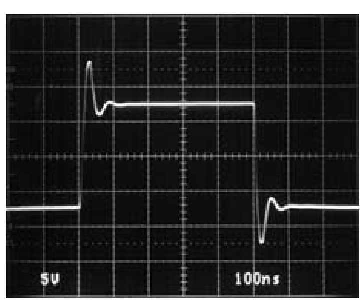
V_S = ±15V 100ns/DIV 1995 G32
R_L = 1k

Large-Signal Transient (G = 1)



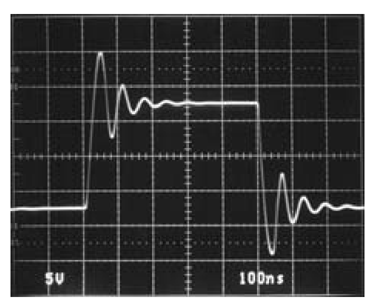
V_S = ±15V 100ns/DIV 1995 G33
R_L = 1k

Large-Signal Transient (G = –1)



V_S = ±15V 100ns/DIV 1995 G34
R_L = 1k

Large-Signal Transient (Noninverting, G = 1, C_L = 100pF)



V_S = ±15V 100ns/DIV 1995 G35
R_L = 1k

PIN FUNCTIONS (Difference Amplifier Configuration)

P1 (Pin 1): Noninverting Gain-of-1 Input. Connects a 4k internal resistor to the op amp's noninverting input.

P2 (Pin 2): Noninverting Gain-of-2 Input. Connects a 2k internal resistor to the op amp's noninverting input.

P4 (Pin 3): Noninverting Gain-of-4 Input. Connects a 1k internal resistor to the op amp's noninverting input.

V_S^- (Pin 4): Negative Supply Voltage.

REF (Pin 5): Reference Voltage. Sets the output level when the difference between the inputs is zero. Connects a 4k internal resistor to the op amp's non inverting input.

OUT (Pin 6): Output Voltage. $V_{OUT} = V_{REF} + 1 \bullet (V_{P1} – V_{M1}) + 2 \bullet (V_{P2} – V_{M2}) + 4 \bullet (V_{P4} – V_{M4})$.

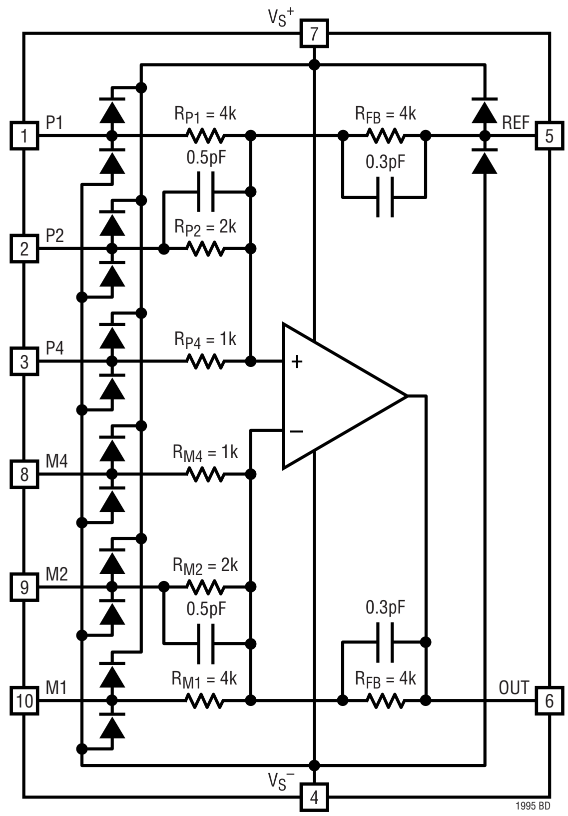
V_S^+ (Pin 7): Positive Supply Voltage.

M4 (Pin 8): Inverting Gain-of-4 Input. Connects a 1k internal resistor to the op amp's inverting input.

M2 (Pin 9): Inverting Gain-of-2 Input. Connects a 2k internal resistor to the op amp's inverting input.

M1 (Pin 10): Inverting Gain-of-1 Input. Connects a 4k internal resistor to the op amp's inverting input.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Configuration Flexibility

The LT1995 combines a high speed precision operational amplifier with eight ratio-matched on-chip resistors. The resistor configuration and pinout of the device is shown in the Block Diagram. The topology is extremely versatile and provides for simple realizations of most classic functional configurations including difference amplifiers, inverting gain stages, noninverting gain stages (including Hi-Z input buffers) and summing amplifiers. The LT1995 delivers load currents of at least 30mA, making it ideal for cable driving applications as well.

The input voltage range depends on gain and configuration. ESD diodes will clamp any input voltage that exceeds the supply potentials by more than several tenths of a volt; and the internal op amp input ports must remain at least 1.75V within the rails to assure normal operation of the part. The output will swing to within one and a half volts of the rails, which in low supply voltage and high gain configurations will create a limitation on the usable input range. It should be noted that while the internal op amp can withstand transient differential input voltages of up to 10V without damage, this does generate large supply current increases (tens of mA) as required for high slew rates. If the device is used with sustained differential input across the internal op amp (such as when the output is clipping), the average supply current will increase, excessive power dissipation will result, and the part may be damaged (i.e., **the LT1995 is not recommended for use in comparator applications or with the output clipped).**

Difference Amplifier

The LT1995 can be connected as a classic difference amplifier with an output function given by:

$$V_{OUT} = G \bullet (V_{IN}^{+} - V_{IN}^{-}) + V_{REF}$$

APPLICATIONS INFORMATION

As shown in Figure 1, the options for fixed gain G include: 1, 1.33, 1.67, 2, 3, 4, 5, 6 and 7, all achieved by pin-strapping alone. With split-supply applications where the output is to be ground referenced, the V_{REF} input is simply tied to ground. The input common mode voltage is rejected by the high CMRR of the part within the usable input range.

Inverting Gain Amplifier

The LT1995 can be connected as an inverting gain amplifier with an output function given by:

$$V_{OUT} = -(G \bullet V_{IN}^-) + V_{REF}$$

As shown in Figure 1, the options for fixed gain G include: 1, 1.33, 1.67, 2, 3, 4, 5, 6 and 7, all achieved by pin strapping alone. The V_{IN}^+ connection used in the difference amp configuration is simply tied to ground (or a low impedance potential equal to the input signal bias to create an input "virtual ground"). With split-supply applications where the output is to be ground referenced, the V_{REF} input is simply tied to ground as well.

Noninverting Gain Buffer Amplifier

The LT1995 can be connected as a high input impedance noninverting gain buffer amplifier with an output function given by:

$$V_{OUT} = G \bullet V_{IN}$$

As shown in Figure 2, the options for fixed gain G include: 1, 1.14, 1.2, 1.33, 1.4, 1.6, 2, 2.33, 2.66, 3, 4, 5, 6, 7 and 8, all achieved by pin strapping alone. With single supply applications, the grounded M input pins may be tied to a low impedance potential equal to the input signal bias to create a "virtual ground" for both the input and output signals. While there is no input attenuation from V_{IN} to the internal noninverting op amp port in these configurations, the P connections vary to minimize offset by providing balanced input resistances to the internal op amp.

Noninverting Gain Amplifier Input Attenuation

The LT1995 can also be connected as a noninverting gain amplifier having an input attenuation network to provide a wide range of additional noninverting gain options. In combination with the feedback configurations for gains of G shown in Figure 2 (connections to the M inputs), the P and REF inputs may be connected to form several resistor divider attenuation ratios A, so that a compound output function is given by:

$$V_{OUT} = A \bullet G \bullet V_{IN}$$

As shown in Figure 3, the options for fixed attenuation A include 0.875, 0.857, 0.833, 0.8, 0.75, 0.714, 0.667, 0.625 and 0.571, all achieved by pin strapping alone. With just the attenuation configurations of Figure 3 and the feedback configurations of Figure 2, seventy-three unique composite gains in the range of 1 to 8 are available (many options for gain below unity also exist). Figure 3 does not include the additional pin-strap configurations offering A values of 0.5, 0.429, 0.375, 0.333, 0.286, 0.25, 0.2, 0.167, 0.143 and 0.125, as these values tend to compromise the low noise performance of the part and don't generally contribute many more unique gain options. It should be noted that with these configurations some degree of imbalance will generally exist between the effective resistances R_P and R_M seen by the internal op amp input ports, noninverting and inverting, respectively. Depending on the specific combination of A and G, the following DC offset error due to op amp input bias current (I_B) should be anticipated: The I_B of the internal op amp is typically 0.6µA and is prepackage tested to a limit of 2µA. Additional output-referred offset = $I_B \bullet (R_P - R_M) \bullet G$. In some configurations, this could be as much as 1.7mV • G additional output offset. The I_{OS} of the internal op amp is typically 120nA and is prepackage tested to a limit of 350nA. The Electrical Characteristics table includes the effects of I_B and I_{OS}.

APPLICATIONS INFORMATION

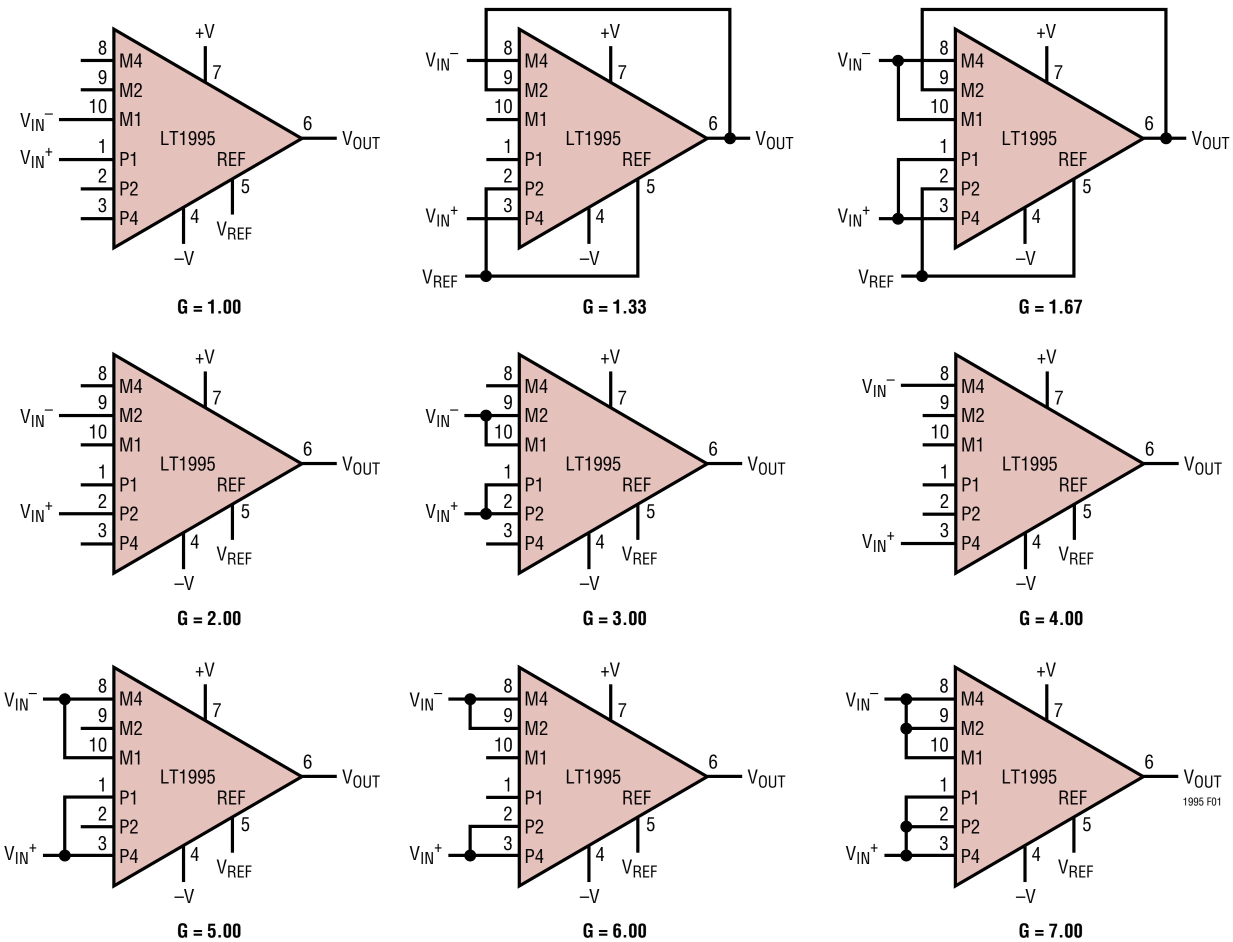


Figure 1. Difference (and Inverting) Amplifier Configurations

Table 1. Pin Use, Input Range, Input Resistance, Bandwidth in Difference Amplifier Configuration

GAIN	1	2	3	4	5	6	7
Use of P1/M1	V_{IN}	Open	V_{IN}	Open	V_{IN}	Open	V_{IN}
Use of P2/M2	Open	V_{IN}	V_{IN}	Open	Open	V_{IN}	V_{IN}
Use of P4/M4	Open	Open	Open	V_{IN}	V_{IN}	V_{IN}	V_{IN}
Positive Input Range: V_{REF} = 0V, V_S = ±15V	±15V	±15V	±15V	±15V	±15V	±15V	±15V
Positive Input Range: V_{REF} = 0V, V_S = ±5V	±5V	±4.88V	±4.33V	±4.06V	±3.9V	±3.79V	±3.71V
Positive Input Range: V_{REF} = 0V, V_S = ±2.5V	±1.5V	±1.13V	±1V	±0.94V	±0.9V	±0.88V	±0.86V
Positive Input Resistance	8k	6k	5.33k	5k	4.8k	4.67k	4.57k
Minus Input Resistance	4k	2k	1.33k	1k	800Ω	667Ω	571Ω
Ref Input Resistance	8k	6k	5.33k	5k	4.8k	4.67k	4.57k
Input Common Mode Resistance, V_{REF} = 0V	4k	3k	2.67k	2.5k	2.4k	2.33k	2.29k
Input Differential Mode Resistance, V_{REF} = 0V	8k	4k	2.67k	2k	1.6k	1.33k	1.14k
–3dB Bandwidth	32MHz	27MHz	27MHz	23MHz	18MHz	16MHz	15MHz

APPLICATIONS INFORMATION

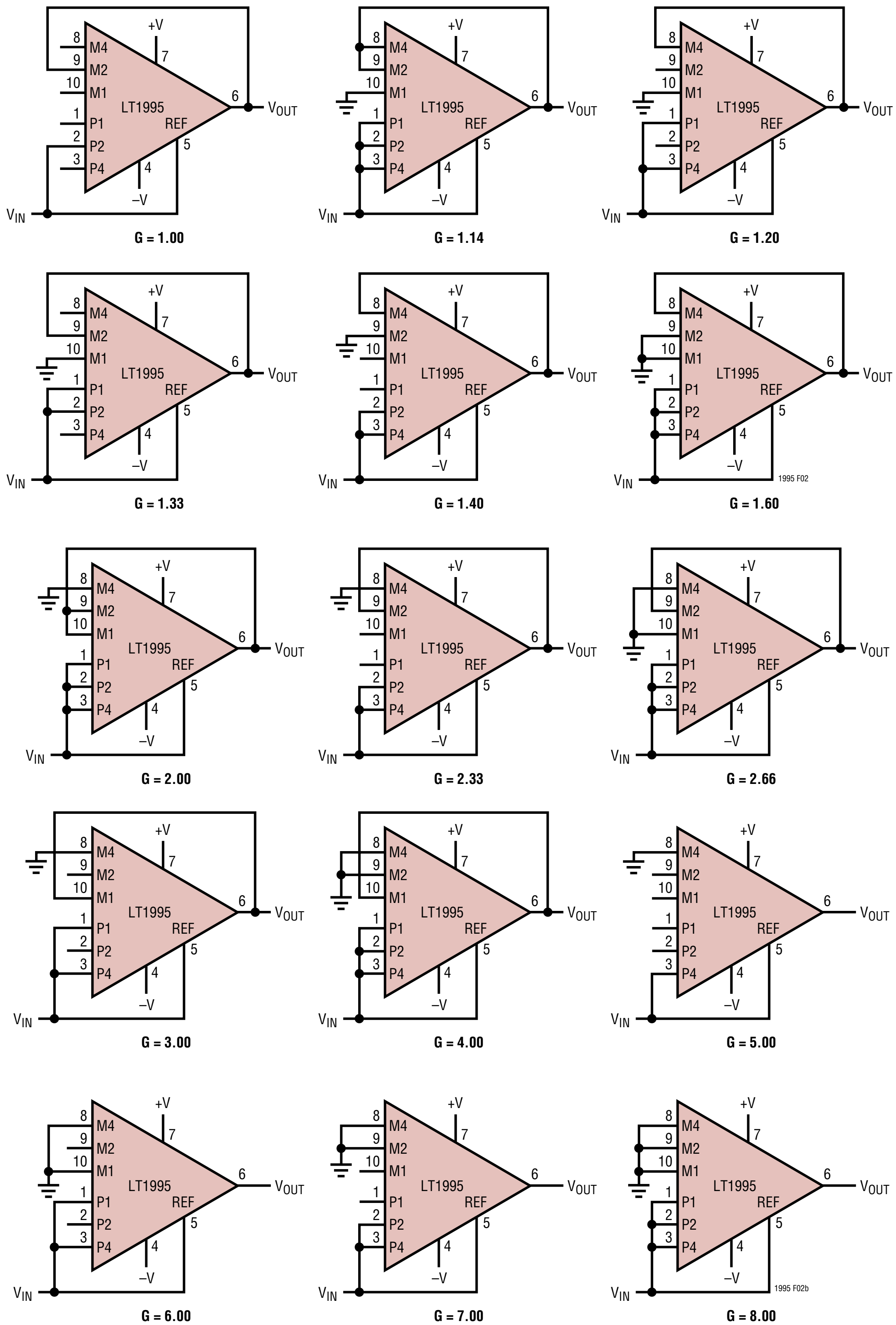
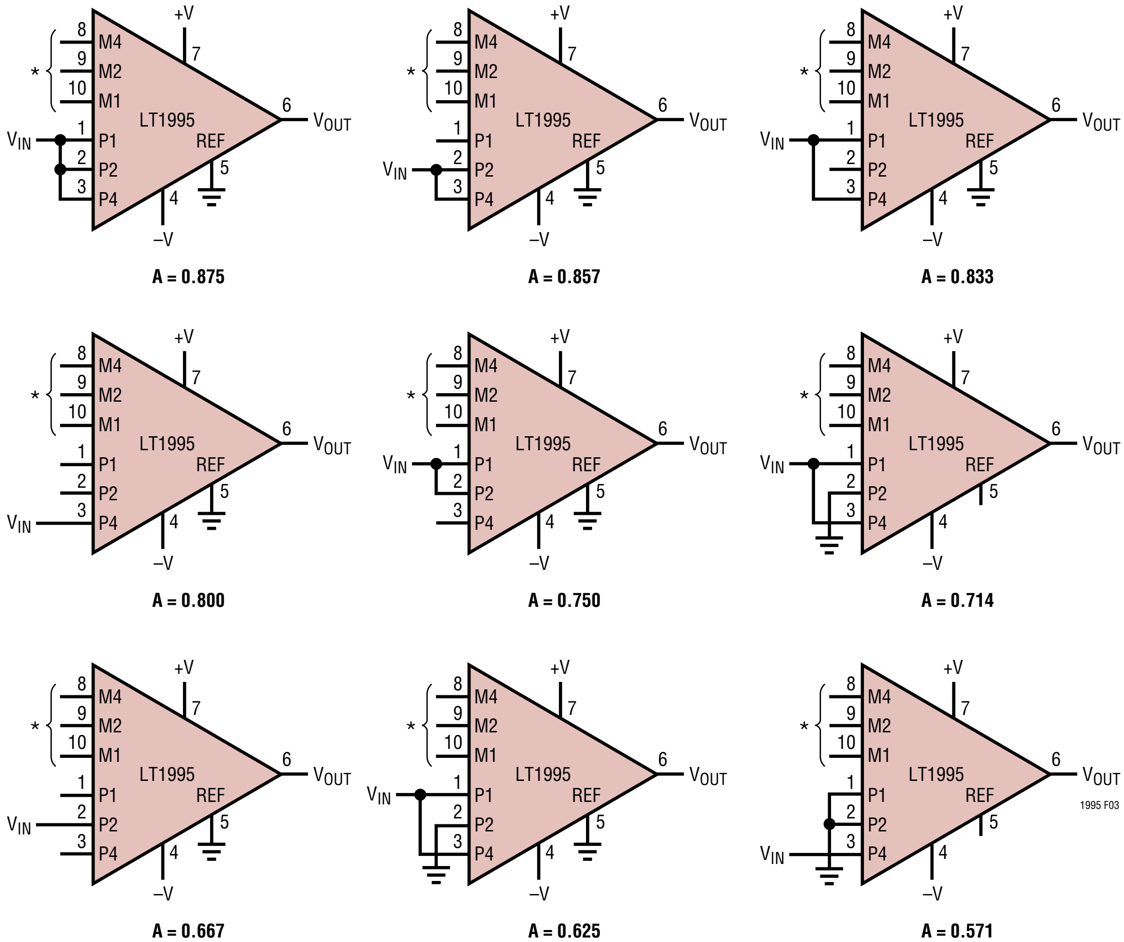


Figure 2. Noninverting Buffer Amplifier Configurations (Hi-Z Input)

APPLICATIONS INFORMATION



*CONFIGURE M INPUTS FOR DESIRED G PARAMETER; REFER TO FIGURE 2 FOR CONNECTIONS

Figure 3. Noninverting Amplifier Input Attenuation Configurations (A > 0.5)

AC-Coupling Methods for Single Supply Operation

The LT1995 can be used in many single-supply applications using AC-coupling without additional biasing circuitry.

AC-coupling the LT1995 in a difference amplifier configuration (as in Figure 1) is a simple matter of adding coupling capacitors to each input and the output as shown in the example of Figure 5. The input voltage V_{BIAS} applied to the REF pin establishes the quiescent voltage on the input and output pins. The V_{BIAS} signal should have a low source impedance to avoid degrading the CMRR (0.5Ω for 1dB CMRR change typically).

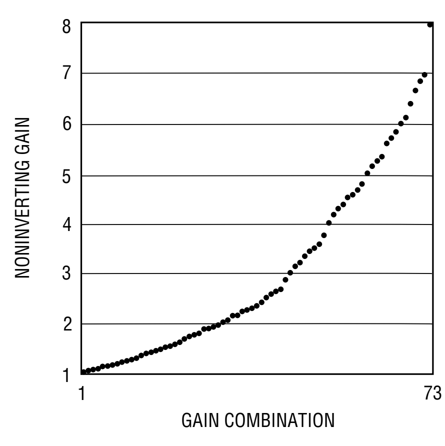


Figure 4. Unique Noninverting Gain Configurations

APPLICATIONS INFORMATION

Using the LT1995 as an AC-coupled inverting gain stage, the REF pin and the relevant P inputs may all be driven from a V_{BIAS} source as depicted in the example of Figure 6, thus establishing the quiescent voltage on the input and output pins. The V_{BIAS} signal will only have to source the bias current (I_B) of the noninverting input of the internal op amp (0.6µA typically), so a high V_{BIAS} source impedance (R_S) will cause the quiescent level of the amplifier output to deviate from the intended V_{BIAS} level by $I_B \bullet R_S$.

In operation as a noninverting gain stage, the P and REF inputs may be configured as a "supply splitter," thereby providing a convenient mid-supply operating point. Figure 7 illustrates the three attenuation configurations that generate 50% mid-supply biasing levels with no external components aside from the desired coupling capacitors. As with the DC-coupled input attenuation ratios, A, a compound output function including the feedback gain parameter G is given by:

$$V_{OUT} = A \bullet G \bullet V_{IN}$$

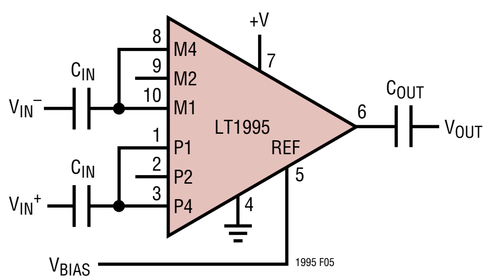


Figure 5. AC-Coupled Difference Amplifier General Configuation (G = 5 Example)

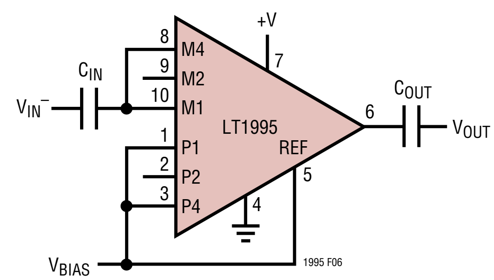


Figure 6. AC-Coupled Inverting Gain Amplifier General Configuration (G = 5 Example)

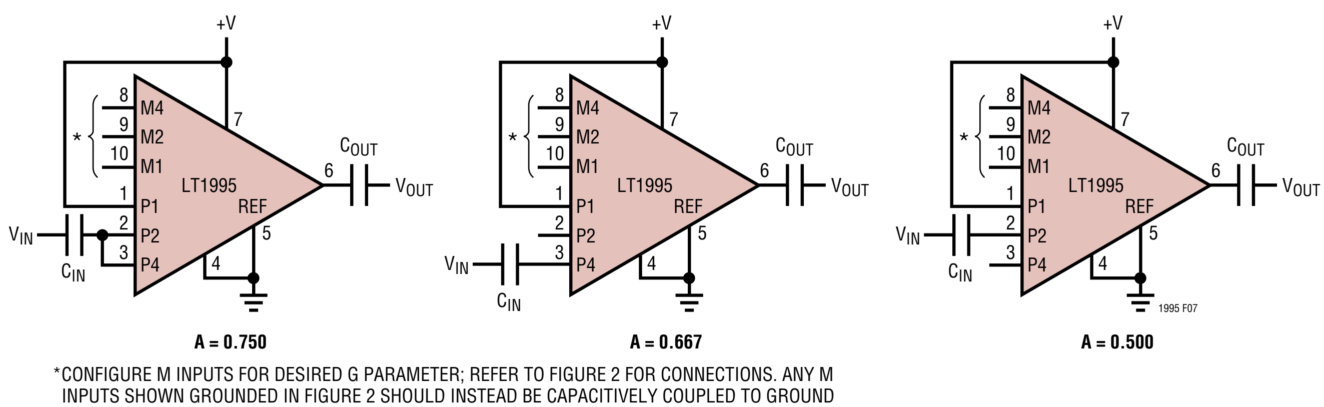


Figure 7. AC-Coupled Noninverting Amplifier Input Attenuation Configurations (Supply Splitting)

APPLICATIONS INFORMATION

If one of the A parameter configurations in Figure 3 is preferred, or the use of an external biasing source is desired, the P and REF input connections shown grounded in a Figure 3 circuit may be instead driven by a V_{BIAS} voltage to establish a quiescent operating point for the input and output pins. The V_{IN} connections of the Figure 3 circuit are then driven via a coupling capacitor. Any grounded M inputs for the desired G configuration (refer to Figure 2) must be individually or collectively AC-coupled to ground. Figure 8 illustrates a complete example circuit of an externally biased AC-coupled noninverting amplifier. The V_{BIAS} source impedance should be low (a few ohms) to avoid degrading the inherent accuracy of the LT1995. 0.013% of additional Gain Error for each ohm of resistance on the REF pin is typical.

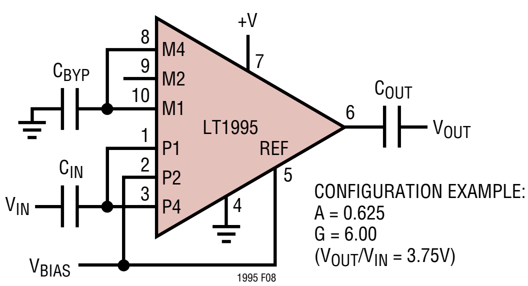


Figure 8. AC-Coupled Noninverting Amplifier with External Bias Source (Example)

Resistor Considerations

The resistors in the LT1995 are very well matched, low temperature coefficient thin film based elements. Although their absolute tolerance is fairly wide (typically ±5% but ±25% worst case), the resistor matching is to within 0.2% at room temperature, and to within 0.3% over temperature. The temperature coefficient of the resistors is typically –30ppm/°C. The resistors have been sized to accommodate 15V across each resistor, or in terms of power, 225mW in the 1k resistors, 113mW in the 2k resistors, and 56mW in the 4k resistors.

Power Supply Considerations

As with any high speed amplifier, the LT1995 printed circuit layout should utilize good power supply decoupling practices. Good decoupling will typically consist of one or more capacitors employing the shortest practical interconnection traces and direct vias to a ground plane. This practice minimizes inductance at the supply pins so the impedance is low at the operating frequencies of the part, thereby suppressing feedback or crosstalk artifacts that might otherwise lead to extended settling times, frequency response anomalies, or even oscillation. For high speed parts like the LT1995, 10nF ceramics are suitable close-in bypass capacitors, and if high currents are being delivered to a load, additional 4.7µF capacitors in parallel can help minimize induced power supply transients.

Because unused input pins are connected via resistors to the input of the op amp, excessive capacitances on these pins will degrade the rise time, slew rate, and step response of the output. Therefore, these pins should not be connected to large traces which would add capacitance when not in use.

Since the LT1995 has a wide operating supply voltage range, it is possible to place the part in situations of relatively high power dissipation that may cause excessive die temperatures to develop. Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A)

APPLICATIONS INFORMATION

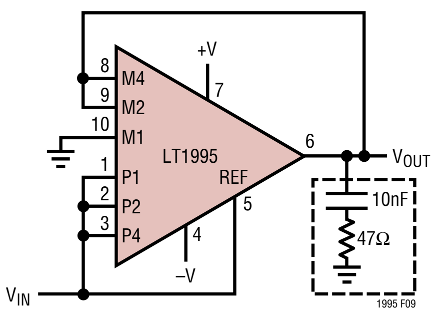
and power dissipation (P_D) as follows for a nominal PCB layout:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

For example, in order to maintain a maximum junction temperature of 150°C at 85°C ambient in an MS10 package, the power must be limited to 0.4W. It is important to note that when operating at ±15V supplies, the quiescent current alone will typically account for 0.24W, so careful thermal management may be required if high load currents and high supply voltages are involved. By additional copper area contact to the supply pins or effective thermal coupling to extended ground plane(s), the thermal impedance can be reduced to 130°C/W in the MS10 package. A substantial reduction in thermal impedance of the DD10 package down to about 50°C/W can be achieved by connecting the Exposed Pad on the bottom of the package to a large PC board metal area which is either open-circuited or connected to V_S^-.

Frequency Compensation

The LT1995 comfortably drives heavy resistive loads such as back-terminated cables and provides nicely damped responses for all gain configurations when doing so. Small capacitances are included in the on-chip resistor network to optimize bandwidth in the basic difference gain configurations of Figure 1. For the noninverting configurations of Figure 2, where the gain parameter G is 2 or less, significant overshoot can occur when driving light loads. For these low gain cases, providing an RC output network as shown in Figure 9 to create an artificial load at high frequency will assure good damping behavior.



CONFIGURATION EXAMPLE:
G = 1.14

Figure 9. Optional Frequency Compensation Network for (1 ≤ G ≤ 2)

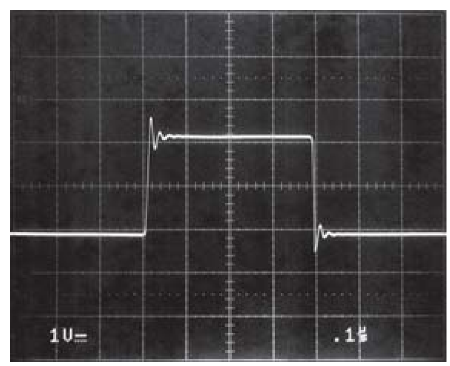
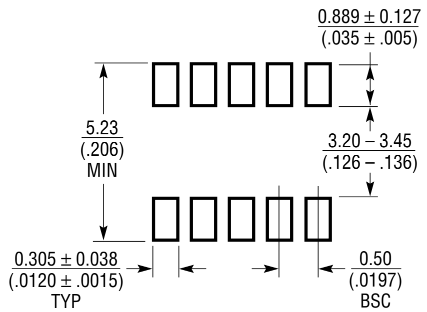


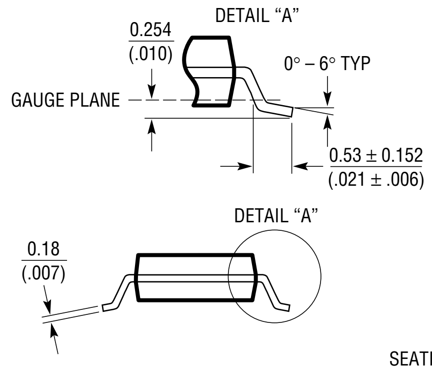
Figure 10. Step Response of Circuit in Figure 9

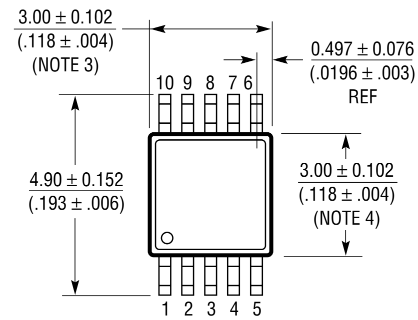
PACKAGE DESCRIPTION

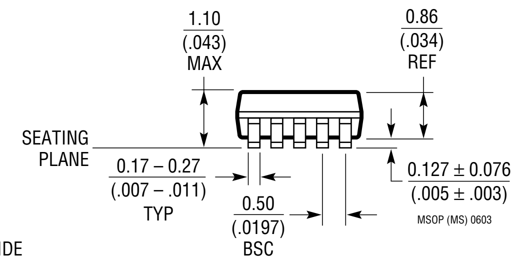
MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661)



RECOMMENDED SOLDER PAD LAYOUT

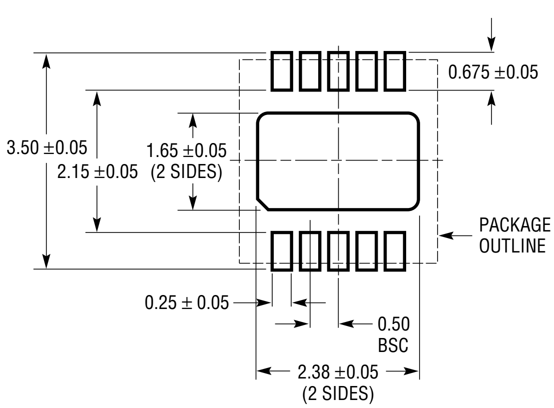




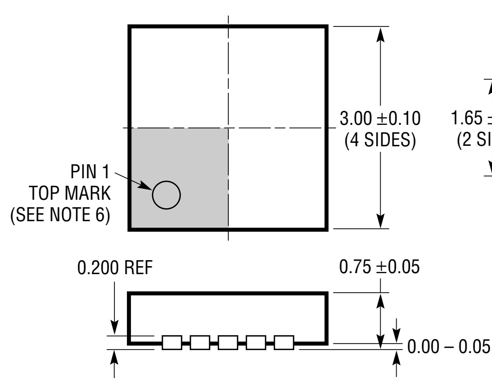


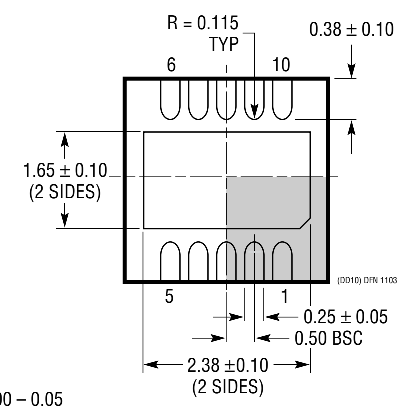
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



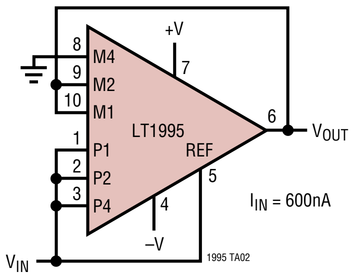


BOTTOM VIEW—EXPOSED PAD

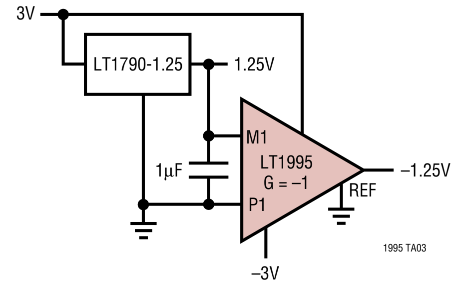
NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATIONS

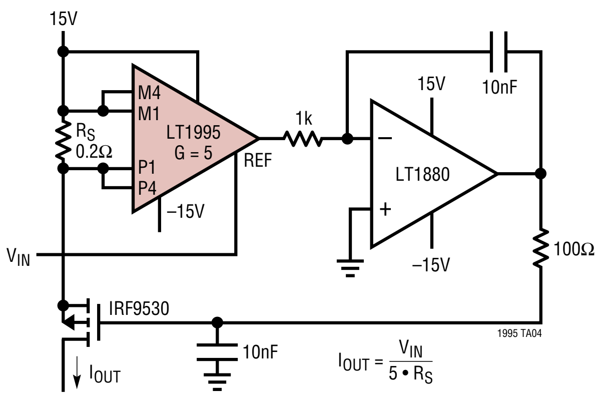
High Input Impedance Precision Gain of 2 Configuration



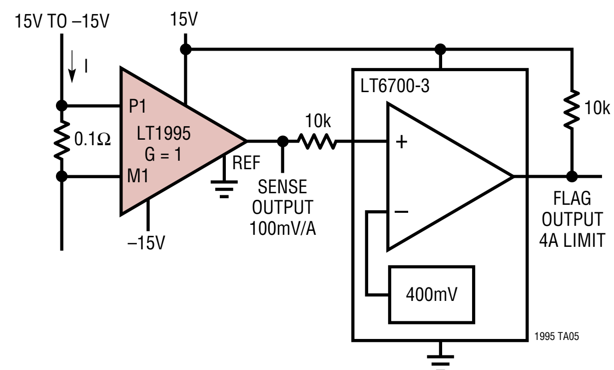
Tracking Negative Reference



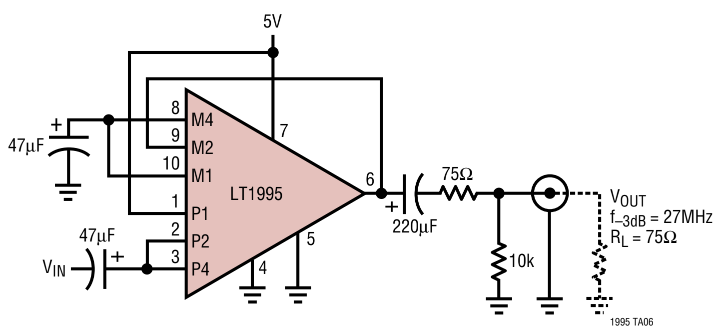
0A to 2A Current Source



Current Sense with Alarm



Single Supply Video Line Driver



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1363	70MHz, 1000V/µs Op Amp	50ns Settling Time to 0.1%, C_{LOAD} Stable
LT1990	High Voltage Difference Amplifier	±250V Common Mode Voltage, Micropower, Pin Selectable G = 1, 10
LT1991	Precision Gain Selectable Amplifier	Micropower, Precision, Pin Selectable G = –13 to 14
LTC1992	Fully Differential Amplifier	Differential Input and Output, Rail-to-Rail Output, I_S = 1.2mA, C_{LOAD} Stable to 10,000pF, Adjustable Common Mode Voltage
LTC6910-x	Programmable Gain Amplifiers	3 Gain Configurations, Rail-to-Rail Input and Output

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

LT/LT 0805 REV B • PRINTED IN THE USA