Synchronous MOSFET Gate Driver IC

FEATURES

- 7V/2A gate drivers (5A GATEL sink current)
- 15ns adaptive non-overlap control
- Integrated boot-strap synchronous PFET
- Supports 3.3V and 5V PWM input signals
- Tri-State PWM input for power stage shutdown
- Sub 50ns minimum pulse width supports 2MHz per-phase operation
- Dual function EN/UV pin provides Enable input and power good output
- Small thermally enhanced 8L SON & 3 x 3mm MLPD packages
- RoHS compliant

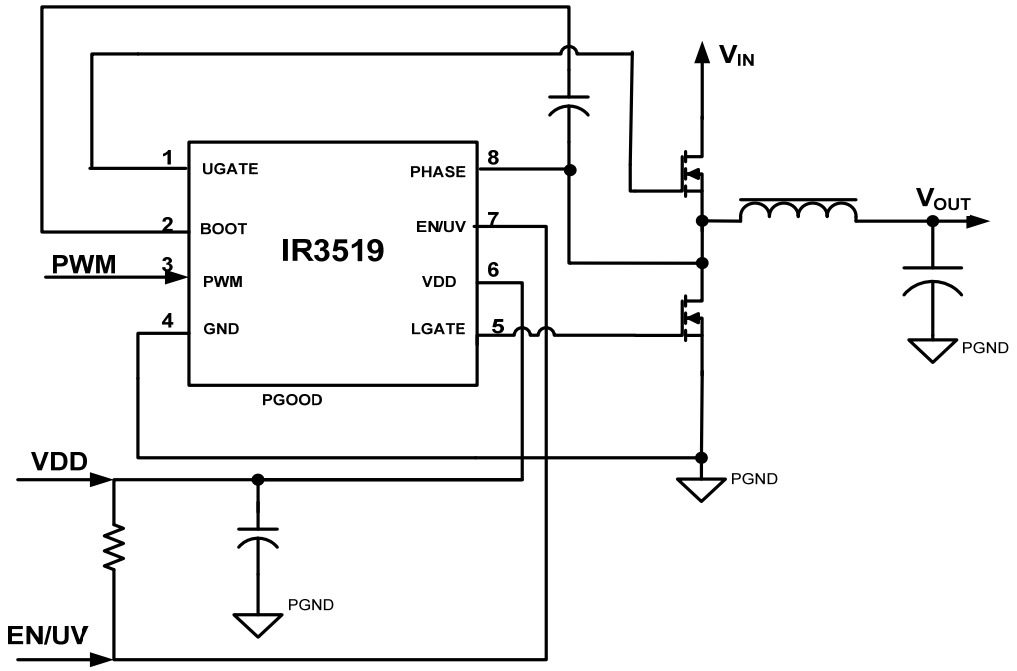
DESCRIPTION

The IR3519 is extended voltage range high-speed gate driver optimized for switching power supply applications. Performance is achieved by 7V/2A gate source and 5-A sink drive capability and is capable of operating at frequencies of up to 2MHz.

The 0.4-Ω impedance of the lower gate driver holds the gate of the Synchronous MOSFET below its threshold to prevent shoot-through current during high dv/dt phase node transitions.

The IR3519 includes a two-way enable/under voltage power good signal. Systems without 3-state featured controllers can use the EN/UV input/output to hold both outputs low during converter shut down.

APPLICATION CIRCUIT



ORDER INFORMATION

Device	Package	Order Quantity
IR3519MTRPBF	8 Lead MLPD (3 x 3 mm body)	3000 per reel
* IR3519MPBF	8 Lead MLPD (3 x 3 mm body)	100 piece strips
IR3519STRPBF	8 Lead SON	2500 per reel
* IR3519SPBF	8 Lead SON	95 per tube

* Samples only

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings (Referenced to GND)
BOOT Voltage: ..... 40 V
PH Voltage: .....-5V(100ns),-0.3V(DC) to 35 V
UGATE Voltage: .....-5V(100ns),-0.3V(DC) to 40 V
LGATE Voltage: .....-5V(100ns),-0.3V(DC) to 8 V
BOOT - PH Voltage: ..... -0.3V to 8 V
UGATE - PH Voltage: ..... -0.3V to 8 V
VDD: ..... 8 V
GND: ..... -0.3V to 0.3V
All other pins ..... -0.3V to 8 V

Operating Junction Temperature .. -10°C to +150°C
MSL Rating ..... Level 2
Reflow Temperature ..... 260°C
Storage Temperature Range ..... -65°C to 150°C
ESD Rating ..... HBM Class 1C JEDEC Standard

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

RECOMMENDED OPERATING CONDITIONS

6.5V≤ VDD ≤ 7.5V, 0 °C ≤ T_J ≤ 125 °C

ELECTRICAL SPECIFICATIONS

The electrical characteristics involve the spread of values guaranteed within the recommended operating conditions. Typical values represent the median values, which are related to 25°C. C_{UGATE} = 3.3nF, C_{LGATE} = 6.8nF (unless otherwise specified).

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Gate Drivers					
UGATE Source Resistance	BOOT – PH = 7V. Note 1		1.0	2.5	Ω
UGATE Sink Resistance	BOOT – PH = 7V. Note 1		1.0	2.5	Ω
LGATE Source Resistance	VDD –GND = 7V. Note 1		1.0	2.5	Ω
LGATE Sink Resistance	VDD – GND = 7V. Note 1		0.4	1.0	Ω
UGATE Source Current	BOOT=7V, UGATE=3.5V, SW=0V. Note 1		2.0		A
UGATE Sink Current	BOOT=7V, UGATE=3.5V, SW=0V. Note 1		2.0		A
LGATE Source Current	VDD=7V, LGATE=3.5V, GND=0V. Note 1		2.0		A
LGATE Sink Current	VDD=7V, LGATE=3.5V, GND=0V. Note 1		5.0		A
UGATE Rise Time	BOOT – PH = 7V, measure 1V to 4V transition time.		5		ns
UGATE Fall Time	BOOT - PH = 7V, measure 4V to 1V transition time.		5		ns
LGATE Rise Time	VDD – GND = 7V, Measure 1V to 4V transition time.		10		ns
LGATE Fall Time	VDD – GND = 7V, Measure 4V to 1V transition time.		5		ns

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
LGATE low to UGATE high delay	BOOT = VDD = 7V, PH =0V GND = 0V, measure time from LGATE falling to 1V to UGATE rising to 1V.	5	15		ns
UGATE low to LGATE high delay	BOOT = VDD = 7V, PH =0V GND = 0V, measure time from UGATE falling to 1V to LGATE rising to 1V.	5	15		ns
Minimum Pulse Width	Note 1		30	50	ns
Passive Gate Pull-Down Resistance			20		kΩ
PH Bias Current	Measure with PWM=Tri-state, PH=1V		-2	-10	µA
VDD Under Voltage Lockout Comparator (V_{UVLO})					
Start Threshold		5.65	6.0	6.3	V
Stop Threshold		5.4	5.7	6.1	V
Hysteresis	Start – Stop			0.4	V
PWM Input					
UGATE Threshold Voltage, $V_{UGATE\ TH}$	PWM rising	2.0	2.2	2.4	V
UGATE Threshold Voltage, $V_{UGATE\ TH}$	PWM falling	1.9	2.1	2.3	V
UGATE Threshold Hysteresis		30	90	170	mV
LGATE Threshold Voltage, $V_{LGATE\ TH}$	PWM falling	0.6	0.8	1.0	V
LGATE Threshold Voltage, $V_{LGATE\ TH}$	PWM rising	0.74	0.9	1.1	V
LGATE Threshold Hysteresis		30	90	170	mV
Tri-State Bias voltage, $V_{PWM\ TRI}$		1.2	1.6	1.8	V
Input Bias Current	V(PWM) = 0V	-260	-210	-160	µA
	V(PWM) = 3.3V	140	200	270	µA
	V(PWM) = 5V	370	460	570	µA
Tri-State Time Constant	C_{PWM} = 20pF, Measure time from V(PWM) = 0V release to LGATE < 1V. Note 1		190		ns
	C_{PWM} = 20pF, Measure time from V(PWM) = 3.3V release to HGATE < 1V. Note 1		270		ns
	C_{PWM} = 20pF, Measure time from V(PWM) = 5V release to HGATE < 1V. Note 1		380		ns

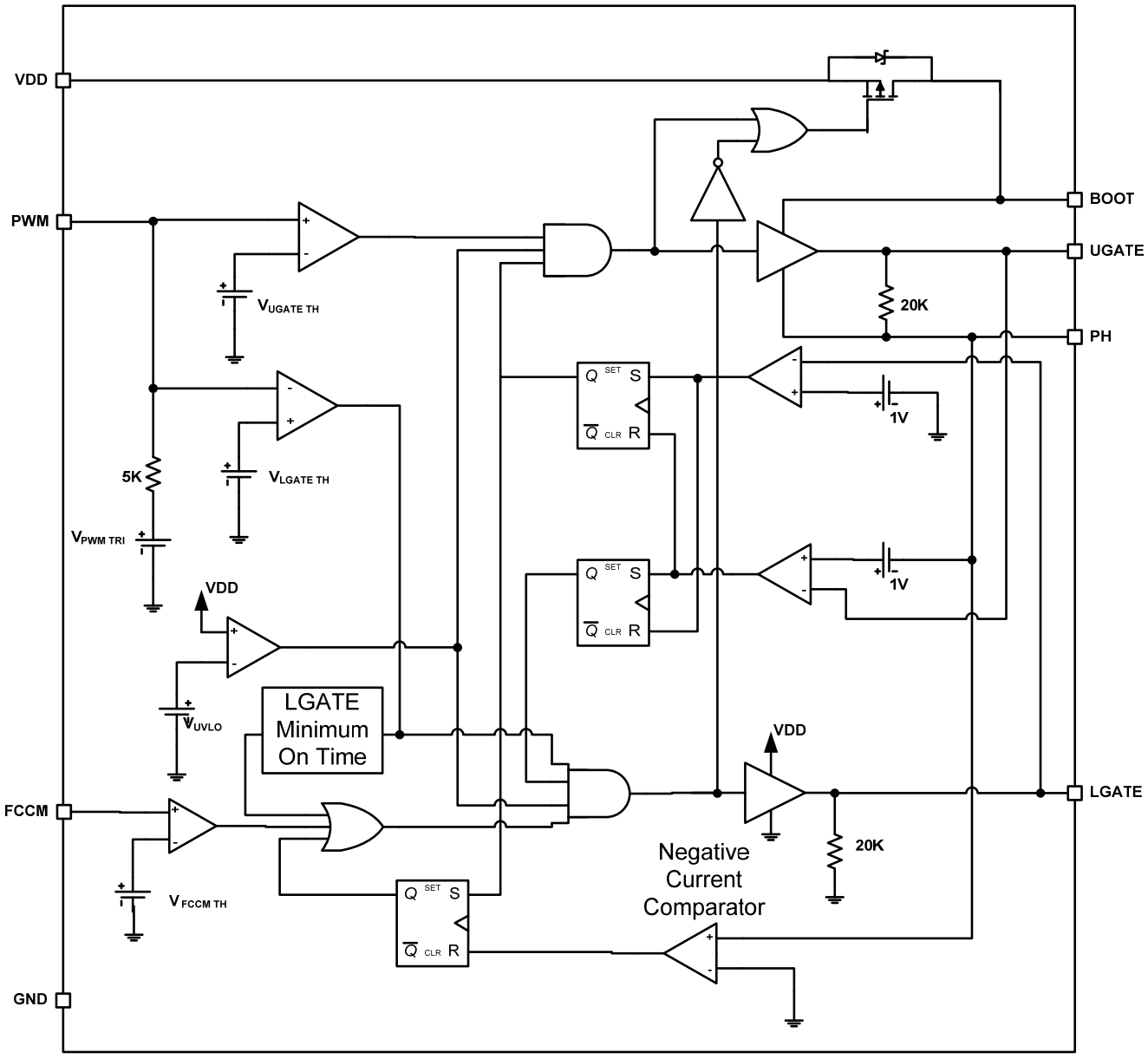
PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
EN/UV Input/Output					
Threshold Voltage, $V_{EN\ TH}$	EN/UV rising, UV FET off	1.1	1.75	2.0	V
	EN/UV falling, UV FET off	0.6	1.1	1.4	V
Hysteresis		350	650	800	mV
Pull-down Resistance		600	1000	1400	Ω
Sink Current	VDD = 2.5V, V(EN/UV) = 0.6V	200	350	500	µA
Bootstrap PFET					
Forward Voltage	I(BOOT) = 30mA, VDD = 7V	450	660	750	mV
General					
VDD Supply Current	EN = 0, PWM = Tri-State		50	100	uA
VDD Supply Current	EN = 3.3 V, PWM = Tri-State		700	1000	uA

Note 1: Guaranteed by design, but not tested in production

IC PIN ORDER AND DESCRIPTION

NAME	NUMBER	I/O LEVEL	DESCRIPTION
UGATE	1	VIN + VDD	High-side driver output and input to GATEL non-overlap comparator
BOOT	2	VIN +VDD	Bootstrapped gate drive supply – connect a capacitor to PHASE
PWM	3	Up to 5V	Logic input
GND	4	Reference IC	Power return – connect to source of synchronous MOSFET
LGATE	5	VDD	Lower gate drive for synchronous MOSFET
VDD	6	Typical 7V	IC bias supply
EN/UV	7	3.3V	Bias this pin to > 2V to enable and < 0.6V to disable the IC (both gate outputs held low). If VDD is below the under voltage lockout threshold this pin is internally pulled low and provides an input Power Good indicator function. If the Power Good and Enable functions are not required this pin can be connected to the VDD pin. Do not float this pin as incorrect operation could occur.
PH	8	VIN	Return for high-side driver, reference for GATEL non-overlap comparator, and input to the diode emulation comparator.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

IR3519 switches the LGATE and UGATE signals when VDD is greater than V_{UVLO} and EN/UV voltage is greater than $V_{EN\ TH}$.

The gate drive logic features adaptive dead time which prevents simultaneous conduction of the upper and lower MOSFETs. The lower gate voltage must be below approximately 1V after PWM goes HIGH and before the upper MOSFET can be gated on. Also the upper gate voltage, the different voltage between UGATE and PH, must be below approximately 1V after PWM goes LOW and before the lower MOSFET can be gated on.

The internal logic will evaluate the PWM voltage level. The PWM is considered HIGH when its level is greater than $V_{UGATE\ TH}$. PWM is considered LOW when its level is below $V_{LGATE\ TH}$. In the middle voltage region of $V_{UGATE\ TH}$ and $V_{LGATE\ TH}$, the PWM will be in tri-state mode. In the absence of external drive, the PWM pin is pulled to this middle region by a $V_{PWM\ TRI}$ source through an internal resistor. After a short time delay in this middle region, IR3519 is forced into a low power state.

The UGATE logic evaluates its input logic signal and generates a PH referenced to drive the UGATE pin, which turns on/off the external high side MOSFET. PH pin is to be connected to the source of the upper MOSFET, the buck inductor, and to the drain of the lower MOSFET. To turn on the upper N channel MOSFET, a bootstrap circuit is required. This is accomplished by charging a capacitor (connected BOOT to PH) after the lower MOSFET conducts and the PH pin is substantially at GND. VDD provides the charging current through an internal BOOTSTRAP diode. The minimum boot capacitor value is calculated below.

The boot capacitor starts the cycle fully charged to a voltage of $V_B(0)$. An equivalent gate drive capacitance is calculated by consulting the high side MOSFET data sheet and taking the ratio of total gate charge at the VDD voltage, $Q_G(VDD)$, to the VDD voltage. $Q_G(VDD)/VDD$ is the equivalent gate drive capacitance C_g which will be used in the following calculations. The voltage of the capacitor pair C_B and C_g after C_g becomes charged at C_B's expense will be $V_B(0)-\Delta V$. Choose a sufficiently small ΔV such that $V_B(0)-\Delta V$ exceeds the maximum gate threshold voltage to turn on the high side MOSFET. Since total charge Q_T is conserved, we can write the following equation.

$$V_B(0)\cdot C_B = Q_T = V(t_{on})\cdot(C_B + C_g)$$

After rearranging this equation, it becomes the equation below.

$$C_B = C_g \cdot \left(\frac{V_B(0)}{\Delta V} - 1\right)$$

Choose a boot capacitor value larger than the calculated C_B. The voltage rating of this part needs to be larger than $V_B(0)$ plus the desired derating voltage. Its ESR and ESL needs to be low in order to allow it to deliver the large current and di/dt's which drive MOSFETs most efficiently. In support of these requirements a ceramic capacitor should be chosen.

The LGATE logic evaluates its input signal and generates a GND referenced to drive the LGATE pin, which turns on/off the external low side MOSFET. The LGATE logic uses VDD source to turn on the low side MOSFET because the source of low side MOSFET is reference to GND.

LAYOUT RECOMMENDATION

One 1uF high quality ceramic capacitor is required to place near VDD pin as possible. Other end of capacitor is recommended to tie to GND pin plan as close to as IC possible. This GND island plan can be via or directly connect to the main GND plan or layer. If the connection of GND pin to the source of low side MOSFET through an internal layer, it is recommended connecting through at least 2 vias by build a small island of next to GND pin. The boot capacitor needs to place close to BOOT and PH pins to reduce the impedance during the turn-on process of high side MOSFET. The main function of boot capacitor is to supply the energy for turning on high side MOSFET. It is recommended to add zero Ohm resistor in series with boot capacitor as place holder. When connecting the trace for UGATE and LGATE signals, one needs to keep in mind that the signal return path is as an important as signal path. The return path contains both AC and DC current. DC current takes the least resistance path. AC current takes the least impedance path. The return path is exits whether or not provide it. If the designer is overlooked the return path, the AC current will cause the more noise in the system. Therefore, it is recommended to place LGATE signal path on top next to the source of low side MOSFET path and place UGATE signal path on top of PH signal path. When connecting PHASE signal path to power stage area, PHASE signal needs to chose quite area. Figure 1 shows the location of connection from power stage to IR3519 PHASE pin less noise sensitive than Figure 2.

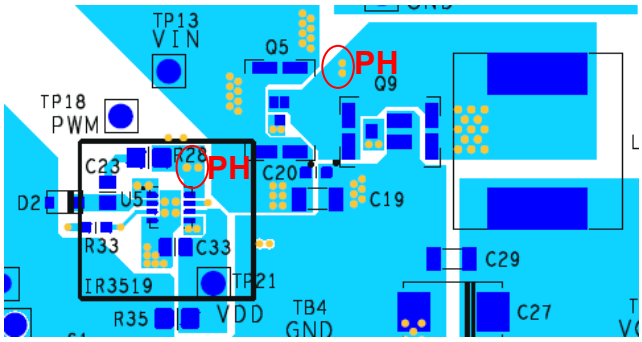


Figure 1: Phase Node Sense with Less Noise

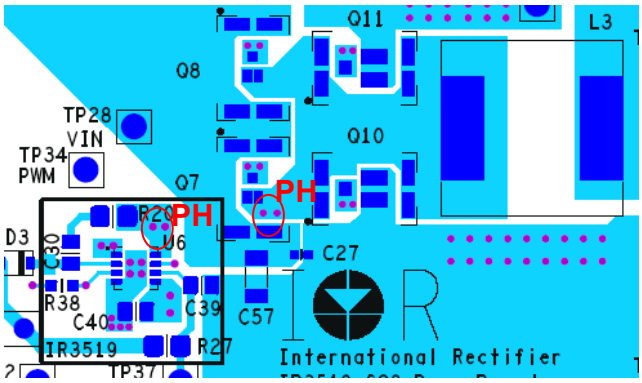
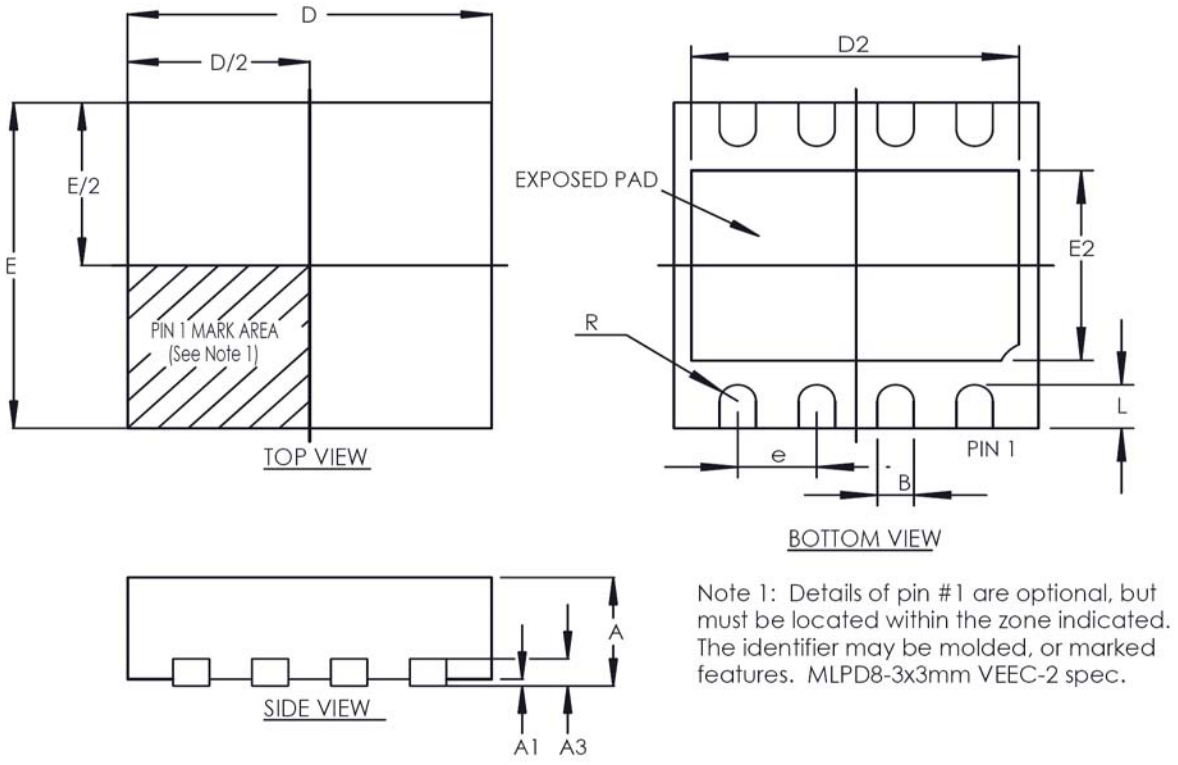


Figure 2: Phase Node Sense with More Noise

PACKAGE INFORMATION

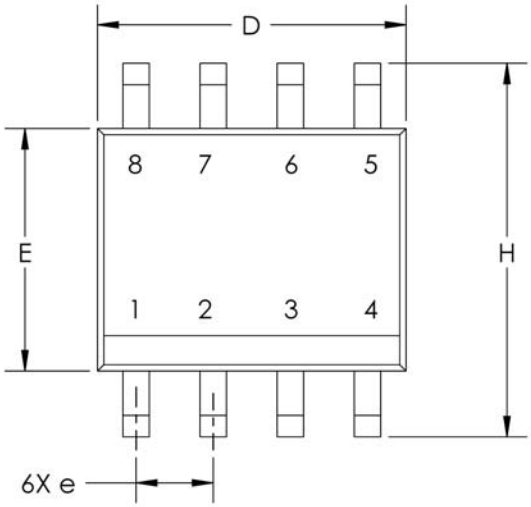
3 X 3MM MLPD



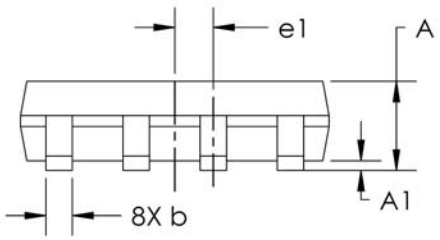
Note 1: Details of pin #1 are optional, but must be located within the zone indicated. The identifier may be molded, or marked features. MLPD8-3x3mm VEEC-2 spec.

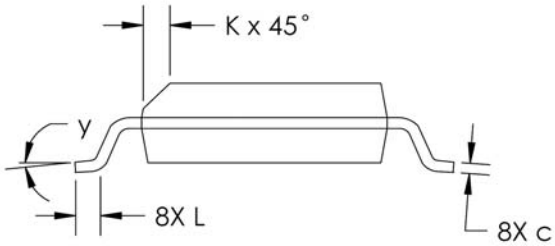
SYMBOL	8-PIN 3x3 (unit: MM)		
DESIGN	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20 REF	
B	0.25	0.30	0.35
D		3.00 BSC	
D2	1.6	--	2.50
E		3.00 BSC	
E2	1.35	--	1.75
e		0.65 PITCH	
L	0.30	0.40	0.50

8L SON



DIM	Inches		Milimeters	
	MIN	MAX	MIN	MAX
A	0.0532	0.0688	1.35	1.75
A1	0.0040	0.0098	0.10	0.25
b	0.013	0.020	0.33	0.51
c	0.0075	0.0098	0.19	0.25
D	0.189	0.1968	4.80	5.00
E	0.1497	0.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	0.2284	0.2440	5.80	6.20
K	0.0099	0.0196	0.25	0.50
L	0.016	0.050	0.40	1.27
y	0°	8°	0°	8°





Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

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