20-25GHz Low Noise Amplifier

GaAs Monolithic Microwave IC in SMD package

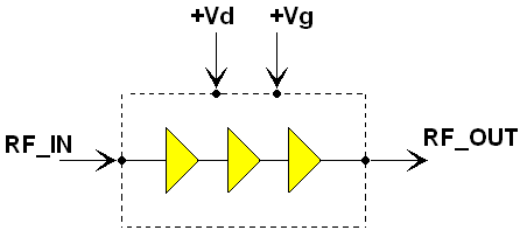
Description

The CHA2411-QDG is a K band low noise amplifier providing 26 dB gain from a single bias supply +5V with a noise figure of 2.5 dB. All the active devices are self biased on chip.

The circuit is manufactured with a pHEMT process 0.25µm.

It is available in lead-free SMD package.

Functional diagram



Main Features

- 20-25GHz Bandwidth
- Excellent 2.5dB Noise Figure
- 26 dB ± 2dB stable Gain vs Ttemperature
- +5V single Supply
- 24L-QFN 4x4 SMD leadless package

Main Characteristics

Tamb = +25°C

Parameters	Min	Typ	Max	Unit
Frequency range	20		25	GHz
Small signal Gain	22	26	30	dB
SSB Noise figure		2.5		dB
Input / Output Return Loss		15		dB

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

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Electrical Characteristics

Full temperature range

Symbol Pins	Parameters	Min	Typ	Max	Unit
Fop	Operating frequency range	20		25	GHz
G	Small signal Gain	22	26	30	dB
ΔG(Fop)	Gain variation @ frequency range		± 0.5		dB
ΔG(T)	Gain variation @ temperature range		± 2		dB
NF	SSB Noise figure		2.5		dB
S11 S22	Input / Output Return		-10		dB
P.1dB In	Input Power at 1 dB Gain Compression @24GHz		-14		dBm
IP3 In	Input IP3 @24GHz		-7.5		dBm
Pout_sat	Saturated Output Power @24GHz		13.5	15	dBm
+Vd, +Vg	Supply Voltage		5		V
+I	Supply Current		43	55	mA
Top	Operating temperature range	-40	25	100	℃

Remark

These performance has been obtained with the chip in QFN package mounted on the recommended boards (ref. 95541 & 95581) described in the document. These performances are highly dependent on this environment.

Absolute Maximum Ratings (1)

Symbol	Parameters	Values	Unit
+Vg, +Vd	Maximum positive supply voltage	6	V
+I	Maximum positive supply voltage	65	mA
Pin	Maximum peak input power overdrive	-5	dBm
Top	Operating temperature range	-40 to +100	℃
Tstg	Storage temperature range	-55 to +125	℃

(1) Operation of this device above anyone of these parameters may cause permanent damage.
Duration < 1s

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Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered).
The temperature is monitored at the package back-side interface (Tcase) as shown below.
The system maximum temperature must be adjusted in order to guarantee that Tcase remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

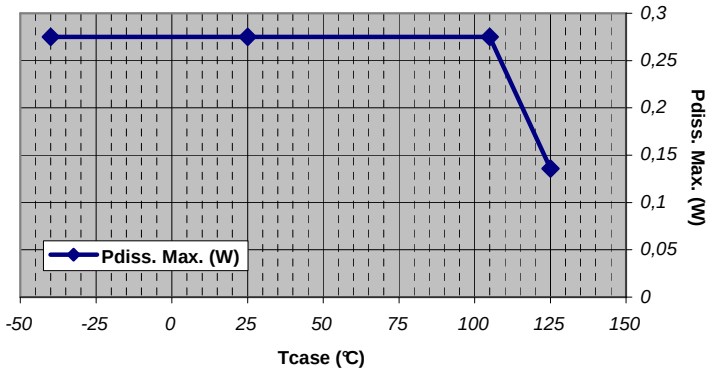
A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below than the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

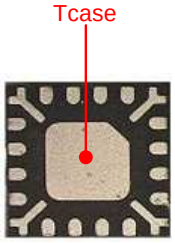
DEVICE THERMAL SPECIFICATION : CHA2411-QDG			
Recommanded max. junction temperature (Tj max)		:	145 °C
Junction temperature absolute maximum rating		:	175 °C
Max. continuous dissipated power @ Tcase=	105 °C	:	0,27 5 W
=> Pdiss derating above Tcase(1)=	105 °C	:	7 mW/°C
Junction-Case thermal resistance (Rth J-C)(2)		:	<143 °C/W
Min. package back side operating temperature(3)		:	-40 °C
Max. package back side operating temperature(3)		:	105 °C
Min. storage temperature		:	-55 °C
Max. storage temperature		:	125 °C

(1) Derating at junction temperature constant = Tj max

*(2) Rth J-C is calculated for a worst case where the **hotter junction** of the MMIC is considered.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example of QFN 16L 3x3 back-side view, temperature reference point (Tcase) location.

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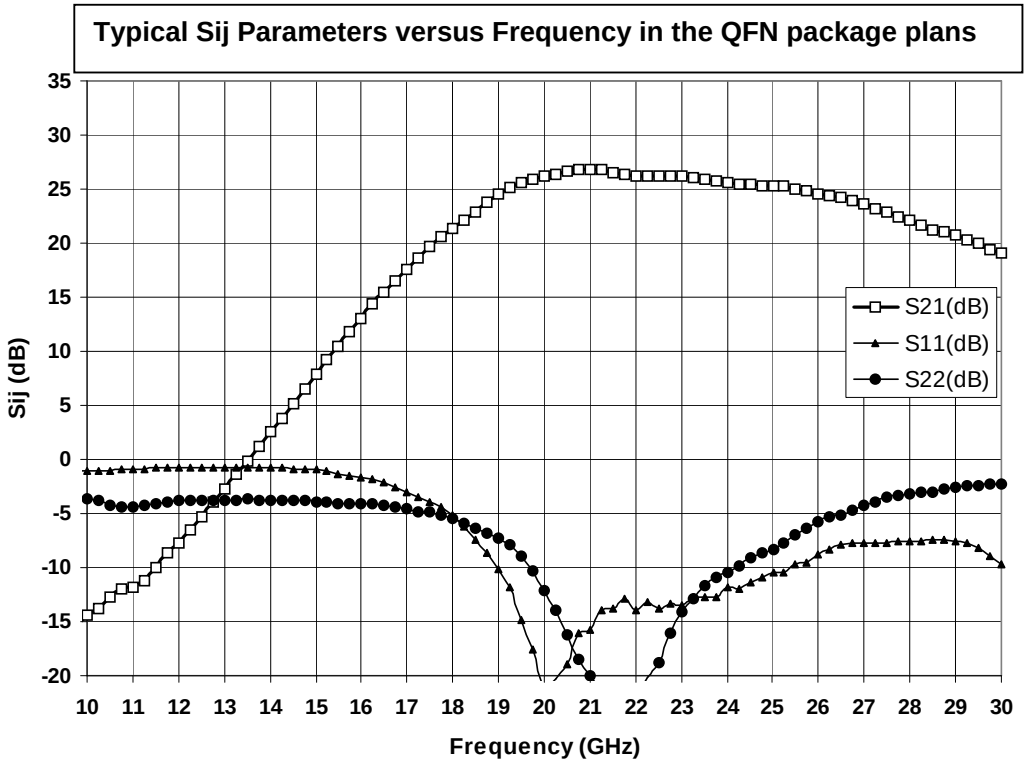
Typical QFN measurements on board 95581 (QFN plan)



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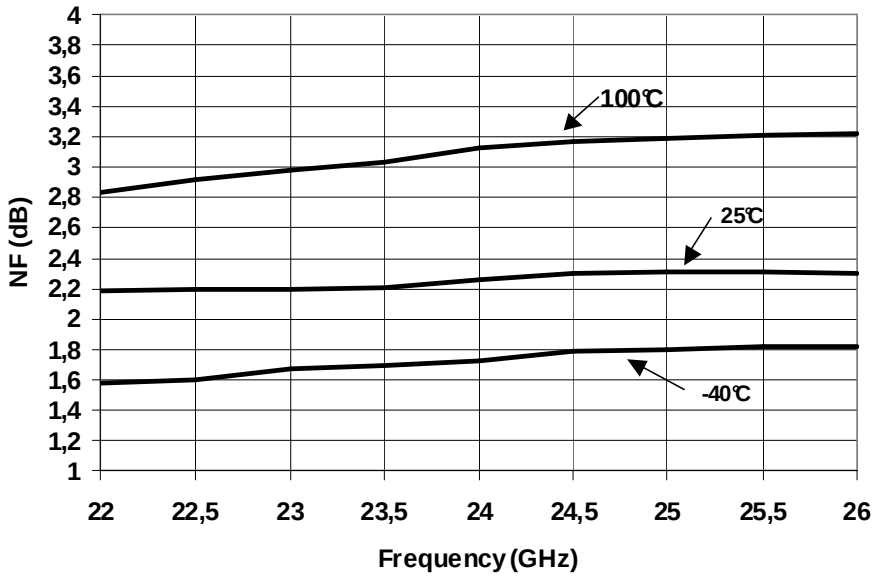
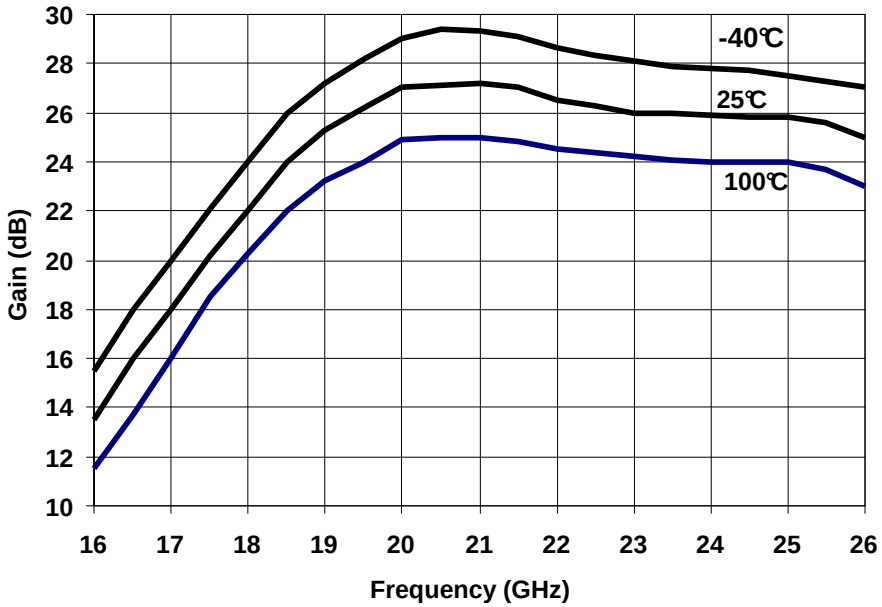
Typical QFN measurements on board 95541 (QFN plan)

Vs = versus

Noise Figure versus Frequency



Gain versus Frequency



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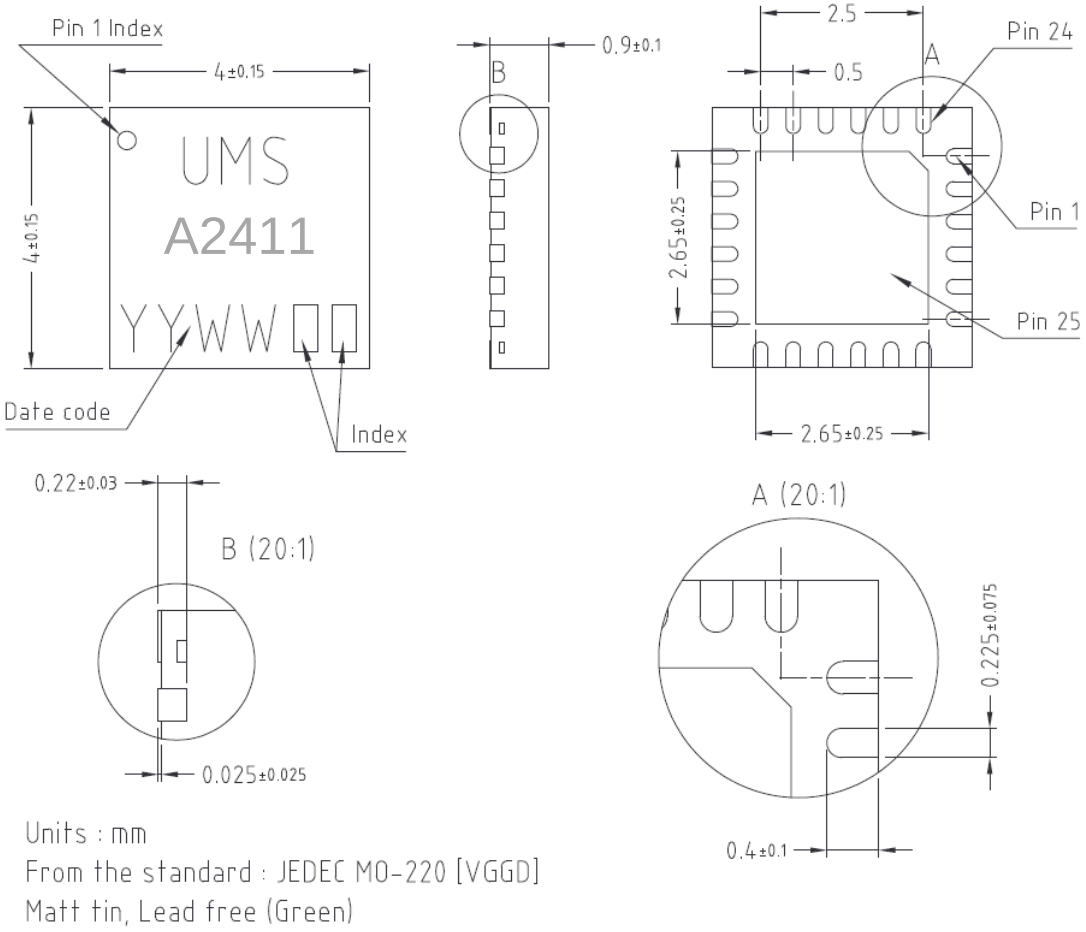
QFN Outline (1)



(1)The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 available at http://www.ums-gaas.com for exact package dimensions.

Pin-out description

Pin number	Pin name	Symbol Name	Description
4	RFIn	RF_IN	Control Voltage port
15	RFOut	RF_OUT	RF1 Input/Output ports
22	VD	+Vd	Positive Drain supply voltage
9	VG	+Vg	Positive Gate supply voltage
3, 5, 14, 16, 25	GND	GND	Ground
1, 2, 6, 7, 8, 10, 11, 12, 13, 17, 18, 19, 20, 21, 23, 24	Nc	Nc	Not connected

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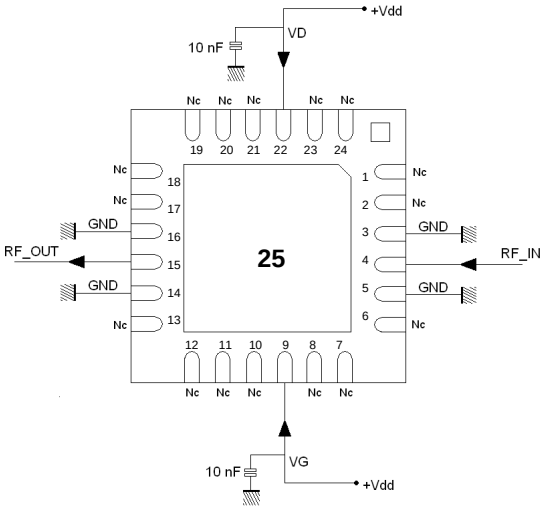
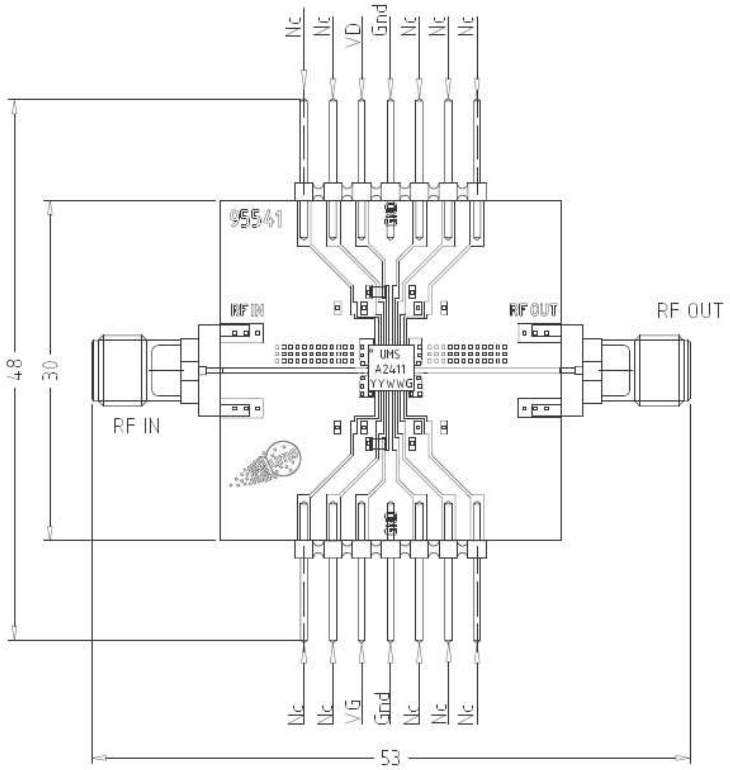
External Components and bias configuration (recommended)



Recommended Test Fixture (Ref. 95541) for measurements over Temperature Range (Unit=mm)



Rep	P/N	Qt	DESIGNATION	REF FABRICANT	FABRICANT
	61495564	1	Monture 30X30 EDG	SEMELLE	(Sous traitance mecanique)
	61495541	1	Demonstrateur Board 24L QFN4X4	CIRCUIT 95541	(Sous traitance Circuit Imprimé)
	47000774	2	Connecteur SMA (DC-28GHz)	PSF-S03-000-01	GIGALANE
	61495570	2	Adaptateur connecteur PSF-S03-000-01	FOURCHE	
		4	Vis CL M2.5X3		
		2	Condo 0603 X7R 10nF ±10% 50V	GRM1888R71H103K	MURATA
		2	Barette male 7x2 Contacts pl. 61497366	47303418040 0	Kontek COMATEL
		1	CHA2411QDG		

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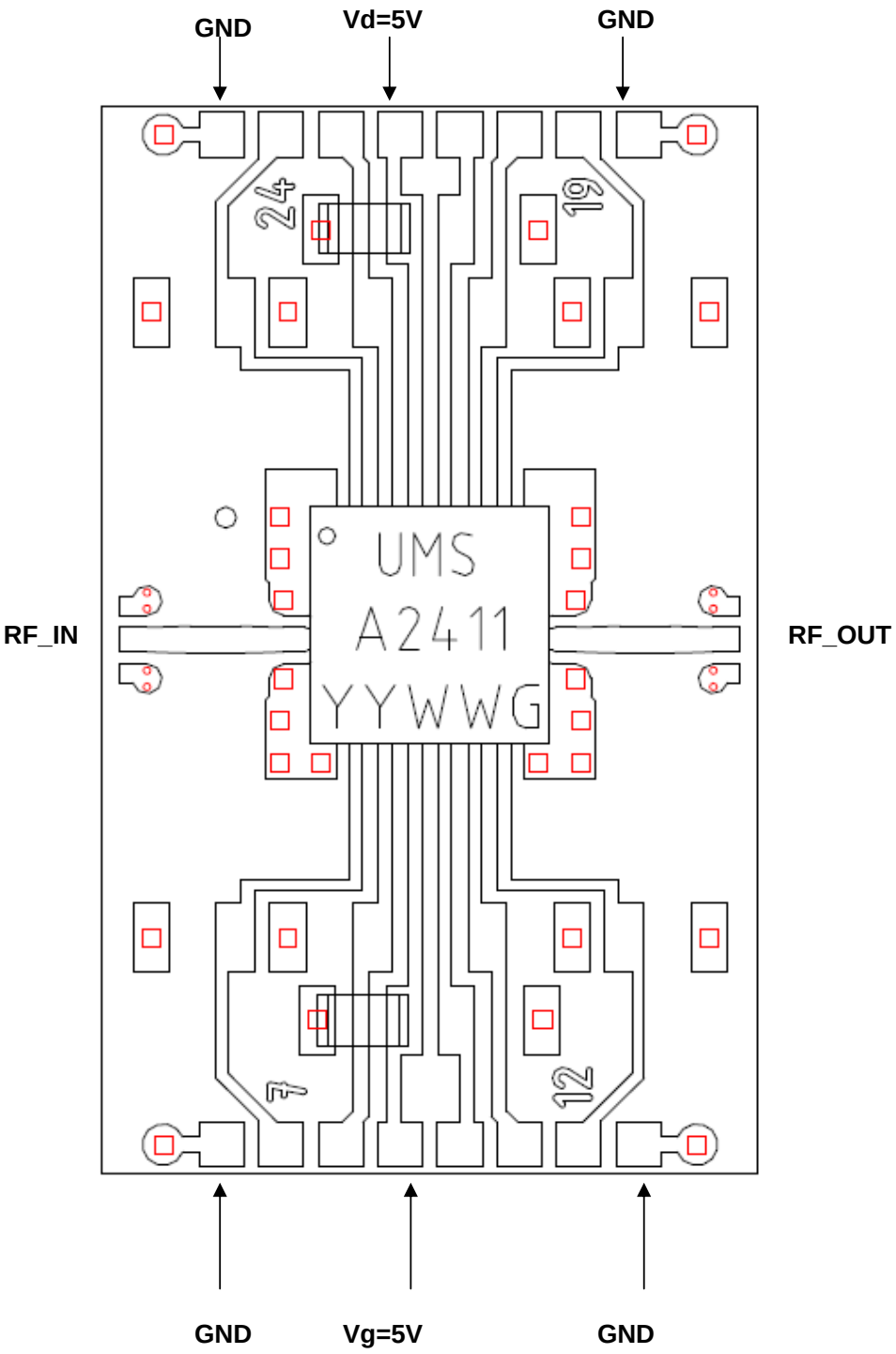
Recommended Test Fixture (Ref. 95581) for measurements in the package's plans with probes



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ESD sensitivity

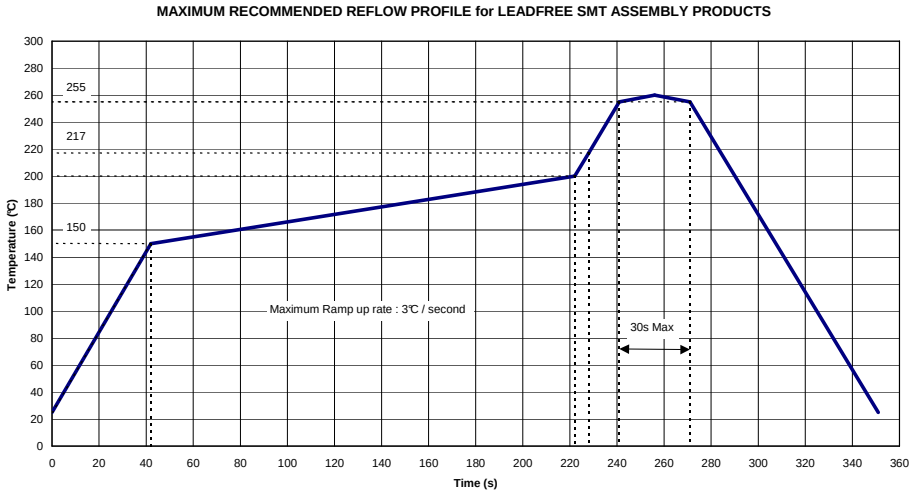
Standard	Value
MIL-STD-1686C	HBM Class 1 (<0V - 1999V)
ESD STM5.1-2001	HBM Class 0 (<250V)

Package Information

Parameter	
Package body material	RoHS-compliant Low stress Injection Molded Plastic
Lead finish	100% matte Sn
MSL Rating	MSL1

Recommended surface mount package assembly(see UMS AN0017)

For volume production the SMD type package can be treated as a standard surface mount component (please refer to the IPC/JEDEC J-STD-020C standard or equivalent). The assembly on the motherboard can be performed using a standard assembly process (e.g. stencil solder printing, standard pick-and-place machinery, and solder reflow oven). However, caution should be taken to perform a good and reliable contact over the whole pad area.



Caution

The solder thickness after reflow should be typical 50µm [2 mils] and the lateral alignment between the package and the motherboard should be within 50µm [2 mils].
It is important for the performance of the product that the whole overlapping area between the motherboard and package pads is connected. Voids or other improper connections, in particular, between the ground pads on motherboard and package will lead to a deterioration of the RF performance and the heat dissipation. The latter effect can reduce drastically reliability and lifetime of the product.

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Ordering Information

24L-QFN4x4 Lead Free Package: CHA2411-QDG/XY

Stick: XY=20 Tape and reel: XY=21

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