AS1112

DataSheet

16-Channel LED Driver with Dot Correction and Greyscale PWM

1 General Description

The AS1112 is a 16-channel, constant current-sink LED driver. Each of the 16 channels can be individually adjusted by 4096-step greyscale PWM brightness control and 64-step constant-current sink (dot correction).

The dot correction circuitry adjusts the brightness variations between the AS1112 channels and other LED drivers. Greyscale control and dot correction circuitry are accessible via the SPI-compatible serial interface. A single external resistor sets the maximum current value of all 16 channels.

The open & short LED detection function indicates a broken, shorted or disconnected LED at one or more of the outputs. The overtemperature flag indicates that the device is in an overtemperature condition.

Table 1. Standard Products

Model	Power-Down	TEST pin
AS1112	Yes	Connect to GND
AS1112B	No	Connect to VCC

An additional power-down pin puts the AS1112 into a 40nA standby-mode.

The AS1112 is available in a 32-pin TQFN 5x5 mm package.

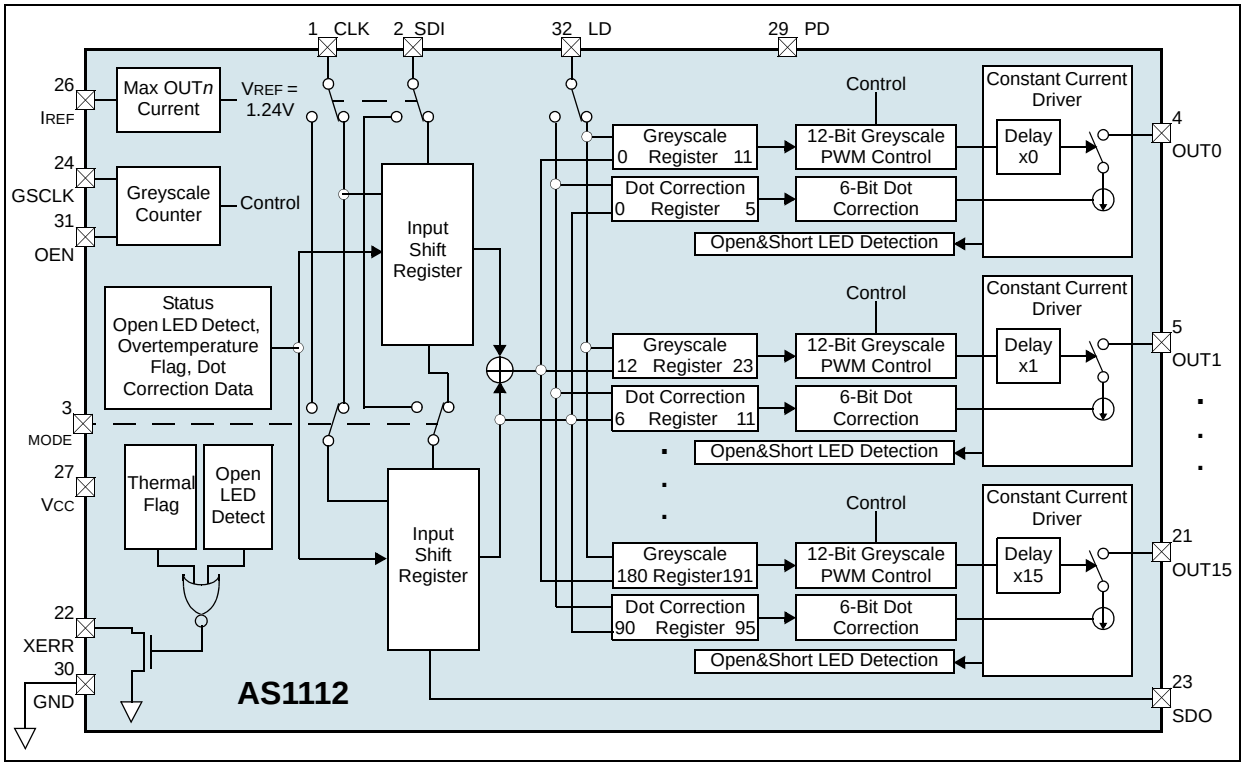
2 Key Features

- 16 Channels
- Greyscale PWM Control: 12-Bit (4096 Steps)
- Dot Correction: 6-Bit (64 Steps)
- Drive Capability (Constant-Current Sink): 0 to 80mA
- LED Power Supply Voltage: Up to 15V
- Supply Voltage Range: 3.0 to 5.5 V
- SPI-Compatible Serial Interface
- Controlled In-Rush Current
- Data Transfer & PWM Clock Rate: up to 30 MHz
- CMOS Level I/O
- Diagnostic Features
  - LED Open/Short Detection
  - Overtemperature Flag
- 32-pin TQFN 5x5 mm Package

3 Applications

The device is ideal for mono-, multi-, and full-color LED displays, LED signboards, and display backlights.

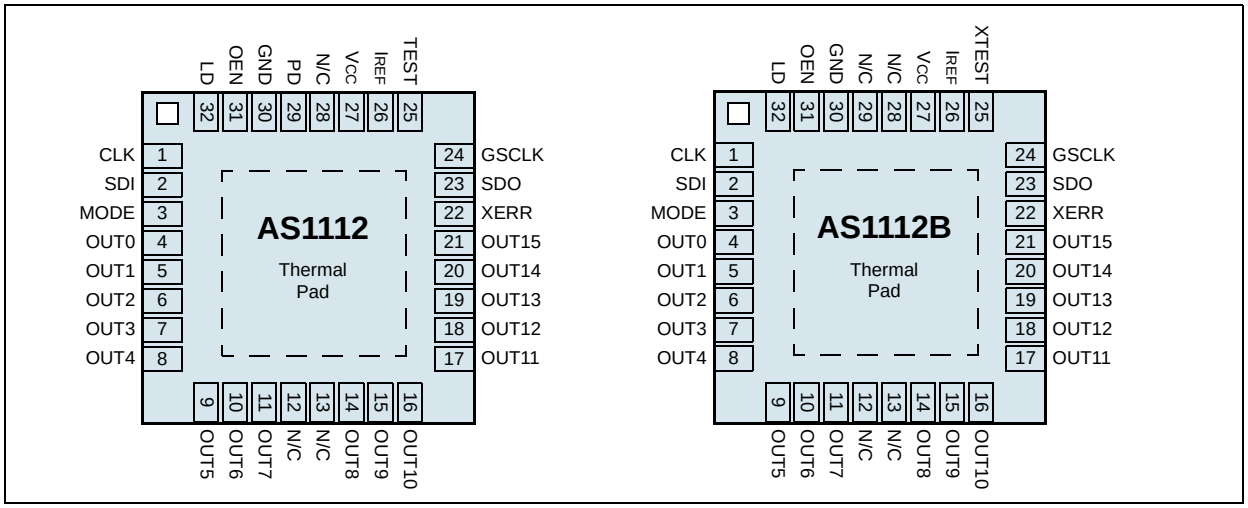
Figure 1. Block Diagram



4 Pinout

Pin Assignments

Figure 2. Pin Assignments (Top View)



Pin Descriptions

Table 2. Pin Descriptions

Pin Number	Pin Name	Description
1	CLK	**Serial Data Shift Clock**
2	SDI	**Serial Data Input**
3	MODE	**Mode Select** input with internal pulldown MODE = GND: Selects greyscale mode (see Setting Greyscale Brightness on page 12). MODE = VCC: Selects dot correction mode (see Setting Dot Correction on page 11).
4:11	OUT0:OUT7	**Constant-Current Outputs 0:7**
14:21	OUT8:OUT15	**Constant-Current Outputs 8:15**
22	XERR	**Error Output** 0 = LED open detection or overtemperature condition is detected. 1 = Normal operation.
23	SDO	**Serial Data Output**
24	GSCLK	**Greyscale Clock**. Reference clock for greyscale PWM control
25	TEST	**Test Pin** This pin must be connected to GND (AS1112) to ensure normal operation.
	XTEST	**Test Pin** This pin must be connected to VCC (AS1112B) to ensure normal operation.
26	IREF	**Reference Current Terminal**
27	VCC	**Power Supply Voltage**
12,13,28	N/C	This pin must not be connected.
29	PD	**Power Down** input with internal pulldown (AS1112) 0 = normal operation mode 1 = powerdown mode
	N/C	**Not Connected** (AS1112B)
30	GND	**Ground**
31	OEN	**Blank Outputs** 0 = OUT*n* outputs are controlled by the greyscale PWM control. 1 = OUT*n* outputs are forced off; the greyscale counter is reset.
32	LD	**Data Latch**. The internal connections are switched by pin MODE. For LD (MODE = GND), the greyscale register receives new data. For LD (MODE = VCC), the dot correction register receives new data.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 3 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Recommended Operating Conditions on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Input Voltage Range to GND	0.3	6	V	
Output Current (DC)		90	mA	
Input Voltage Range	-0.3	V_{CC} + 0.3	V	
Output Voltage Range V_{SDO}, V_{XERR} to GND	-0.3	V_{CC} + 0.3	V	
Output Voltage Range V_{OUT0}: V_{OUT15} to GND	-0.3	15	V	
ESD Rating		2	kV	*JEDEC 22-A114 Human Body Model*
Storage Temperature Range	-55	+150	ºC	
Operating Ambient Temperature Range	-40	+85	ºC	
32-pin TQFN 5x5 mm Package Thermal Impedance		23	ºC/W	on 4-Layer PCB
Package Body Temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).

6 Recommended Operating Conditions

Table 4. DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage		3		5.5	V
V_{OUT}	Voltage Applied to Output (OUT0:OUT15)				15	V
V_{IH}	High-Level Input Voltage		0.8 x V_{CC}		V_{CC}	V
V_{IL}	Low-Level Input Voltage		GND		0.2 x V_{CC}	V
I_{OH}	High-Level Output Current	V_{CC} = 5 V at SDO			-1	mA
I_{OL}	Low-Level Output Current	V_{CC} = 5 V at SDO, XERR			1	mA
I_{COC}	Constant Output Current	OUT0:OUT15			80	mA

Table 5. AC Characteristics – V_{CC} = 3 V to 5.5 V, T_{AMB} = -40 to 85°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CLK}	Data Shift Clock Frequency	CLK			30	MHz
f_{GSCLK}	Greyscale Clock Frequency	GSCLK			30	MHz
t_{WH0}/t_{WL0}	CLK Pulse Duration	CLK = 1/0 [1]	16			ns
t_{WH1}/t_{WL1}	GSCLK Pulse Duration	GSCLK = 1/0 [2]	16			ns
t_{WH2}	LD Pulse Duration	LD = 1 [1]	20			ns
t_{WH3}	OEN Pulse Duration	OEN = 1 [2]	20			ns
t_{SU0}	Setup Time	SDI, CLK [3]	12			ns
t_{SU1}		CLK, LD [3]	12			
t_{SU2}		MODE, CLK [4]	12			
t_{SU3}		MODE, LD [4]	12			
t_{SU4}		OEN, GSCLK [2]	12			
t_{H0}	Hold Time	CLK, SDI [3]	12			ns
t_{H1}		LD, CLK [1]	12			
t_{H2}		CLK, MODE [4]	12			
t_{H3}		LD, MODE [4]	12			
t_{H4}		OEN, GSCLK [2]	12			

1. See Figure 10 on page 12.
2. See Figure 14 on page 14.
3. See Figure 12 on page 13.
4. See Figure 7 on page 8.

7 Electrical Characteristics

V_{CC} = +3.0 to +5.5V, T_{AMB} = -40 to +85ºC. Typical values are at T_{AMB} = 25°C, V_{CC} = 5V (unless otherwise specified).

Table 6. Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OH}	High-Level Output Voltage	I_{OH} = -1mA, SDO	V_{CC} - 0.5			V
V_{OL}	Low-Level Output Voltage	I_{OL} = 1mA, SDO, XERR			0.5	V
I	Input Current	V_{IN} = V_{CC} or GND; Pins OEN, TEST, GSCLK, CLK, SDI, LD	-1		1	µA
		V_{IN} = V_{CC}; pin MODE, PD			100	
		V_{IN} = GND; pin MODE, PD	-1		1	
I_{CC}	Supply Current	All outputs off, R_{IREF} = 10kΩ		1.2	3	mA
		All outputs off, R_{IREF} = 1.3kΩ		4	10	
		All outputs on, R_{IREF} = 1.3kΩ		15	20	
		All outputs on, R_{IREF} = 640Ω		30	40	
I_{PD}	Power Down Current			40		nA
I_{COC}	Constant Output Current	All outputs on, V_{OUT} = 2V, R_{IREF} = 640Ω	54	61	69	mA
I_{LEAK}	Leakage Output Current	All outputs off, V_{OUT} = 15V, R_{IREF} = 640Ω, OUT0:OUT15		20		nA
ΔICOC	Constant Current Error	V_{OUT} = 2V, R_{IREF} = 640Ω, OUT0:OUT15		±3	±4.5	%
		V_{OUT} = 2V, R_{IREF} = 480Ω, OUT0:OUT15		±3	±4.5	
		Device to device, average current from OUT0:OUT15, R_{IREF} = 1920Ω (20 mA)		±3	±4.5	
		Device to device, average current from OUT0:OUT15, R_{IREF} = 480Ω (80 mA)		±3	±4.5	
ΔILNR	Line Regulation	V_{OUT} = 2V, R_{IREF} = 640Ω OUT0:OUT15		±1	±2.5	%/V
		V_{OUT} = 2V, R_{IREF} = 480Ω OUT0:OUT15		±1	±2.5	
ΔILDR	Load Regulation	V_{OUT} = 2 to 4V, R_{IREF} = 640Ω, OUT0:OUT15		±0.1	±0.5	%/V
		V_{OUT} = 2 to 4V, R_{IREF} = 480Ω, OUT0:OUT15		±0.1	±0.5	
T_{TEF}	Thermal Error Flag Threshold	Junction temperature [1]		150		ºC
T_{TWF}	Thermal Warn Flag Threshold	Junction temperature [1]		125		ºC
V_{LSD}	LED Short Detection Threshold	V_{CC} = 5V		3.6		V
V_{LOD}	LED Open Detection Threshold			0.3	0.4	V
V_{IREF}	Reference Voltage Output	R_{IREF} = 640Ω	1.20	1.24	1.28	V

1. Specified by design. Not tested.

Switching Characteristics

V_{CC} = +3.0 to +5.5V, T_{AMB} = -40 to +85ºC. Typical values are at T_{AMB} = 25°C, V_{CC} = 5V (unless otherwise specified).

Table 7. Switching Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{R0}	Rise Time	SDO		8		ns
t_{R1}		OUT*n*, DC = $3F_{HEX}$		20		
t_{F0}	Fall Time	SOUT		8		ns
t_{F1}		OUT*n*, DC = $3F_{HEX}$		20		
t_{PD0}	Propagation Delay Time	CLK, SDO [1]		15		ns
t_{PD1}		OEN, OUT0 [2]		30		
t_{PD2}		OUT*n*, XERR [2] (includes error detection time, see Figure 8 on page 10)		1000		
t_{PD3}		GSCLK, OUT0 [2]		30		
t_D	Average Output Delay Time	OUT*n*, OUT*n*+1 [2]		30		ns

1. See Figure 12 on page 13.
2. See Figure 14 on page 14.

Dissipation Ratings

Table 8. Dissipation Ratings

Package Type	Power Rating (T_{AMB} < 25ºC)	Derating Factor above 25ºC	Power Rating (T_{AMB} = 70ºC)	Power Rating (T_{AMB} = 85ºC)
32-pin TQFN 5x5 mm	5433mW	43.47mW/ºC	3477mW	2825mW

8 Typical Operating Characteristics

V_{DD} = 5V, T_{AMB} = 25ºC.

Figure 3. Output Current vs. V_{DS};

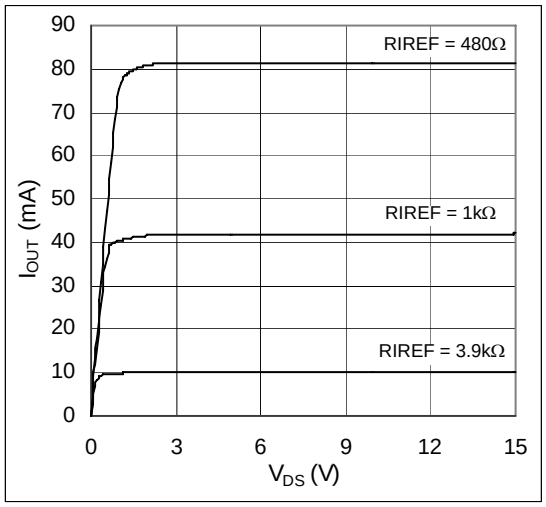


Figure 4. Output Current vs. V_{DS};

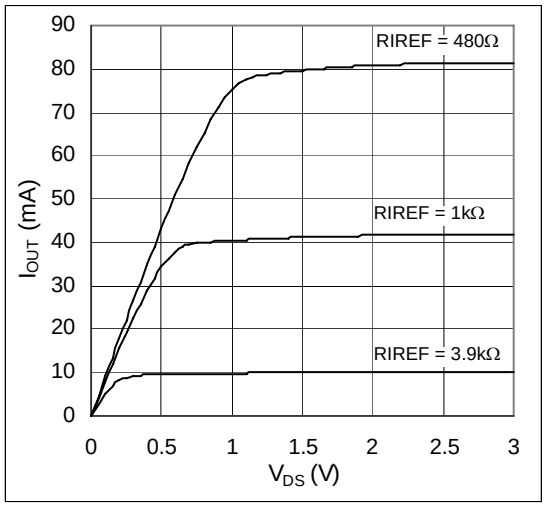


Figure 5. Output Current vs. R_{EXT}

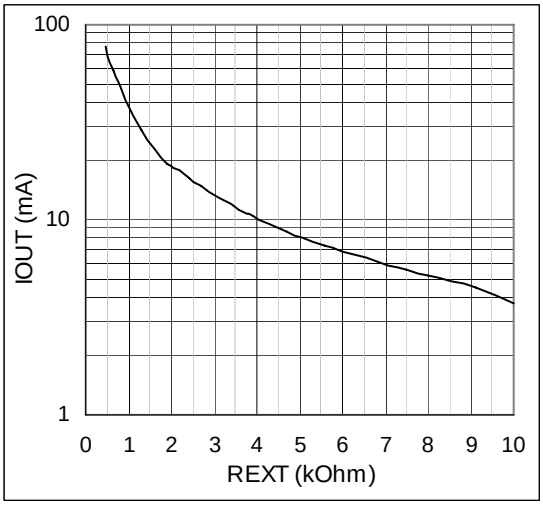
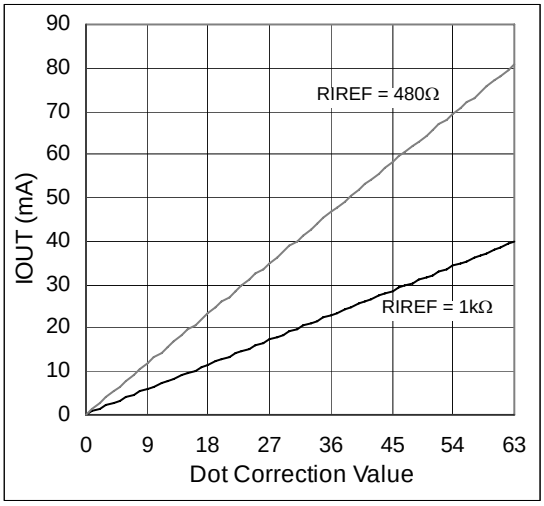


Figure 6. Output Current vs. Dot Correction Value



9 Detailed Description

Serial Interface

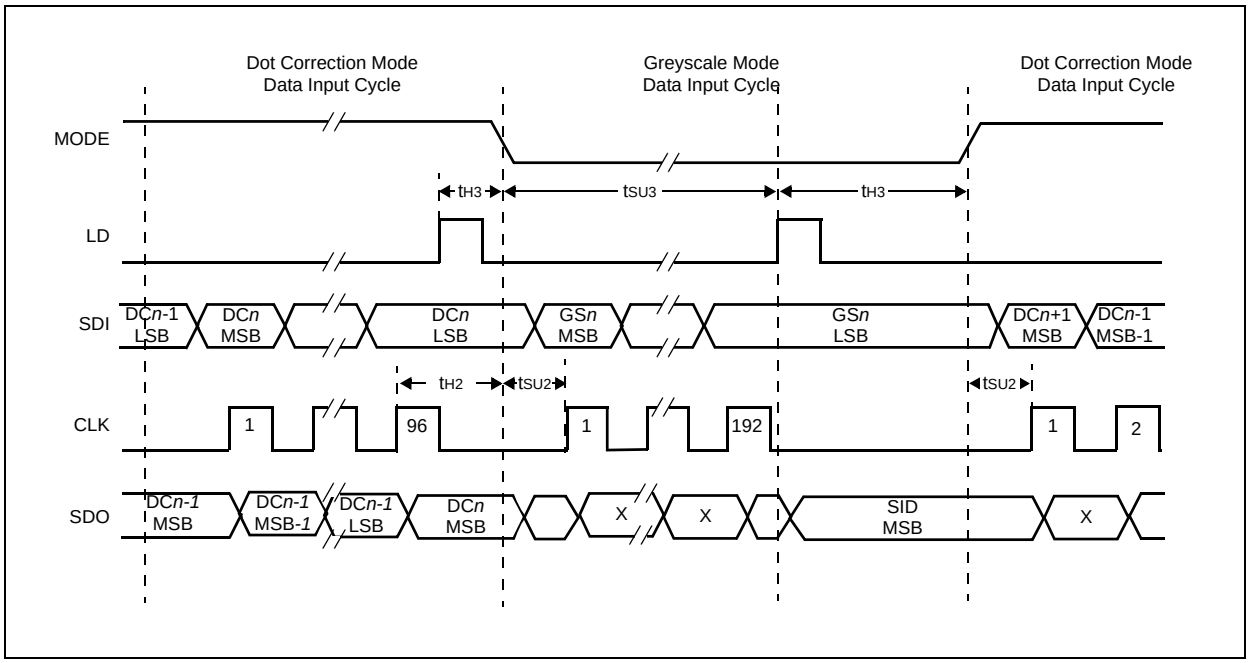
The AS1112 features a versatile 3-pin (CLK, SDI, and SDO) serial interface, which can be connected to microcontrollers or digital signal processors in various configurations.

The rising edge of the CLK signal shifts data from pin SDI to the internal register. After all data is clocked in, the serial data is latched into the internal registers at the rising edge of the LD signal.

Note: All data is clocked in with the MSB first.

Multiple AS1112 devices can be cascaded by connecting the SDO pin of one device with pin SDI of the next device (see Figure 15 on page 15). The SDO pin can also be connected to the microcontroller to receive status information from the AS1112. The serial data format is 96-bit or 192-bit wide, depending on mode of the device (see LD on page 2).

Figure 7. Serial Data Input Timing Diagram



Error Information Output

The open-drain output pin XERR indicates if the device is in one of the two error conditions: overtemperature flag or open LED detect. During normal operation, the internal transistor connected to pin XERR is turned off and the voltage on XERR is pulled up to V_{CC} through an external pullup resistor.

If an overtemperature or open LED condition is detected, the internal transistor is switched on, and XERR is pulled to GND. Because XERR is an open-drain output, multiple AS1112 devices can be ORed together and pulled up to V_{CC} with a single pullup resistor (see Figure 15 on page 15). This reduces the number of signals needed to report a system error.

To differentiate the overtemperature flag from the open LED detect flag from pin XERR, the open LED detect flag can be masked out by setting OEN = 1 (see Table 9).

Table 9. XERR Truth Table

Error Condition			Error Information				Selected Mode			Status
	Temp.	OUT*n* Voltage	Thermal Error Flag	Thermal Warning Flag	Open LED Detect	Short LED Detect	OEN	Mode	XERR	
Open	$T_J < T_{TEF}$	OUT*n* > V_{LOD}	0	Don't Care	0	Don't Care	0	0	1	normal
		OUT*n* < V_{LOD}	0	Don't Care	1	Don't Care	0	0	0	open error
	$T_J > T_{TEF}$	OUT*n* > V_{LOD}	1	Don't Care	0	Don't Care	0	0	0	temp. error
		OUT*n* < V_{LOD}	1	Don't Care	1	Don't Care	0	0	0	open & temp. error
Temp	$T_J > T_{TEF}$	Don't Care	0	Don't Care	Don't Care	Don't Care	1	0	1	normal
	$T_J < T_{TEF}$	Don't Care	1	Don't Care	Don't Care	Don't Care	1	0	0	temp error
	$T_J > T_{TWF}$	Don't Care	Don't Care	0	Don't Care	Don't Care	1	1	1	normal
	$T_J < T_{TWF}$	Don't Care	Don't Care	1	Don't Care	Don't Care	1	1	0	temp. warn

Overtemperature Error/Warning Flags

The AS1112 provides a overtemperature circuit to indicate that the device is in an overtemperature condition. If the device junction temperature (T_J) exceeds the threshold temperature (150°C typ), the overtemperature circuit trips and pulls XERR to ground. The overtemperature flag status can be read out from the AS1112 status register.

To prevent an overtemperature condition the AS1112 offers an temperature warning flag at 125°C typical. This flag can be used to take precautions (e.g. start an external cooling) against a overtemperature condition.

Open LED Detection

The AS1112 integrated open LED detection circuit reports an error if any of the 16 LEDs is open or disconnected from the circuit. The open LED detection circuit trips when the error detection is activated (see Table 9) and the voltage at OUT*n* is less than V_{LOD}.

Note: The voltage at each OUT*n* is sampled 1µs after being switched on. Please refer to Figure 8.

The open LED detection circuit also pulls XERR to GND when tripped. The open LED status of each channel can also be read out from the AS1112 status information data (SID) during a greyscale data input cycle.

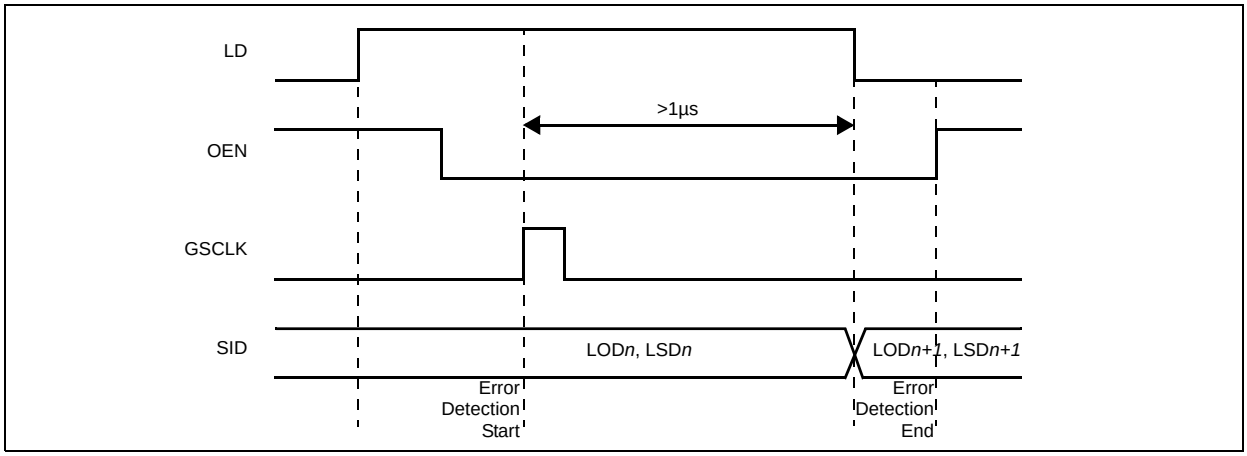
Shorted LED Detection

The AS1112 integrated shorted LED detection circuit detects if any of the 16 LEDs is short-circuited. The shorted LED detection circuit trips when the error detection is activated and the voltage at OUT*n* is higher than V_{LSD}.

Note: The voltage at each OUT*n* is sampled 1µs after being switched on. Please refer to Figure 8.

The shorted LED status of each channel can only be read out from the AS1112 status information data (SID) during a greyscale data input cycle.

Figure 8. Error Detection Timing (GS=FFFF$_{HEX}$, DC=3F$_{HEX}$)



Note: The rising edge of LD latches new data into the internal registers depending on the logic level of the pin MODE. If the pin MODE is tied GND, the greyscale registers are updated. If the pin MODE is tied to VCC, the dot correction registers are updated.

Delay Between Outputs

The AS1112 uses graduated delay circuits between OUT*n* outputs. These circuits are contained in the constant-current driver block of the AS1112 (see Figure 1 on page 1). The average-delay time is 30ns (typ).

The maximum delay is 450ns (typ) from OUT0 to OUT15. The delay scheme works by switching on and switching off each output channel. Thus the on/off time of each channel is the same regardless of the delay. These delays prevent large inrush currents and switching noise that can reduce bypass capacitance when the outputs are switched on.

OUT*n* Enable

All OUT*n* channels can be collectively switched off with one signal. When OEN is set to 1, all OUT*n* channels are disabled, regardless of the device logic operations. The greyscale counter is also reset when OEN is set to 1.

When OEN is set to 0, all OUT*n* channels are in normal operation.

Table 10. Pin OEN Truth Table

OEN	**OUT0:OUT15**
0	Normal Operation
1	Disabled

Setting Maximum Channel Current

The maximum output current per channel is programmed by a single resistor, RIREF, which is placed between pin IREF and GND. The voltage on pin IREF is set by an internal band gap VIREF (1.24V typ). The maximum channel current is equivalent to the current flowing through RIREF multiplied by a factor of 31.5. The maximum output current is calculated as:

$$I_{MAX} = \frac{V_{IREF}}{R_{IREF}} \times 31.5 \qquad \textit{(EQ 1)}$$

Where:

VIREF = 1.24V;
RIREF = User-selected external resistor.

Figure 5 on page 7 shows the maximum output current IOUT versus RIREF, where RIREF is the value of the resistor between IREF terminal to GND, and IOUT is the constant output current of OUT0:OUT15.

Power Dissipation

To ensure proper operation of the device, the total power dissipation of the AS1112 must be below the power dissipation rating of the device package. Total power dissipation is calculated as:

$$PD = (V_{CC} \times I_{CC}) + (V_{OUT} \times I_{MAX} \times n \times \frac{DCn}{63} \; d_{PWM}) \qquad \textit{(EQ 2)}$$

Where:

V_{CC} is the device supply voltage;
I_{CC} is the device supply current;
V_{OUT} is the device OUT*n* voltage when driving LED current;
I_{MAX} is the LED current adjusted by R_{IREF};
DC*n* is the maximum dot correction value for OUT*n*;
n is the number of OUT*n* driving LED at the same time;
d_{PWM} is the duty cycle defined by pin OEN or the greyscale PWM value.

Operating Modes

The AS1112 operates in two modes (see Table 11). Greyscale operating mode (see Figure 12 on page 13) and the shift registers are in reset state at power-up.

Table 11. Operating Modes

Mode	Input Shift Register	Operating Mode
0	192-bit	Greyscale PWM Mode
1	96-bit	Dot Correction Data Input Mode

Setting Dot Correction

The AS1112 can perform independent fine-adjustments to the output current of each channel, i.e., dot correction. Dot correction is used to adjust brightness deviations of LEDs connected to the output channels (OUT0:OUT15).

The 16 channels can be individually programmed with a 6-bit word. The channel output can be adjusted in 64 steps from 0 to 100% of the maximum output current (I_{MAX}). The output current for each OUT*n* channel can be calculated as:

$$I_{OUTn} = I_{MAX} \times \frac{DCn}{63} \qquad \textit{(EQ 3)}$$

Where:

I_{MAX} is the maximum programmable output current for each output;
DC*n* is the programmed dot correction value for output (DC*n* = 0 to 63);
n = 0 to 15

Dot correction data are simultaneously entered for all channels. The complete dot correction data format consists of 16 x 6-bit words, which forms a 96-bit serial data packet (see Figure 9). Channel data is put on one by one, and the data is clocked in with the MSB first.

Figure 9. Dot Correction Data Packet Format

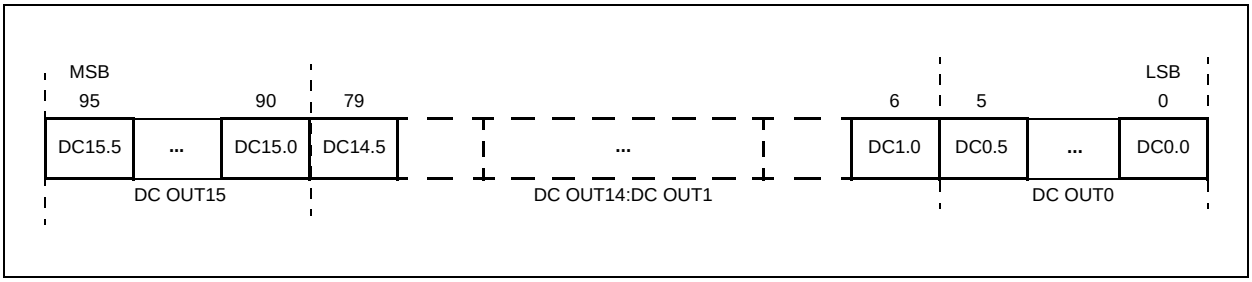
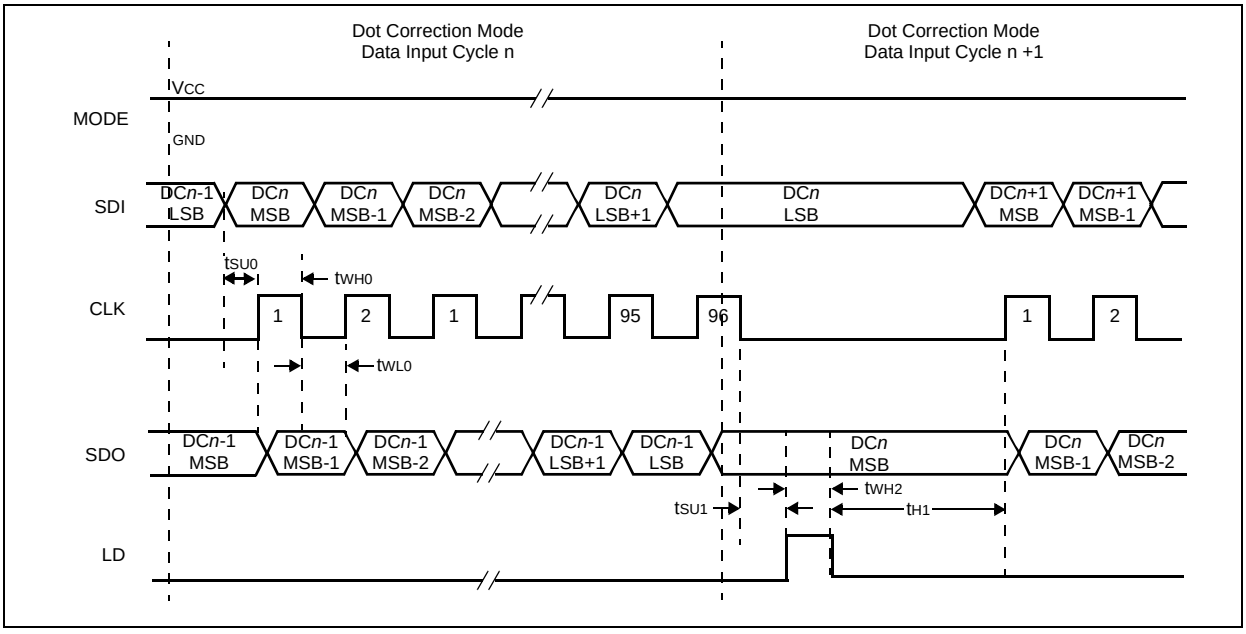


Figure 10. Dot Correction Data Input Timing Diagram



Setting Greyscale Brightness

The brightness of each channel output can be adjusted using a 12 bits-per-channel PWM control scheme which results in 4096 brightness steps, from 0% to 100% brightness. The brightness level for each output is calculated as:

$$\%\text{Brightness} = \frac{GSn}{4095} \times 100 \qquad \textit{(EQ 4)}$$

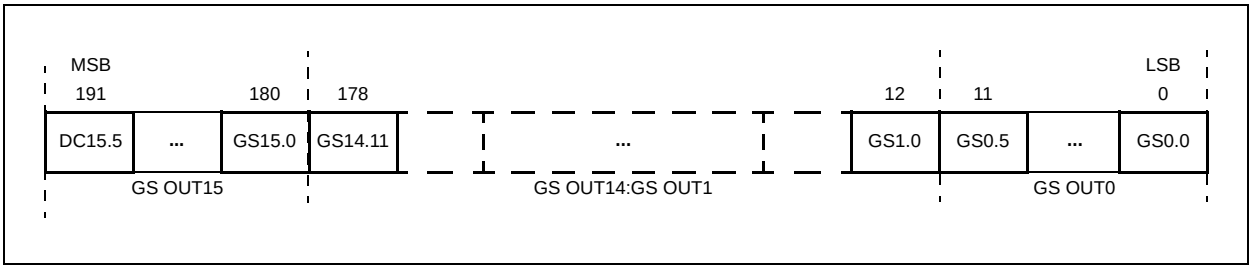
Where:

GS*n* is the programmed greyscale value for OUT*n* (GS*n* = 0 to 4095);
n = 0 to 15 greyscale data for all outputs.

The input shift register shifts greyscale data into the greyscale register for all channels simultaneously. The complete greyscale data format consists of 16 x 12 bit words, which forms a 192-bit wide data packet (see Figure 11).

Note: The data packet must be clocked in with the MSB first.

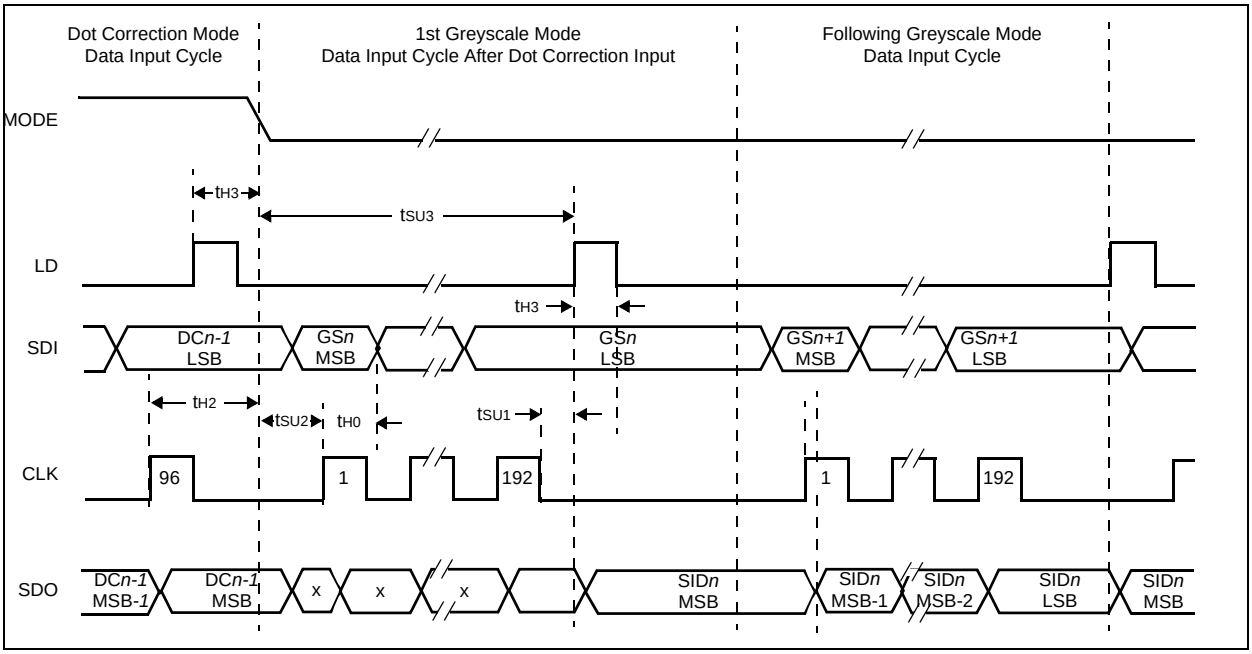
Figure 11. Greyscale Data Packet Format



When pin MODE is tied to GND, the AS1112 enters greyscale data input mode. The device switches the input shift register to 192-bit width. After all data is clocked in, the rising edge of the LD signal latches the data into the greyscale register (see Figure 12).

All greyscale data in the input shift register is replaced with status information data (SID) after latching into the greyscale register.

Figure 12. Greyscale Data Input Timing Diagram

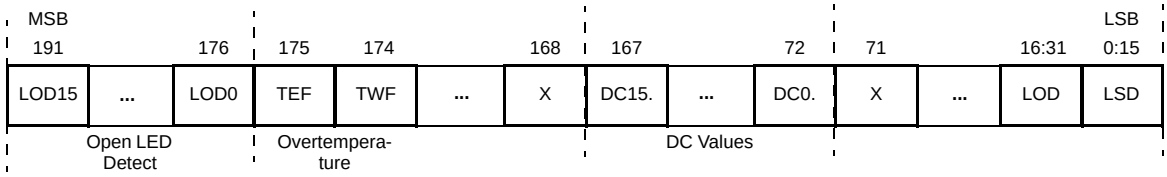


Status Information Data (SID)

The AS1112 contains an integrated status information register, which can be accessed in greyscale mode (MODE = GND). Once the LD signal latches the data into the greyscale register, the input shift register data is replaced with status information data (see Figure 13).

Open, shorted LED, temperature warning and overtemperature flags as well as the dot-correction registers can be read out at pin SDO. The status information data packet is 192 bits wide. Bits 191:176 and 31:16 contain the open LED detection status of each channel (either 191:176 or 31:16 can be used for readout). Bit 175 contains the thermal error flag status. Bit 174 contains the temperature warning flag. Bits 167:72 contain the data of the dot-correction register. Bit 15:0 contains the LED shorted flags. The remaining bits are reserved. The complete status information data packet is shown in Figure 13.

Figure 13. Status Information Data Packet Format



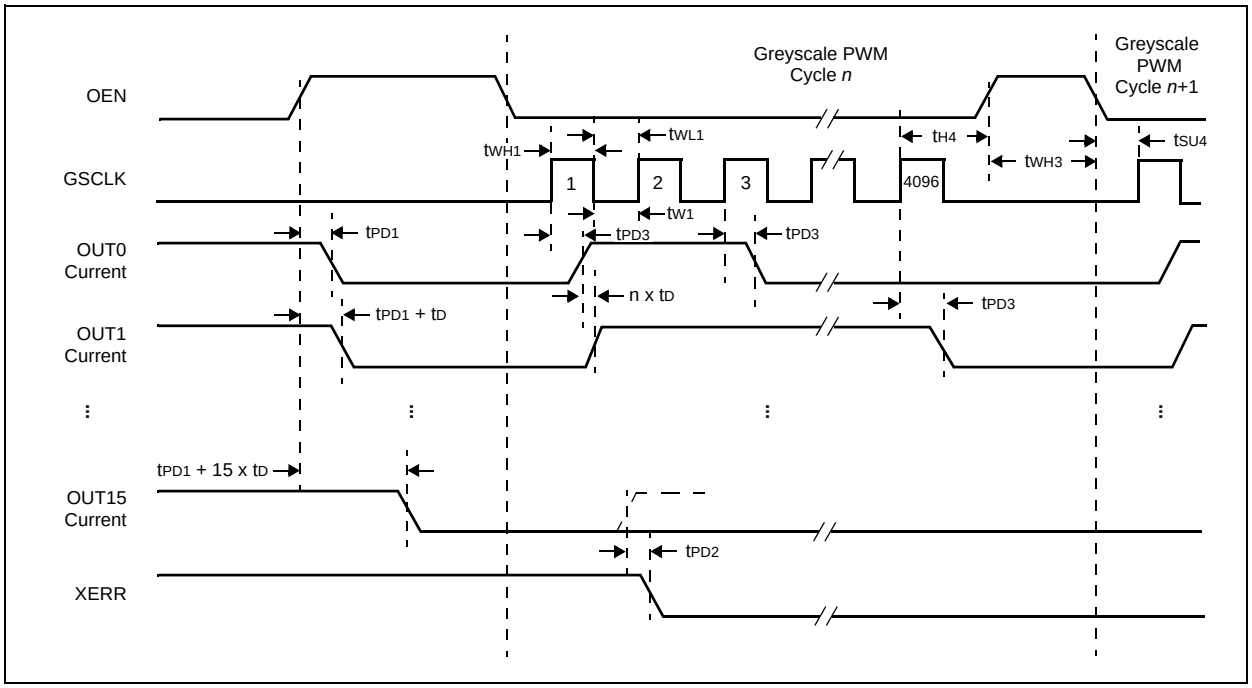
Bit #	Description	Bit #	Description
0:15	LED Short Detection, LSD	168:173	Undefined
16:31	LED Open Detection (Optional, same as bits 176:191), LOD	174	Temperature Warning Flag (TWF, 125ºC, typ)
32:71	Undefined	175	Temperature Error Flag (TEF, 150ºC, typ)
72:167	Dot Correction Readback (16 x 6 Bit)	176:191	LED Open Detection, LOD

Greyscale PWM Operation

The falling edge of the OEN signal initiates a greyscale PWM cycle. The first GSCLK pulse after the falling edge of OEN increments the greyscale counter by one and switches on any OUT*n* whose greyscale value does not equal zero. Each subsequent rising edge of GSCLK increments the greyscale counter by one.

The AS1112 compares the greyscale value of each OUT*n* channel with the greyscale counter value. All OUT*n* whose greyscale values equal the counter values are switched off. A OEN = 1 signal after 4096 GSCLK pulses resets the greyscale counter to zero and completes a greyscale PWM cycle (see Figure 14).

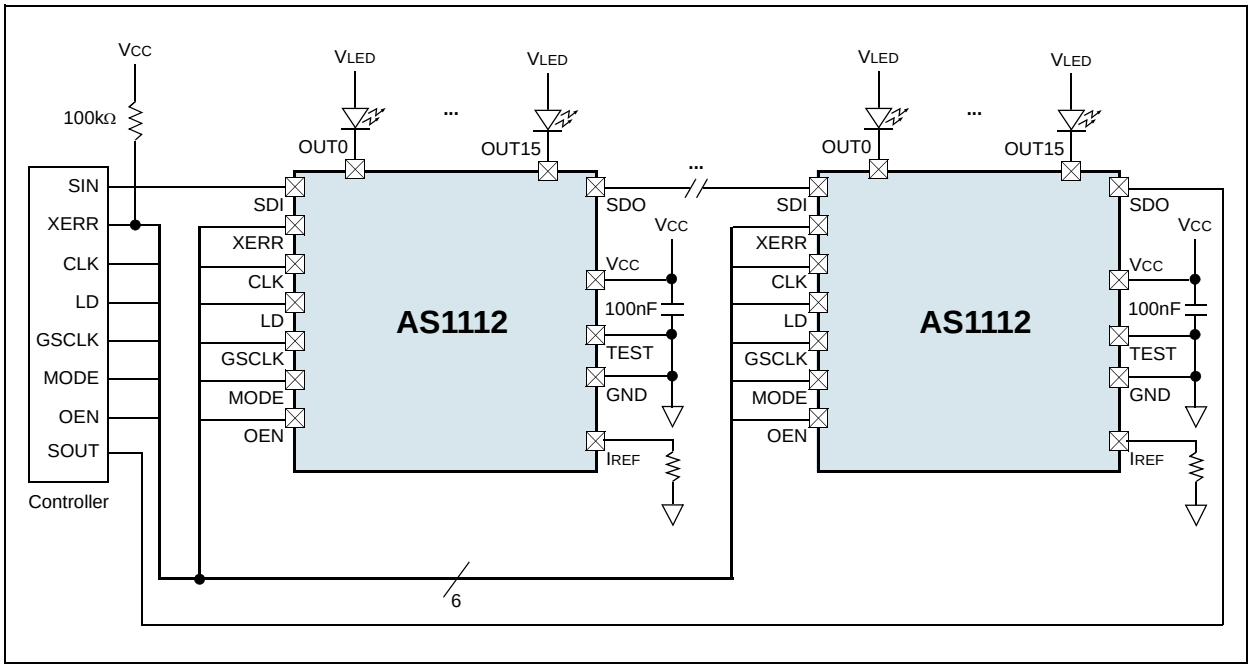
Figure 14. Greyscale PWM Cycle Timing Diagram



Serial Data Transfer Rate

Figure 15 shows a cascaded arrangement AS1112 devices connected to a controller, building a basic module of an LED display system.

Figure 15. Cascaded Configuration



The maximum number of cascading AS1112 devices depends on the application system and is in the range of 40 devices. The minimum frequency needed can be calculated by the following equations:

$$f_{GSCLK} = 4096 \times f_{UPDATE} \quad \textit{(EQ 5)}$$

Where:

f_{GSCLK} is the minimum frequency needed for GSCLK;

f_{UPDATE} is the update rate of whole cascaded system.

$$f_{CLK} = 193 \times f_{UPDATE} \times n \quad \textit{(EQ 6)}$$

Where:

f_{CLK} is the minimum frequency needed for CLK and SIN;

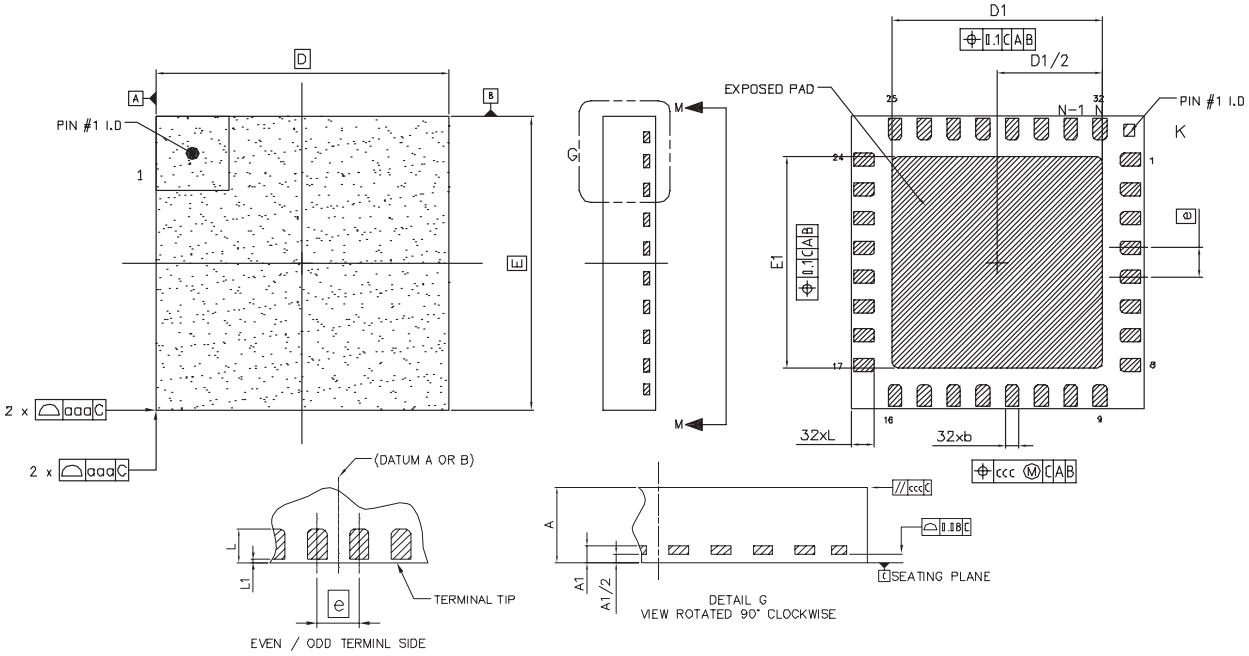
f_{UPDATE} is the update rate of whole cascaded system;

n is the number of cascaded of AS1112 devices.

10 Package Drawings and Markings

The device is available in an 32-pin TQFN 5x5 mm package.

Figure 16. 32-pin TQFN 5x5 mm Package



Common Dimensions								
Symbol	**Min**	**Nom**	**Max**		**Symbol**	**Min**	**Nom**	**Max**
A	0.80		1.00		e		0.5 BSC	
A1		0.203 REF			L	0.30	0.40	0.50
b	0.18	0.23	0.30		L1			0.10
D		5.00 BSC			P		45° BSC	
E		5.00 BSC			aaa		0.15	
D1	3.50	3.60	3.70		ccc		0.10	
E1	3.50	3.60	3.70					

Notes:

1. Dimensioning and tolerancing conform to *ASME Y14.5 M-194*.
2. All dimensions are in millimeters while angle is in degrees.
3. Dimension b applies to metallized terminal and is measured between 0.25mm and 0.30mm from the terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal
5. Radius on terminal is optional.

11 Ordering Information

The device is available as the standard products shown in Table 12.

Table 12. Ordering Information

Model	Description	Delivery Form	Package
AS1112-BQFT	16-Channel LED Driver with Dot Correction and Greyscale PWM with Active-High TEST Input and Power-Down Mode	Tape and Reel	32-pin TQFN 5x5 mm
AS1112B-BQFT	16-Channel LED Driver with Dot Correction and Greyscale PWM with Active-Low XTEST Input and without Power-Down Mode	Tape and Reel	32-pin TQFN 5x5 mm

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