

AS13985

Micropower 150mA Low-Noise LDO

Data Sheet

1 General Description

The AS13985 is a high-performance low-dropout 150mA voltage regulator designed for use with very-low ESR output capacitors. The device can deliver superior performance in all specifications critical to battery-powered designs, and is perfectly suited for mobile phones, PDAs, MP3 players, and other battery powered devices.

Stability is guaranteed with a ceramic output capacitor from 1 to 22 μ F. The low equivalent series resistance of these capacitors ensures low output impedance at high frequencies.

Automatic sleep mode requires less than 1 μ A quiescent current when pin EN is pulled low.

Regulation performance is excellent even under low dropout conditions, when the power transistor has to operate in linear mode.

A 10nF bypass capacitor can be added to reduce output noise to 30 μ V. The low-noise performance allows direct connection of noise sensitive circuits without additional filtering networks.

Multiple output voltage options are available as standard products. Contact austriamicrosystems AG for details.

The AS13985 is available in a 5-bump WLP package and a 5-pin SOT23 package.

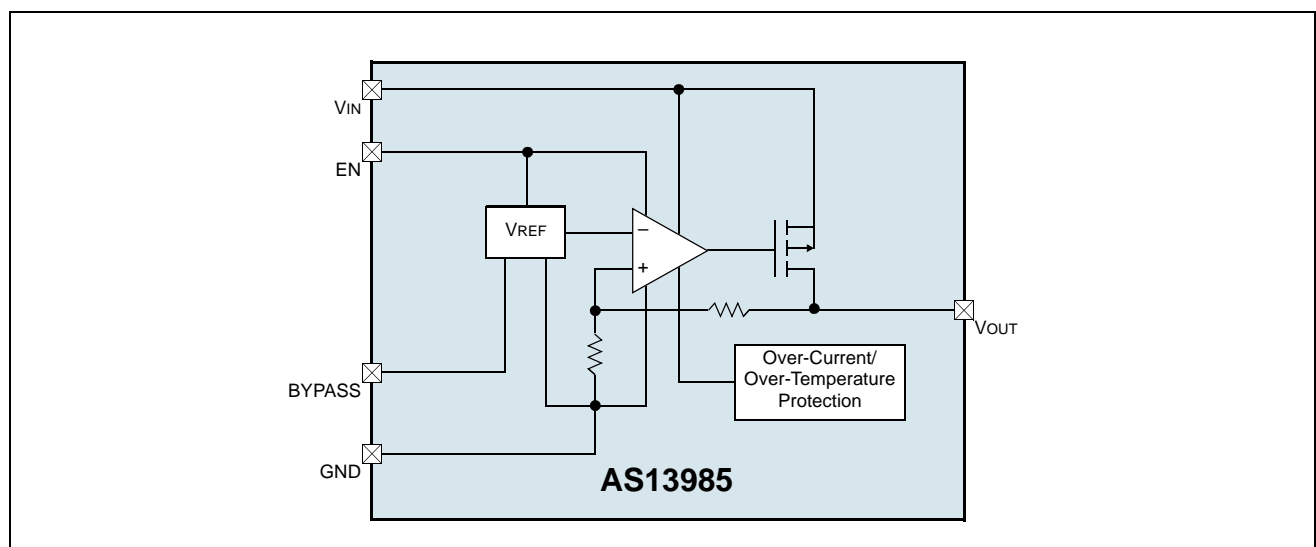
2 Key Features

- Ultra-Low Dropout Voltage (typically 45mV @ 150mA, 0.3mV @ 1mA)
- Supply Range: 2.5 to 5.5V
- Output Voltage Range: 1.2 to 5.0V (in 25mV Steps)
- Output Current: 150mA (Guaranteed)
- Stable with Low-ESR Output Capacitor
- Integrated Over-Temperature/Over-Current Protection
- Low GND Pin Current (only 95 μ A)
- Output Voltage Accuracy: 1%
- Minimal External Components Required
- High Peak-Current Capability
- Low Shutdown Current: \leq 1 μ A
- Operating Temperature Junction Range: -40 to +125 $^{\circ}$ C
- Smallest Available Packages:
 - 5-bump WLP
 - 5-pin SOT23

3 Applications

The AS13985 is ideal for powering cordless and mobile phones, MP3 players, CD and DVD players, PDAs, hand-held computers, digital cameras, and any other hand-held battery-powered device.

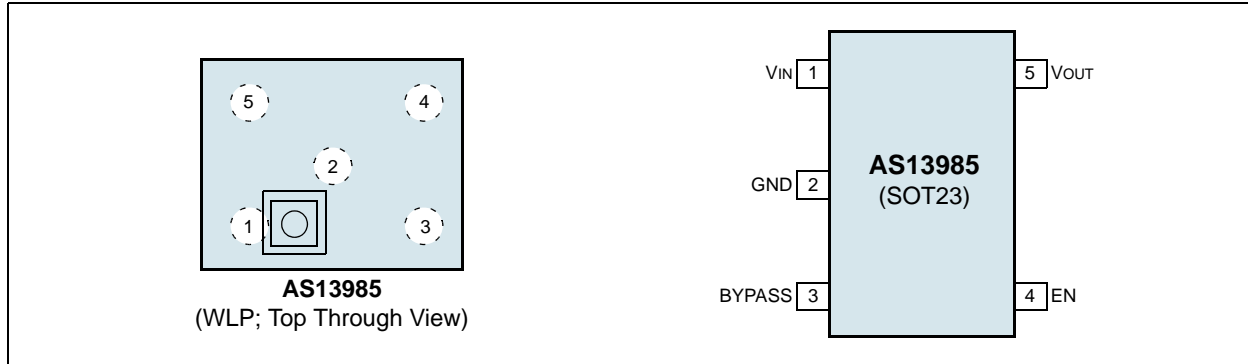
Figure 1. Block Diagram



4 Pinout

4.1 Pin Assignments

Figure 2. Pin Assignments (Top View)



4.2 Pin Descriptions

Table 1. Pin Descriptions

Name	WLP	SOT23	Description
V _{IN}	4	1	Input Voltage
GND	2	2	Ground
BYPASS	5	3	Low-Noise Operation Bypass Capacitor
EN	1	4	Logic-High Enable Input. $V_{EN} \geq 1.2V$: V _{OUT} is enabled. $V_{EN} \leq 0.4V$: V _{OUT} is disabled. Note: This pin must not float as it is internally pulled up or down.
V _{OUT}	3	5	Regulated Output Voltage

5 Absolute Maximum Ratings

Stresses beyond those listed in [Table 2](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 6 Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Input Supply Voltage (Survival)	-0.3	+7	V	
Input Supply Voltage (Operating)	+2.5	+5.5	V	
Shutdown Input Voltage (Survival)	-0.3	+7	V	
Output Voltage (Survival)	-0.3	+7	V	
I _{OUT} (Survival)				Short-circuit protected.
Input/Output Voltage (Survival) ¹	-0.3	+7	V	
Power Dissipation ²				Internally limited.
Operating Junction Temperature	-40	+125	°C	
Storage Temperature Range	-65	+150	°C	
Package Body Temperature		+260	°C	The reflow peak soldering temperature (body temperature) specified is in accordance with <i>IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices"</i> . The lead finish for Pb-free leaded packages is matte tin (100% Sn).

1. The output PNP structure contains a diode between pins V_{IN} and V_{OUT} that is normally reverse-biased. reversing the polarity of pins V_{IN} and V_{OUT} will activate this diode.
2. The maximum allowable power dissipation is a function of the maximum junction temperature (T_{J(MAX)}), the junction-to-ambient thermal resistance (Θ_{JA}), and the ambient temperature (T_{AMB}). The maximum allowable power dissipation at any ambient temperature is calculated as:

$$P_{(MAX)} = (T_{J(MAX)} - (T_{AMB})) / \Theta_{JA} \quad (EQ 1)$$

Where:

The value of Θ_{JA} for the SOT23 package is 220°C/W in a typical PC-board mounting.

The value of Θ_{JA} for the WLP package is 225°C/W.

Note: Exceeding the maximum allowable dissipation will cause excessive device temperature and the regulator will go into thermal shutdown.

6 Electrical Characteristics

$T_{AMB} = 25^{\circ}\text{C}$, $V_{IN} = V_{OUT(NOM)} + 0.5\text{V}$, $C_{OUT} = C_{IN} = 1\mu\text{F}$, $C_{BYPASS} = 10\text{nF}$, $I_{OUT} = 1\text{mA}$, $V_{EN} = 1.4\text{V}$ (unless otherwise specified)

Caution: Exposing the WLP package to direct light could cause device malfunction.

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V_{IN}	Operating Input Voltage		2.5		5.5	V	
$V_{OUT(NOM)} - V_{OUT}$	Output Voltage Accuracy < 2.5V V_{OUT}	$I_{OUT} = 1\text{mA}$	-50		50	mV	
		$T_{AMB} = -40$ to 125°C	-75		75		
	Output Voltage Accuracy $\geq 2.5\text{V } V_{OUT}$	$I_{OUT} = 1\text{mA}$	-1		1	% of $V_{OUT(NOM)}$	
		$T_{AMB} = -40$ to 125°C	-2		2		
ΔV_{OUT}	Line Regulation ¹	$V_{IN} = (V_{OUT(NOM)} + 0.5\text{V})$ to 4.5V , $V_{OUT} < 3\text{V}$	-0.15		0.15	%/ V	
		$V_{IN} = (V_{OUT(NOM)} + 0.5\text{V})$ to 5.5V , $V_{OUT} < 3\text{V}$	-0.3		0.3		
	Load Regulation	$I_{OUT} = 1$ to 150mA , $V_{OUT} < 2.5\text{V}$, $T_{AMB} = -40$ to 125°C			0.002	0.008	%/ mA
		$I_{OUT} = 1$ to 150mA , $V_{OUT} \geq 2.5\text{V}$, $T_{AMB} = -40$ to 125°C (for WLP)			0.0004	0.002	
		$I_{OUT} = 1$ to 150mA , $T_{AMB} = -40$ to 125°C (for SOT23-5), $V_{OUT} \geq 2.5\text{V}$			0.0025	0.005	
Output AC Line Regulation	$V_{IN} = V_{OUT(NOM)} + 1\text{V}$, $I_{OUT} = 150\text{mA}$, $t_r = t_f = 30\mu\text{s}$			1		mV _{PP}	
I_Q	Quiescent Current	On Mode: $V_{EN} = 1.2\text{V}$, $I_{OUT} = 0\text{mA}$		95		μA	
		On Mode: $V_{EN} = 1.2\text{V}$, $I_{OUT} = 0\text{mA}$, $T_{AMB} = -40$ to 125°C			130		
		On Mode: $V_{EN} = 1.2\text{V}$, $I_{OUT} = 0$ to 150mA		160			
		On Mode: $V_{EN} = 1.2\text{V}$, $I_{OUT} = 0$ to 150mA , $T_{AMB} = -40$ to 125°C			250 ²		
		Off Mode: $V_{EN} = 0.4\text{V}$, $I_{OUT} = 0\text{mA}$		0.003 ²			
		Off Mode: $V_{EN} = 0.4\text{V}$, $T_{AMB} = -40$ to 125°C , $I_{OUT} = 0\text{mA}$			1		
V_{DROP}	Dropout Voltage ³	$I_{OUT} = 1\text{mA}$		0.3		mV	
		$I_{OUT} = 1\text{mA}$, $T_{AMB} = -40$ to 125°C			2 ²		
		$I_{OUT} = 50\text{mA}$		15			
		$I_{OUT} = 50\text{mA}$, $T_{AMB} = -40$ to 125°C			35		
		$I_{OUT} = 100\text{mA}$		30			
		$I_{OUT} = 100\text{mA}$, $T_{AMB} = -40$ to 125°C			70		
		$I_{OUT} = 150\text{mA}$		45			
$I_{OUT} = 150\text{mA}$, $T_{AMB} = -40$ to 125°C			100				
I_{SC}	Short Circuit Current	$R_{LOAD} = 0\Omega$		500		mA	
SVR	Supply Voltage Rejection	$V_{IN} = V_{OUT(NOM)} + 1\text{V}$, $V_{RIPPLE} = 50\text{mV}$, $I_{OUT} = 50\text{mA}$, $f = 1\text{kHz}$		60		dB	
		$V_{IN} = V_{OUT(NOM)} + 1\text{V}$, $V_{RIPPLE} = 50\text{mV}$, $I_{OUT} = 50\text{mA}$, $f = 10\text{kHz}$		55			
$I_{OUT(PK)}$	Peak Output Current	$V_{OUT} \geq V_{OUT(NOM)} - 5\%$	300	500		mA	
V_{EN}	Enable Input Logic Low	$V_{IN} = 2.5$ to 5.5V , $T_{AMB} = -40$ to 125°C ⁴			0.4	V	
	Enable Input Logic High		1.2				

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{EN}	Enable Input Current	V _{EN} = 0.4V, V _{IN} = 5.5V		±1 ²		nA
e _N	Output Noise Voltage	BW = 10Hz to 100kHz, C _{OUT} = 1μF, I _{OUT} = 0mA		30		μVRMS
t _{ON}	Turn On Time ⁵	C _{BYPASS} = 10nF		150	250	μs
T _{SHDN}	Thermal Shutdown Threshold ^{4, 6}			160		°C
Recommended Output Capacitor						
C _{OUT}	Output Capacitor	Capacitance	1		22 ²	μF
		ESR	5		5000	mΩ

1. Temperature variations are included within the output voltage accuracy.
2. Guaranteed by design.
3. Dropout voltage is the input-to-output voltage difference at which the output voltage is 100mV below its nominal value (does not apply to input voltages below 2.5V).
4. EN must be driven with a $t_R = t_F < 10\text{ms}$.
5. Turn on time is time measured between the enable input just exceeding the V_{EN} high value and the output voltage just reaching 95% of its nominal value.
6. Typical thermal protection hysteresis is 20°C.

Figure 3. AC Line Regulation Input Voltage Test Signal

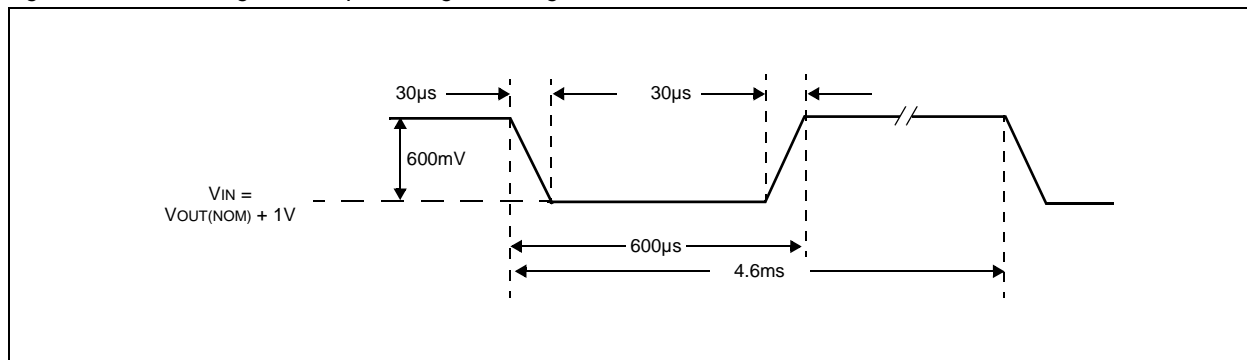
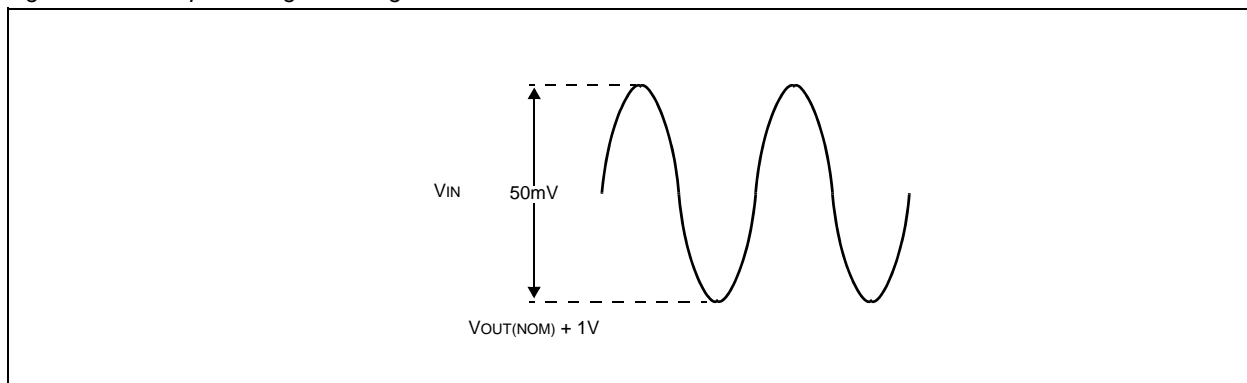


Figure 4. SVR Input Voltage Test Signal



7 Typical Operating Characteristics

$T_{AMB} = +25^{\circ}\text{C}$ (unless otherwise specified)

Figure 5. Output Voltage vs. Temperature;
 $V_{IN} = 3.4\text{V}$, $V_{SHDN} = 1.4\text{V}$, $I_{OUT} = 1\text{mA}$

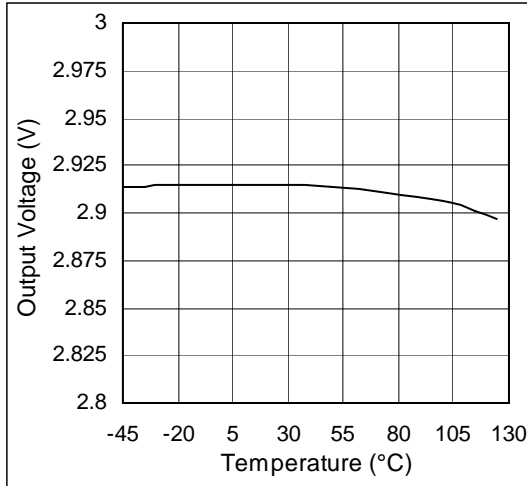


Figure 7. Load Regulation vs. Temperature;
 $V_{IN} = 3.4\text{V}$, $V_{SHDN} = 1.4\text{V}$, $I_{OUT} = 1$ to 150mA

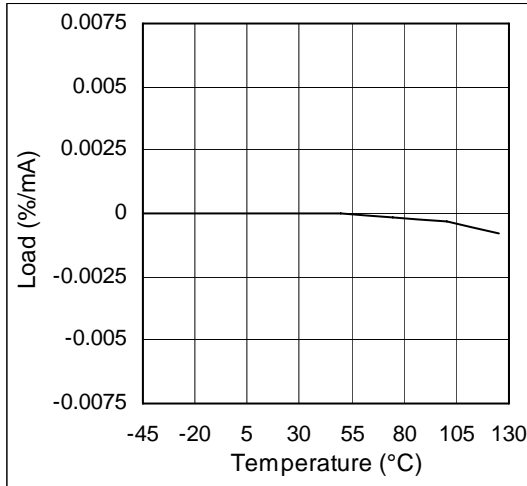


Figure 9. SVR vs. Frequency; $V_{IN} = 3.9$ to 3.95V ,
 $V_{OUT} = 2.9\text{V}$, $I_{OUT} = 50\text{mA}$, $V_{SHDN} = 1.4\text{V}$

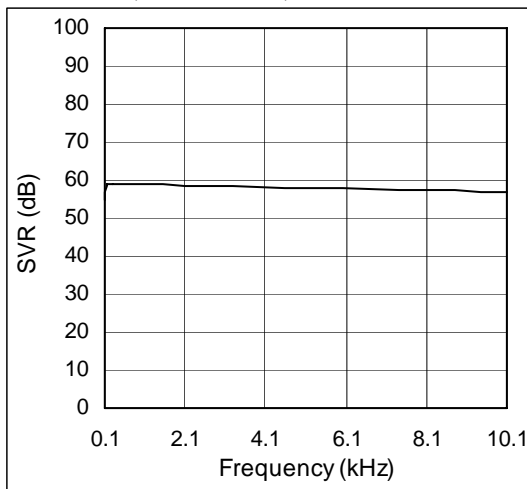


Figure 6. Shutdown Voltage vs. Temperature;
 $V_{OUT} = 2.9\text{V}$, $I_{OUT} = 10\text{mA}$

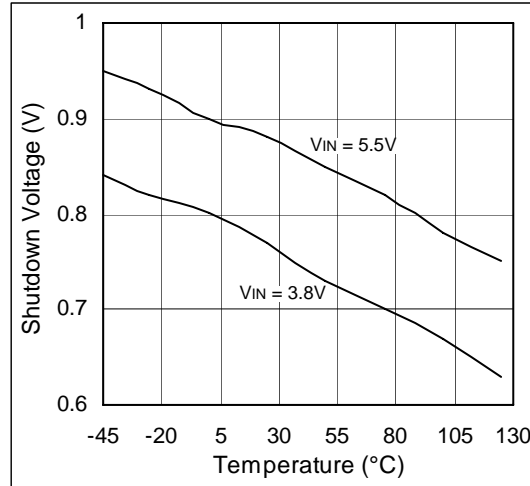


Figure 8. Line Regulation vs. Temperature;
 $V_{IN} = 3.4$ to 5.0V , $V_{SHDN} = 1.4\text{V}$, $I_{OUT} = 1\text{mA}$

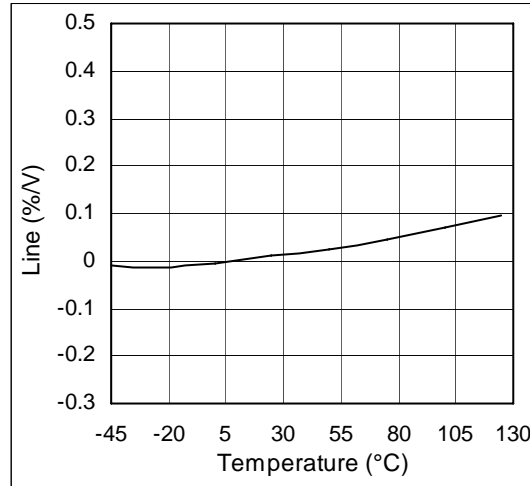


Figure 10. Quiescent Current vs. Temperature;
 $V_{OUT} = 2.9\text{V}$, $V_{SHDN} = 1.4\text{V}$

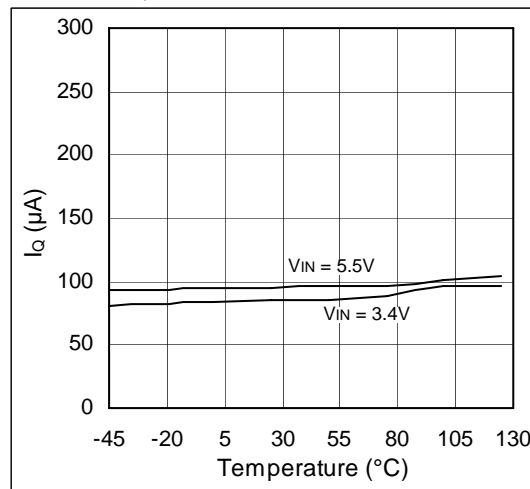


Figure 11. Line Transient Response; $V_{IN} = 3.8$ to $4.4V$, $T_J = 25^\circ C$, $I_{OUT} = 150mA$, $C_{IN} = C_{OUT} = 1\mu F$, $V_{OUT} = 2.7V$, $C_{BYPASS} = 10nF$, Rise Time/Fall Time = $1\mu s$

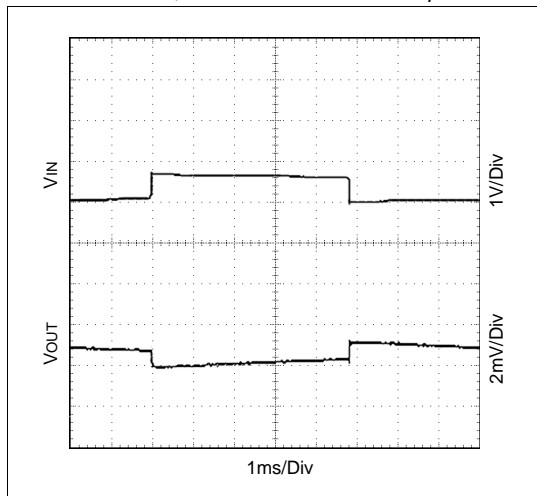
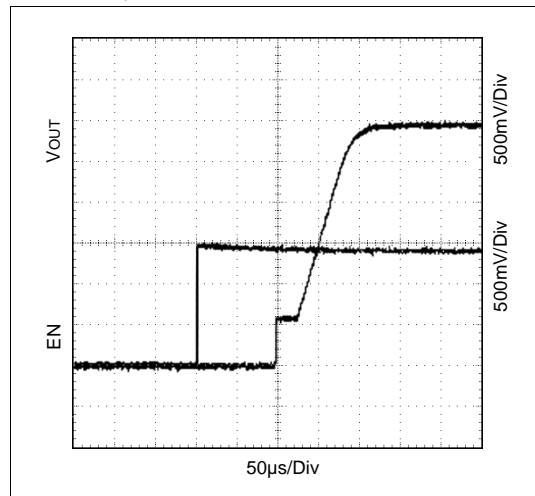
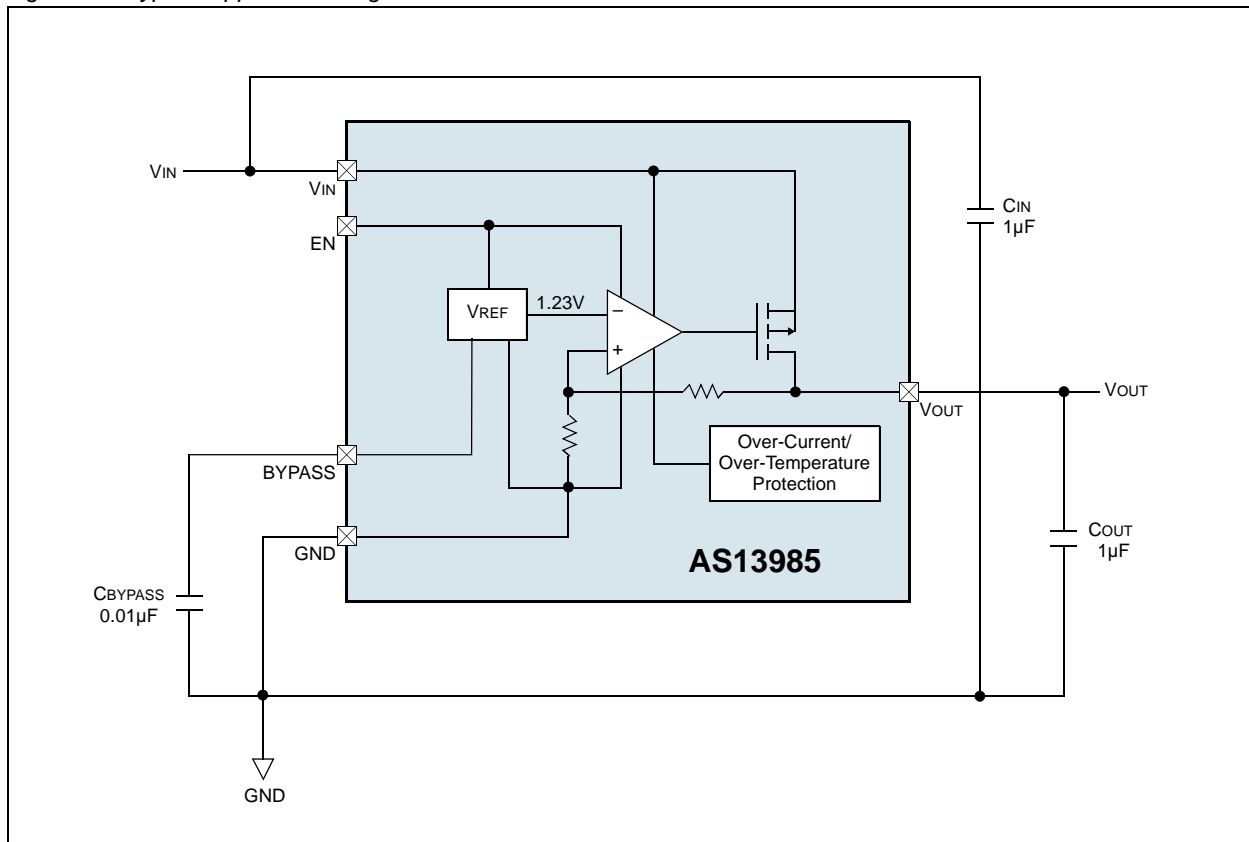


Figure 12. Turn On Time; $V_{IN} = 3.3V$, $C_{BYPASS} = 10nF$, $C_{IN} = C_{OUT} = 1\mu F$ (Ceramic), $t_R = 20ns$, $I_{OUT} = 1mA$, $V_{OUT} = 2.8V$



8 Typical Application

Figure 13. Typical Application Diagram



9 Package Drawings and Markings

The AS13985 is available in a 5-bump WLP package and a 5-pin SOT23 package.

Figure 14. 5-bump WLP Package

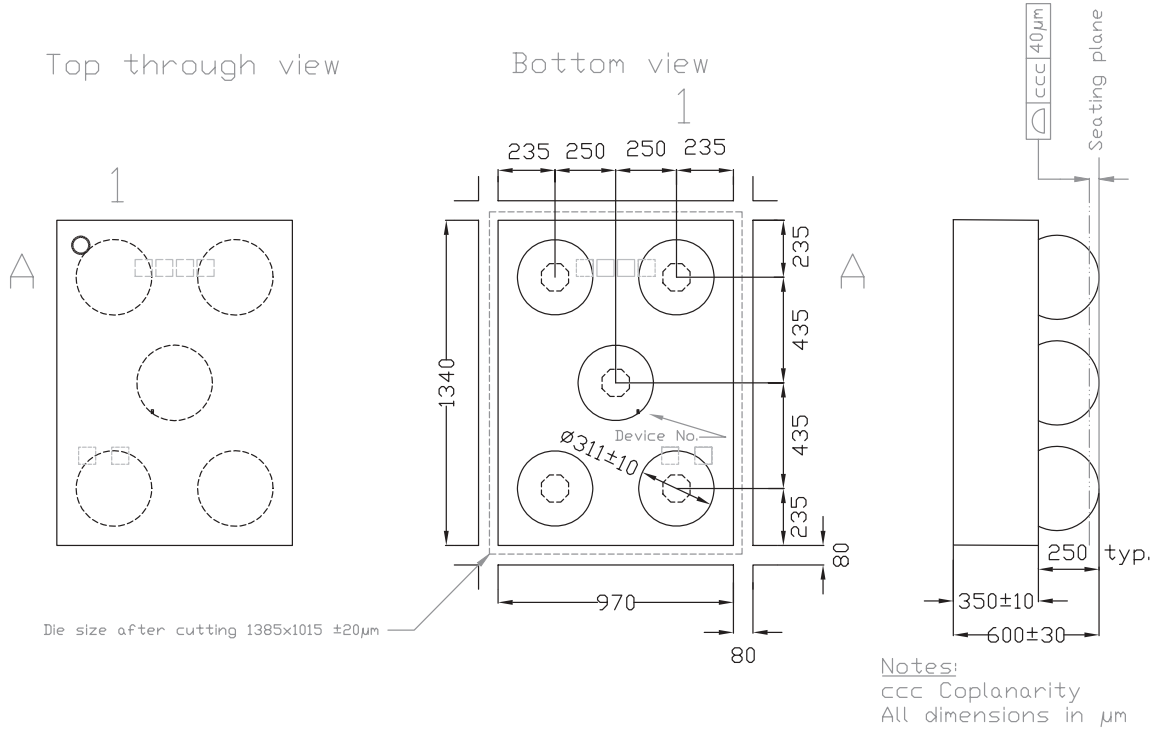
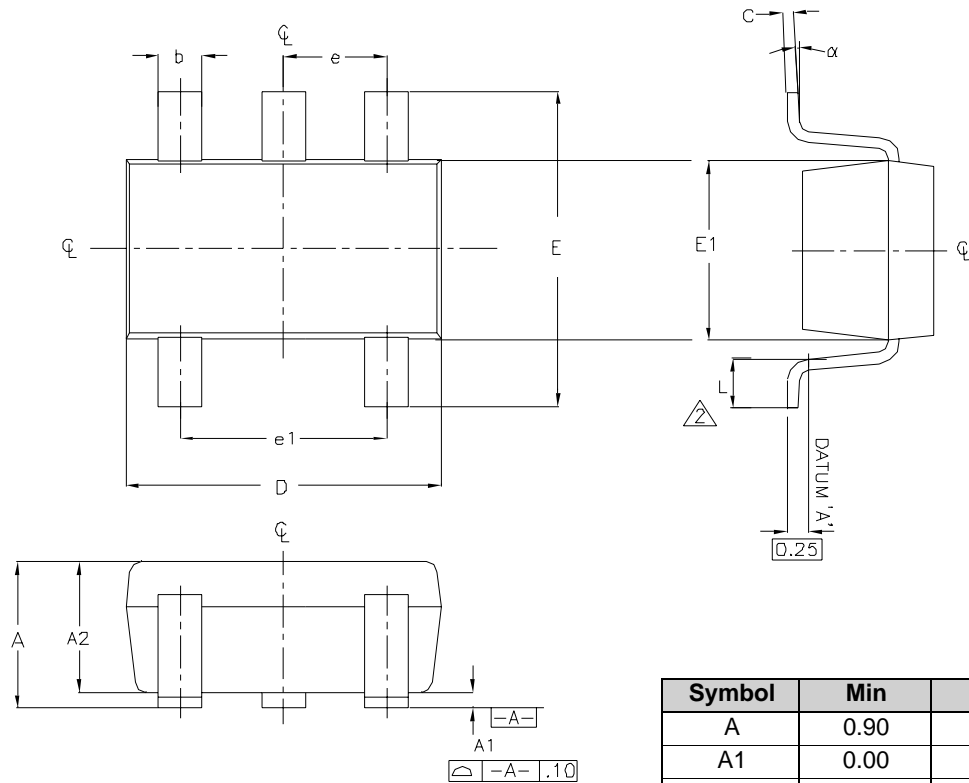


Figure 15. 5-pin SOT23 Package

**Notes:**

1. All dimensions are in millimeters.
2. Foot length is measured at the intercept point between datum A and lead surface.
3. Package outline exclusive of mold flash and metal burr.
4. Package outline inclusive of solder plating.
5. Complies with EIAJ SC74.

Symbol	Min	Max
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.30	0.50
C	0.09	0.20
D	2.80	3.05
E	2.60	3.00
E1	1.50	1.75
L	0.30	0.55
e	0.95 Ref	
e1	1.90 Ref	
α	0°	8°

10 Ordering Information

The AS13985 is available as the standard versions listed in [Table 4](#). Other versions are available upon request. Contact austriamicrosystems, AG for more information.

Table 4. Ordering Information

Model	Marking	Description	Delivery Form	Package
AS13985F33-T	ASKK	3.3V LDO, 150mA	Tape and Reel	5-bump WLP
AS13985F30-T	ASKJ	3.0V LDO, 150mA	Tape and Reel	5-bump WLP
AS13985F29-T	ASKI	2.9V LDO, 150mA	Tape and Reel	5-bump WLP
AS13985F28-T	ASLE	2.8V LDO, 150mA	Tape and Reel	5-bump WLP
AS13985F27-T	ASKL	2.7V LDO, 150mA	Tape and Reel	5-bump WLP
AS13985F18-T	ASKM	1.8V LDO, 150mA	Tape and Reel	5-bump WLP
AS13985F12-T	ASKN	1.2V LDO, 150mA	Tape and Reel	5-bump WLP
AS13985H33-T	ASK0	3.3V LDO, 150mA	Tape and Reel	5-pin SOT23
AS13985H30-T	ASK1	3.0V LDO, 150mA	Tape and Reel	5-pin SOT23
AS13985H29-T	ASK2	2.9V LDO, 150mA	Tape and Reel	5-pin SOT23
AS13985H28-T	ASLF	2.8V LDO, 150mA	Tape and Reel	5-pin SOT23
AS13985H27-T	ASK3	2.7V LDO, 150mA	Tape and Reel	5-pin SOT23
AS13985H18-T	ASK4	1.8V LDO, 150mA	Tape and Reel	5-pin SOT23
AS13985H12-T	ASK5	1.2V LDO, 150mA	Tape and Reel	5-pin SOT23

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