ADNS-5700

PCB Design Guidelines for ADNS-5700 One Chip USB LED Sensor

Application Note 5417

Lead (Pb) Free
RoHS 6 fully
compliant

Introduction

The ADNS-5700 is a one chip USB LED optical mouse sensor. The purpose of this application note is to provide printed circuit board (PCB) design recommendations that can guide mouse manufacturer to produce a good quality LED mouse for optimum performance.

A good USB corded mouse design should demonstrate good performance in all areas including:

- Passes EN 61000-4-4/IEC 801-4 Electrical Fast Transient (EFT) test
- Passes FCC Part 15C Class B and worldwide analogous emission limits (EMI)
- Passes IEC 61000-4-2:2001Electrostatic discharge(ESD) immunity test

PCB Design Recommendations

The application circuit as shown in Figure 1 was designed to form a good navigation system for ADNS-5700. In order to pass the above three regulatory standard criteria, the PCB can follow some guidelines as outlined below.

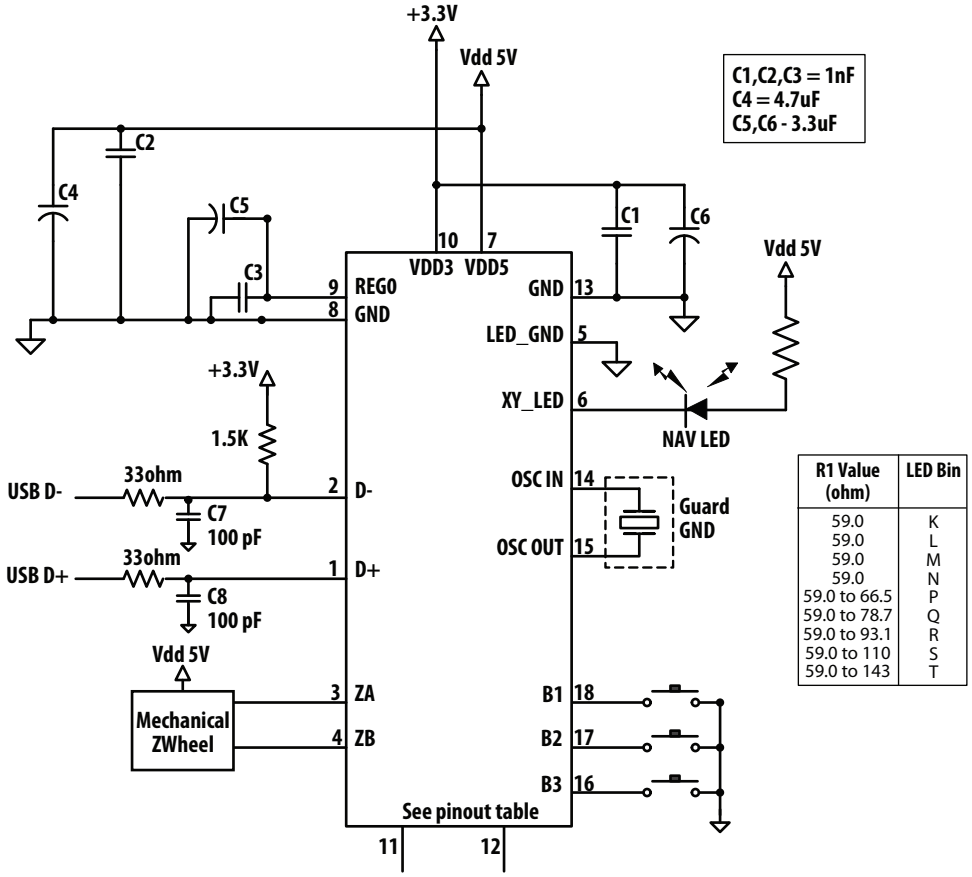

Figure 1. ADNS-5700 Sensor application schematics

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PCB Layout Design and Assembly Recommendations

1. Grounding

A good grounding layout can enhance the EMI, EFT and ESD performance.

- MUST have a continuous ground plane and unbroken plane from USB connector to sensor ground pins 8 and 13. The plane should be as short and thick as possible.
- MUST NOT use jumper to connect the GND planes. GND plane should be the largest piece in the layout.
- Connect USB-GND and USB-Shield planes as a single plane. The sensor grounding pins 9 and 13 are to be connected to USB-GND directly.
- All decoupling capacitors as shown in the application schematic should be connected to their respective GND plane.

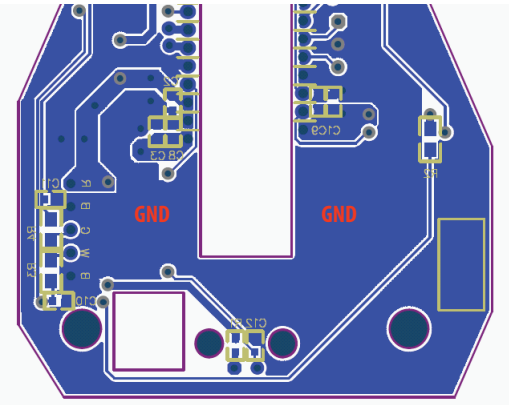

Figure 2. Grounding Layout

2. VDD5

VDD5 is the 5volts power supply from USB bus to ADNS-5700 sensor. This VDD5 power line can be layout as a small plane or a single line with the recommended value of decoupling capacitors to DGND. The power line path should be as short as possible and jumper can be used if necessary. See Figure 5.

3. D+ and D−

- D+ and D− are the USB data lines. Both data lines must be layout in same length with the shortest possible path and placed as far away from the resonator or high frequency traces. In addition, avoid using any jumpers on these data lines. Good layout practice on data lines can improve on EMI performance. In addition the parallel D+/− traces can be contained by ground plane to reduce coupling effects from high frequency traces.

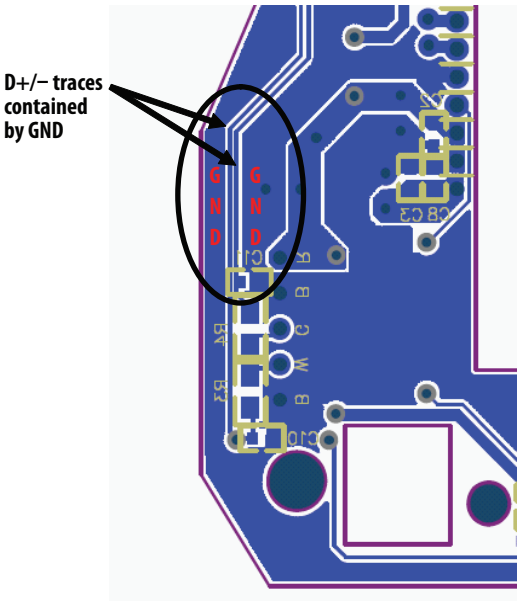

Figure 3. Grounding Layout

- The D+ and D− MUST be filtered with 33ohm and 100pF circuit.

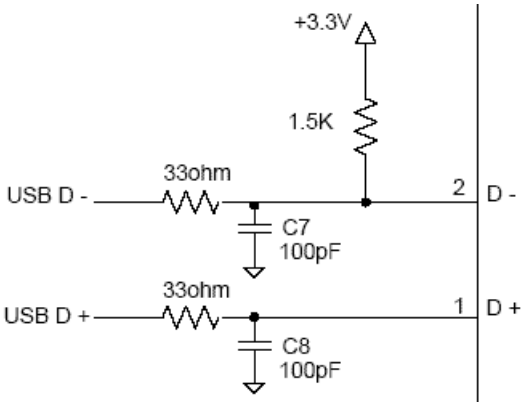

Figure 4. D+/− circuit

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4. **Capacitors**
   - MUST have a 3.3uF and 1nF capacitor each on pin 9 and 10. The capacitors return path to ground for REG0 pin 9 to 8 and for VDD3 pin 10 to 13.
   - All caps MUST be as close to VDD5, VDD3, REG0 sensor pins as possible and ground at their respective sensor GND pins with trace length less than 5mm.
   - Ceramic non-polarity caps and tantalum polarity caps are recommended.
   - Caps should have less than 5nH of self inductance.

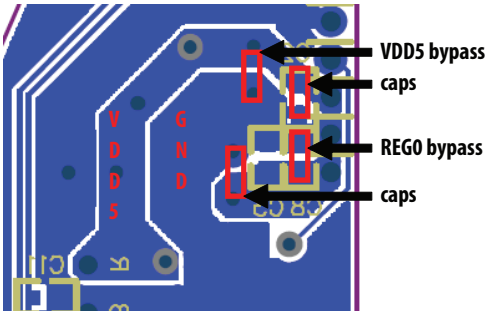

Figure 5. VDD5 and REG0 bypass circuit

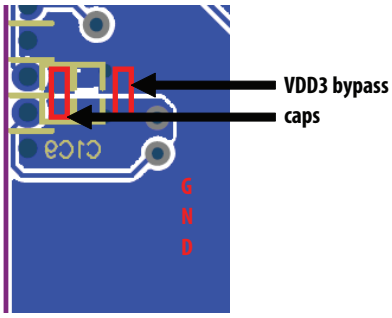

Figure 6. VDD3 bypass circuit

5. **1.5KΩ pull up resistor**
   - The 1.5kΩ pullup resistor should be ± 1% tolerance and can be placed near to either ADNS-5700 chip or USB connection point.

6. **Resonator**
   - The traces from sensor to resonator MUST be equal and symmetrical in length.
   - The PCB area around the resonator MUST be guarded with ground plane.
   - It is recommended to use a ground shielded oscillator with 3 pins where the middle pin is ground.

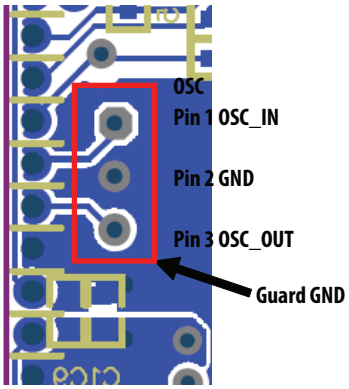

Figure 7. Oscillator Layout

7. **USB Cable**
   - MUST use a shielded USB cable to provide better EMI immunity.

8. **Jumpers**
   - It is recommended not use jumper on GND, D+ and D− lines but jumper is allowed on digital lines: Buttons (B1, B2, B3, B4 & B5), Z-wheel (ZA & ZB) and Tilt-wheel (TW1 & TW2).

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AV02-1737EN - January 15, 2009

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