1 MSPS 12-Bit Impedance Converter, Network Analyzer

Preliminary Technical Data

AD5933

FEATURES

50KHz Max Excitation Output
Impedance Range .1k-20M, 12 Bit Resolution
Selectable System Clock from the following:
PLL, RC Oscillator, External Clock
DSP Real and Imaginary Calculation (FFT)
3V Power Supply,
Programmable Sinewave Output
Frequency Resolution 27 Bits (<0.1Hz)
Frequency Sweep Capability
12 Bit Sampling ADC
ADC Sampling 1MSPS, INL +/- 1LSB Max.
On Chip Temp Sensor allows +/-2 oC accuracy
Serial ^{I2}C Loading
Temperature Range –40-125oC 16 SSOP

APPLICATIONS

Complex Impedance Measurement
Impedance Spectrometry
Biomedical and Automotive Sensors
Proximity Sensors
FFT Processing

GENERAL DESCRIPTION

The AD5933 is a high precision impedance converter system solution which combines an on board frequency generator with a 12 Bit 1MSPS ADC. The frequency generator allows an external complex impedance to be excited with a known frequency. The response signal from the impedance is sampled by the on board ADC and FFT processed by an on-board DSP engine. The FFT algorithm returns a Real (R) and Imaginary (I) data word, allowing impedance to be conveniently calculated. The impedance magnitude and phase is easily calculated using the following equations:

$$\text{Magnitude} = \sqrt{R^2 + I^2}$$

$$\text{Phase} = \text{Tan}^{-1}\ (I/R)$$

To determine the actual real impedance value Z(W) , generally a frequency sweep is performed. The impedance can be calculated at each point and a frequency vs magnitude plot can be created.

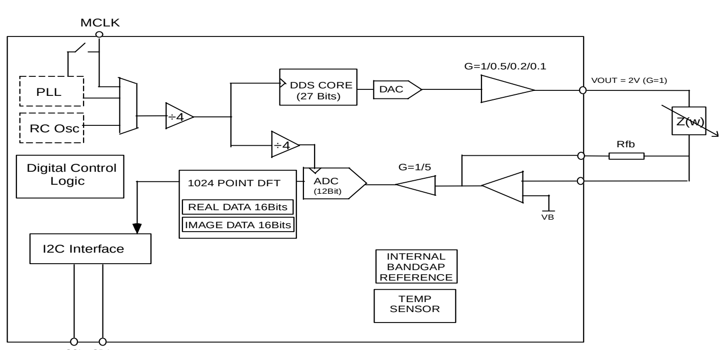
The system allows the user to program a 2V PK-PK sinusoidal signal as excitation to an external load. Output ranges of 1V, 500mV, 200mV can also be programmed. The signal is provided on chip using DDS techniques. Frequency resolution of 27 bits (less than 0.1HZ) can be achieved. The clock for the DDS can be generated from an external reference clock, an internal RC oscillator or an internal PLL. The PLL has a gain stage of 512 and typically needs a reference clock of 32KHz on the MCLK pin.

To perform the frequency sweep, the user must first program the conditions required for the sweep; start frequency, delta frequency, step frequency, etc. A Start Command is then required to begin the sweep.

At each point on the sweep the ADC will take 1024 samples and calculate a Discrete Fourier Transform to provide the real and imaginary data for the waveform. The real and imaginary data is available to the user through the 12C interface.

To determine the impedance of the load at any one frequency point, Z(w), a measurement system comprised of a trans impedance amplifier, gain stage and ADC are used to record data. The gain stage for the response stage is 1 or 5.

The ADC is a low noise, high speed 1MSPS sampling ADC that operates from a 3V supply. Clocking for both the DDS and ADC signals is provided externally via the MCLK reference clock, which is provided externally from a crystal oscillator. The AD5933 is available in a 16 ld SSOP.



Rev. PrA

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REVISION HISTORY

12/04—Revision PrA—Preliminary Version

SPECIFICATIONS

V_{DD} = +3.0 V +/- 10%, T_{MIN} to T_{MAX} unless otherwise noted.

Table 1.

Parameter	B Version[1]			Unit	Test Conditions/Comments
	Min	Typ	Max		
System Specs:					
Impedance Range	.0001		20	M Ohm	
Total System Accuracy		1		%	
System ppm		TDB		ppm/oC	
MCLK Update Rate			16	MSPS	
Output Stage					
Frequency Specs					
Output Frequency Range	0		50KHz	Hz	Uni-Polar Sinusoidal Signal.
Frequency Resoltuion		27		Bits.	<0.1 Hz Resolution
MCLK					External Rerference Clock. Typically 16.667MHz.
Initial Frequency Accuracy		0.1		Hz	Output Exitation Accuracy. 0 -50KHz Range.
RC OSCILLATOR					Internal RC Oscillator.
Initial Frequency Accuracy		1.5		%	Output Excitation Accuracy. 0 -50KHz Range.
Calibrated Frequency Accuracy		0.1		Hz	0 -50KHz Range. 1 point Offset Calibration
Frequency Tempco		10		ppm/oC	Requires 2 point User Calibration.
Frequency Jitter		TDB			Jitter on VOUT Pin, 30KHz output.
PLL					
PLL Gain		512			
INPUT CLOCK RANGE		32		KHZ	
Frequency Jitter		TDB			Jitter on VOUT Pin, 30KHz output.
Output Voltage Specs					
AC Voltage Range		2.0		Volts	Pk-Pk Unipolar Voltage on Output.
Output Voltage Error		TBD		%	Voltage Error on Pk-Pk Output.
DC Bias		Vdd/2		Volts	DC bias of AC Signal
DC Bias Error		TBD		%	Tolerance of DC Bias
AC Voltage Range		1.0		Volts	Pk-Pk Unipolar Voltage on Output.
Output Voltage Error		TBD		%	Voltage Error on Pk-Pk Output.
DC Bias		Vdd/4		Volts	DC bias of AC Signal
DC Bias Error		±1		%	Tolerance of DC Bias
AC Voltage Range		0.4		Volts	Pk-Pk Unipolar Voltage on Output.
Output Voltage Error		TBD		%	Voltage Error on Pk-Pk Output.
DC Bias		Vdd/8		Volts	DC bias of AC Signal
DC Bias Error		TBD		%	Tolerance of DC Bias
AC Voltage Range		0.2		Volts	Pk-Pk Unipolar Voltage on Output.
Output Voltage Error		TBD		%	Voltage Error on Pk-Pk Output.
DC Bias		Vdd/16		Volts	DC bias of AC Signal
DC Bias Error		TBD		%	Tolerance of DC Bias
DC Output Impedance		120		Ohm	
Short Circuit Current		75		mA	At 3 Volts.
Short Circuit Current		100		mA	At 5 Volts.
AC Characteristics					
Signal to Noise Ratio		60		db	
Total Harmonic Distortion		-66		db	
Spurious free Dynamic Range					
Wideband		60		db	

Parameter	B Version[1] Min	Typ	Max	Unit	Test Conditions/Comments
Narrowband		80		db	
Clock Feedthrough		TBD		db	
System Response Stage					
Analog Input VIN					
Input Leakage Current		1		nA	To Pin VIN
Input Capacitance		0.5		pF	To Pin VIN
Input Impedance		100M		Ohm	To Pin VIN
ADC Accuracy					
Resolution		12			
Sampling Rate		1		MSPS	
Integral Nonlinearity		±1		LSB	No missing Codes
Differential Nonlinearity		±1		LSB	
Offset Error					
Gain Error					
TEMPERATURE SENSOR					
Accuracy		±1		oC	TA = -40 - 125 DEGREES
Resolution		0.03125		oC	
Temperature Conversion Time		TBD		uS	
LOGIC INPUTS					
Vih, Input High Voltage			2.2	VDD = 3v	
Vil, Input Low Voltage	0.8			VDD = 3V	
Input Current			±1	uA	
Input Capacitance			±3	pF	
POWER REQUIREMENTS					
Vdd			3.0	Volts	
IDD (Normal Mode)		15		mA	
IDD (Powerdown Mode)		TBD		uA	

[1] Temperature ranges are as follows: B Version: –40°C to +125°C, typical at 25°C.
[2] Guaranteed by design and characterization, not production tested.

TIMING CHARACTERISTICS

Table 2. I²C Serial Interface

Parameter[1]	Limit at T_{MIN}, T_{MAX}	Unit	Description
F_{SCL}	400	kHz max	SCL clock frequency
t_1	2.5	µs min	SCL cycle time
t_2	0.6	µs min	t_{HIGH}, SCL high time
t_3	1.3	µs min	t_{LOW}, SCL low time
t_4	0.6	µs min	$t_{HD, STA}$, start/repeated start condition hold time
t_5	100	ns min	$t_{SU, DAT}$, data setup time
t_6[2]	0.9	µs max	$t_{HD, DAT}$ data hold time
	0	µs min	$t_{HD, DAT}$ data hold time
t_7	0.6	µs min	$t_{SU, STA}$ setup time for repeated start
t_8	0.6	µs min	$t_{SU, STO}$ stop condition setup time
t_9	1.3	µs min	t_{BUF}, bus free time between a stop and a start condition
t_{10}	300	ns max	t_F, fall time of SDA when transmitting
	0	ns min	t_R, rise time of SCL and SDA when receiving (CMOS compatible)
t_{11}	300	ns max	t_F, fall time of SDA when transmitting
	0	ns min	t_F, fall time of SDA when receiving (CMOS compatible)
	300	ns max	t_F, fall time of SCL and SDA when receiving
	20 + 0.1 C_B	ns min	t_F, fall time of SCL and SDA when transmitting
C_B[3]	400	pF max	Capacitive load for each bus line

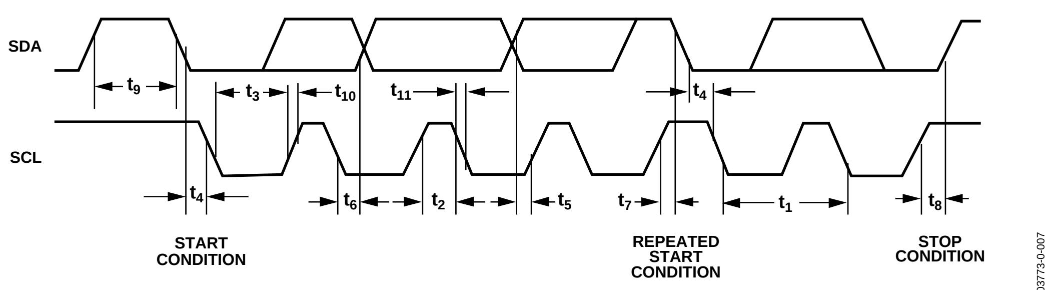

Figure 1. I²C Interface Timing Diagram

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

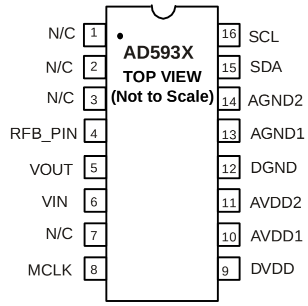

Table 3.

Mnemonic	Function
N/C	No Connect.
RFB_PIN	External Feedback Resistor. This is used to set the gain of the input signal of the VIN node.
VOUT	Output AC Excitation signal. Programmble Frequnency range 0-50KHz.
VIN	Input Signal to transimpedance amplifier. External Feedback resistor will control gain of transimpedance amplifier.
MCLK	Master Clock for the system. Used to provide output excitation signal and as sampling of ADC.
DVDD	Digital Supply Voltage
AVDD1	Analog Supply Voltage 1
AVDD2	Analog Supply Voltage 2
DGND	Digital Ground
AGND1	Analog Gnd 1
AGND2	Analog Gnd 2
SDA	I2C DATA INPUT
SCL	I2C CLOCK INPUT.

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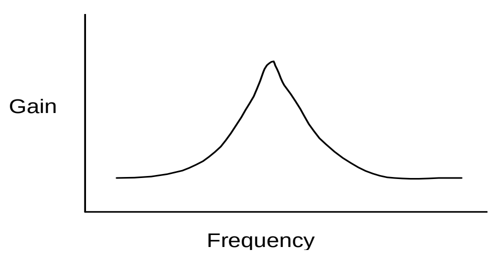

Figure 2.

The system allows the user to program a 2V PK-PK sinusoidal signal as excitation to an external load. Output ranges of 1V, 500mV, 200mV can also be programmed. The signal is provided on chip using DDS techniques. Frequency resolution of 27 bits (less than 0.1HZ) can be achieved. The clock for the DDS can be generated from an external reference clock, an internal RC oscillator or an internal PLL. The PLL has a gain stage of 520 and typically needs a reference clock of 32KHz on the MCLK pin.

OUTPUT STAGE

The output stage of the AD5933, shown in diagram below, provides a constant output frequency or frequency sweep function which has a programmable output voltage of 2/1/0.5/0.2V. The frequency sweep sequence is pre-progammed through the I2C interface. An I2C command is used to start the excitation sequence.

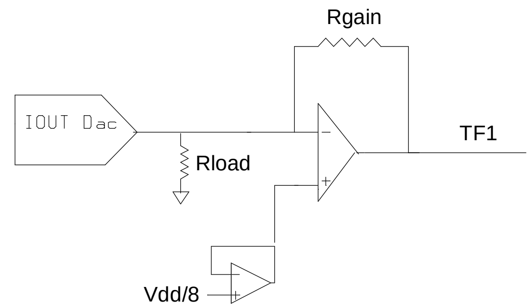

Figure 3.

CIRCUIT DESCRIPTION

The AD5933 has a fully integrated Direct Digital Synthesis (DDS) core to generate required frequencies. The block requires a reference clock to provide digitally created sine waves up to 50KHz. This is provided through an external reference clock, MCLK. This clock is internally divided down by 4 to provide the reference clock or fMCLK to the DDS.

The internal circuitry of the DDS consists of the following main sections: a Numerical Controlled Oscillator (NCO), a Frequency Modulator, SIN ROM and a Digital-to-Analog Converter.

NUMERICAL CONTROLLED OSCILLATOR + PHASE MODULATOR

The main component of the NCO is a 27-bit phase accumulator which assembles the phase component of the output signal.

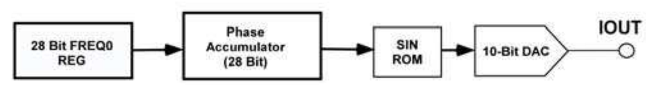

Figure 4

Continuous time signals have a phase range of 0 to 2pi. Outside this range of numbers, the sinusoid functions repeat themselves in a periodic manner. The digital implementation is no different. The accumulator simply scales the range of phase numbers into a multi-bit digital word. The phase accumulator in the DDS is implemented with 28 bits. Therefore, 2pi = 227. Likewise, the DPhase term is scaled into this range of numbers 0 < DPhase < 227 – 1. Making these substitutions into the equation above

$$f = \text{DPhase} \times \text{fMCLK}/227$$

where 0 < DPhase < 227 - 1.

(Note. fmclk = MCLK/4)

The input to the phase accumulator (i.e., the phase step) is selected from the frequency register. NCOs inherently generate continuous phase signals, thus avoiding any output discontinuity when switching between frequencies.

SIN ROM

To make the output from the NCO useful, it must be converted from phase information into a sinusoidal value. Since phase information maps directly into amplitude, the SIN ROM uses the digital phase information as an address to a look-up table, and converts the phase information into amplitude. Although the NCO contains a 27-bit phase accumulator, the output of the NCO is truncated to 12 bits. Using the full resolution of the phase accumulator is impractical and unnecessary as this would require a look-up table of 227 entries. It is necessary only to have sufficient phase resolution such that the errors due to truncation are smaller than the resolution of the 10-bitDAC. This requires the SIN ROM to have two bits of phase resolution more than the 10-bit DAC. The DDS includes a high impedance current source 10-bit DAC.

RESPONSE STAGE

The diagram below shows the input stage to pin TF1. Current from the external sensor load flows through the TF1 pin and into a transimpedance amplifier which has an external resistor across its feedback. The user needs to choose a precision resistor in the feedback loop such that the dynamic range of the ADC is used. The positive node of the transimpedance amplifier is biased to VDD/2. The output of the Transimpedance amplifier can then be gained by either 1 or 5, and is fed directly into the input of the ADC.

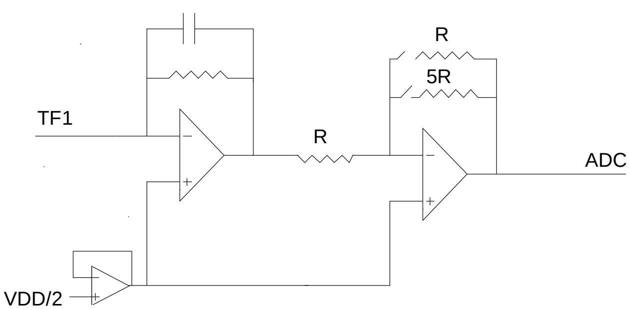

Figure 5.

ADC OPERATION

The AD5933 has an integrated on board 12 bit ADC. The ADC contains an on-chip track and hold amplifier, a successive approximation A/D converter. Clocking for the A/D is provided using a divided down ratio of the reference clock.

The A/D is a successive approximation analog to digital converter, based on a Capacitive DAC design Architecture. The figures below show simplified schematics of the ADC. The ADC is comprised of control logic, a SAR, and a capacitive DAC, all of which are used to add and subtract fixed amounts of charge from the Sampling capacitor to bring the comparator back into a balanced condition. The 1st figure shows the ADC during its acquisition phase. SW2 is closed and SW1 is in position A, the comparator is held in a balanced condition, and the sampling capacitor acquires the signal on VA1, for example.

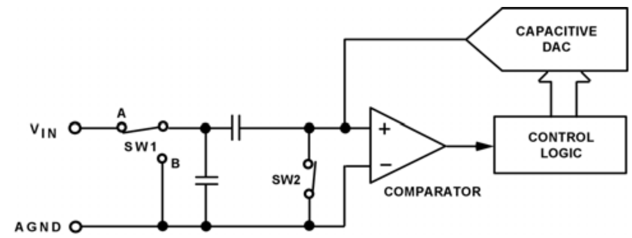

Figure 6.

When the ADC starts a conversion, SW2 will open and SW1 will move to position B, as shown below, causing the comparator to become unbalanced. The control logic and the capacitive DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is re-balanced, the conversion is complete. The control logic generates the ADC output code.

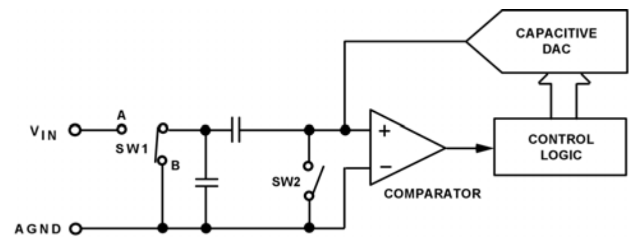

Figure 7.

The start conversion for the ADC is either user controlled via an external adc_trig pin or can be internally programmed as a delay from the start of the exitation signal. The data from the ADC is directly available on the I2C interface or can either be stored in a FIFO RAM until the entire frequency sweep is completed.

DFT CONVERSION

A discrete Fourier transform is calculated for each frequency point in the sweep. The return signal is converted by the ADC, windowed and then multiplied with a test phasor value to give a real and imaginary output. This is repeated for 1024 sample points of the input signal and the results of each multiplication summed to give a final answer as a complex number. The resultant answer at each frequency is two 16 bit words, the real and imaginary data in complex form.

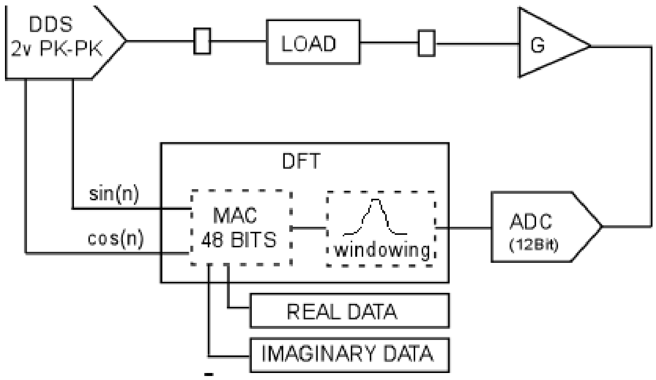

Figure 8.

The DFT algorithm is represented by

$$X(f) = SUM\ x(n)[Cos(n)-jSine(n)]$$

Both the real and Imaginary data register have 15 bits of data and one sign bit. The 15 bits of data are in 2's compliment format. The magnitude of the signal can be represented by

$$Magnitude = \sqrt{R^2 + I^2}$$

This magnitude that's returned is a scaled valued of the actual complex impedance measured. The multiplication factor between the magnitude returned and the actual impedance is called the GAIN FACTOR. The user needs to then calculate this GAIN FACTOR value and use it for calibration in the system.

TEMPERATURE SENSOR

The temperature sensor is a 13-bit digital temperature sensor with a 14th bit that acts as a sign bit. The block houses an on-chip temperature sensor, a 13-bit A/D converter and a reference circuit. The A/D converter section consists of a conventional successive-approximation converter based around a capacitor DAC.

The on-chip temperature sensor allows an accurate measurement of the ambient device temperature to be made. The specified measurement range of the sensor is −40°C to +150°C. At +150°C. The structural integrity of the device starts to deteriorate when operated at voltage and temperature maximum specifications.

Temperature Conversion Details

The conversion clock for the part is internally generated; no external clock is required except when reading from and writing to the serial port. In normal mode, an internal clock oscillator runs an automatic conversion sequence. During this automatic conversion sequence, a conversion is initiated every 1 second. At this time, the part powers up its analog circuitry and performs a temperature conversion. This temperature conversion typically takes 800 μs, after which time the analog circuitry of the part automatically shuts down. The analog circuitry powers up again when the 1 second timer times out and the next conversion begins. The result of the most recent temperature conversion is always available in the serial output register because the serial interface circuitry never shuts down.

The temperature sensor block will default to a power-down state. To perform a temperature measurement a command is written to the control register. After the temperature operation is complete, the block automatically powers down until the next temperature command is issued.

In normal conversion mode, the internal clock oscillator is reset after every read or write operation. This causes the device to start a temperature conversion, the result of which is typically available 800 μs later. Similarly, when the part is taken out of shutdown mode, the internal clock oscillator is started and a conversion is initiated. The conversion result is available 800 μs later, typically. Reading from the device before a conversion is complete causes the block to stop converting; the part starts again when serial communication is finished.

Temperature Value Register

The temperature value register is a 16-bit read-only register that stores the temperature reading from the ADC in 13-bit twos complement format plus a sign bit. The two MSB bits are don't cares. DB13 is the sign bit. The ADC can theoretically measure a 255°C temperature span. The internal temperature sensor is guaranteed to a low value limit of −40°C and a high limit of +150°C.

Table 4. Temperature Data Format

Temperature	Digital Output DB13…DB0
−40°C	11, 1011 0000 0000
−30°C	11, 1100 0100 0000
−25°C	11, 1100 1110 0000
−10°C	11, 1110 1100 0000
−0.03125°C	11, 1111 1111 1111
0°C	00, 0000 0000 0000
+0.03125°C	00, 0000 0000 0001
+10°C	00, 0001 0100 0000
+25°C	00, 0011 0010 0000
+50°C	00, 0110 0100 0000
+75°C	00, 1001 0110 0000
+100°C	00, 1100 1000 0000
+125°C	00, 1111 1010 0000
+150°C	01, 0010 1100 0000

Temperature Conversion Formula

1. Positive Temperature = ADC Code(d)/32

2. Negative Temperature = (ADC Code*(d) – 16384)/32

   *Using all 14 bits of the data byte, includes the sign bit.

   Negative Temperature = (ADC Code(d)* – 8192)/32

   *DB13 (sign bit) is removed from the ADC code

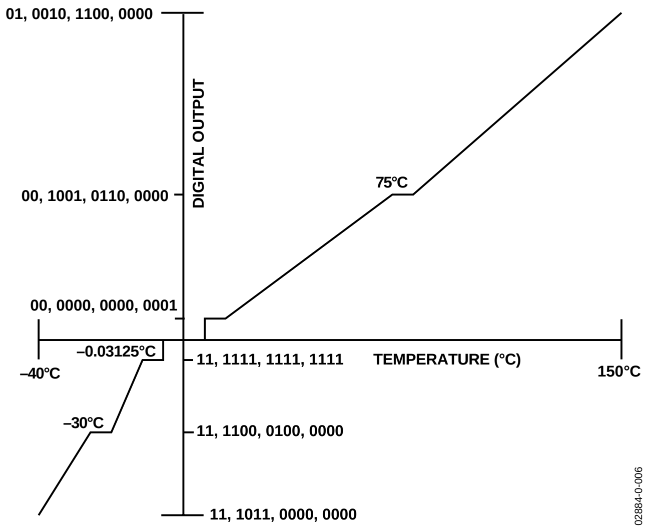

Figure 9. Temperature to Digital Transfer Function

REGISTER MAP (EACH ROW EQUALS 8 BITS OF DATA)

Table 5.

Register Name	Reg Add.	Register Data [8Bits]	Read/Write Register	Register Type
RAM				
Control Register	80h	D15-D8	Read/Write	RAM
	81h	D7-D0	Read/Write	RAM
Start Frequency (24 Bits)	82h	D23-D16	Read/Write	RAM
	83h	D15-D8	Read/Write	RAM
	84h	D7-D0	Read/Write	RAM
Frequency Increment Word	85h	D23-D16	Read/Write	RAM
	86h	D15-D8	Read/Write	RAM
	87h	D7-D0	Read/Write	RAM
No of Increments (9 Bits) Bits D15-D9 = Don't care Bits D8-D0= number of frequency increments.	88h	D15-D8	Read/Write	RAM
	89h	D7-D0	Read/Write	RAM
Settling time Cycles (16 Bits) D15 – D11= Don't care D10 –D9 = 2 bit decode D8-D0 = number of cycles D10 D9 0 Default 0 1 number of cycles x2 1 0 reserved 1 1 number of cycles x4	8Ah	D15-D8	Read/Write	RAM
	8Bh	D7-D0	Read/Write	RAM
Leakage limit for test A D7 – D4 = Don't care D3 – D0 = 4 Bit Limit	8Ch	D7-D0	Read/Write	RAM
Leakage limit for test B D7 – D4 = Don't care D3 – D0 = 4 Bit Limit	8Dh	D7-D0	Read/Write	RAM
Leakage limit for test C D7 – D4 = Don't care D3 – D0 = 4 Bit Limit	8Eh	D7-D0	Read/Write	RAM
Status Register	8fh	D7-D0	Read/Write	RAM
Index Counter of Frequency (9 Bits) Bits D15 –D9 = Don't care Bits D8- D0 = Increments register after a frequency increment command. Set to zero at initial frequency.	90h	D15-D8	Read Only	RAM
	91h	D7-D0	Read Only	
Temperature Data Register	92h	D15-D8	Read Only	RAM
	93h	D7-D0	Read Only	RAM

Register Name	Reg Add.	Register Data [8Bits]	Read/Write Register	Register Type
Real Data	94h	D15-D8	Read Only	RAM
	95h	D7-D0	Read Only	RAM
Imaginary Data	96h	D15-D8	Read Only	RAM
	97h	D7-D0	Read Only	RAM
Checksum	98h	D7-D0	Read Only	RAM

CONTROL REGISTER

The AD5933 contains a 16 bit control register (address 80h and 81h) that set the AD5933 control modes. The five MSB's of the control register are decoded to provide control functions for frequency sweep, power down and various other control functions, defined in Table below. The other command functions of the control register are explained on the following pages.

Note: For error checking on the control register it is advised to write one byte at a time with PEC enabled. This allows full error checking to be completed before the control register is updated and therefore ensures the control is not updated with incorrect data. The Control register will power-up in the following state xA000h (i.e. in Power-down)

Table 6. Control Register Map

Bit						
D15	D15	D14	D13	D12	D11	FREQUENCY SWEEP
D14	0	0	0	0	0	No Operation/ Exit Fuse Blow Mode
D13	0	0	0	0	1	Initialize Sensor with Start Frequency
D12	0	0	0	1	0	Start Frequency Sweep
D11	0	0	0	1	1	Increment Frequency
	0	0	1	0	0	Repeat Frequency
	0	1	0	0	0	Reserved.
	0	1	0	0	1	Measure Temperature
	0	1	0	1	0	Power Down
	0	1	0	1	1	Standby Mode
D10						External Calibration Mode = "1"
D9			D9	D8		Output Voltage
D8			0	0		No Divide. (Normal Mode = 2.0V)
			0	1		Divide by 10 (200mv)
			1	0		Divide by 5 (400mv)
			1	1		Divide by 2 (1.0v)
D7						Post Gain "0" = Multiply X 5; "1" = Multiply X 1.
D6						Error Checking Enable = "1"; Disable="0"
D5						Reserved. Set to "0"
D4						RESET
D3			D3	D2		System Clock
D2			0	0		Internal Oscillator
			0	1		Reserved.
			1	0		External Oscillator
			1	1		PLL
D1			0			RESERVED
D0			0			RESERVED

CONTROL REGISTER DECODE:

INITIALIZE SENSOR WITH START FREQUENCY

This command enables the DDS to output the start frequency for an indefinite time. It is used is to excite the sensor initially. When the output load (sensor) has settled after a time determined by the user, the user must initiate a "start frequency sweep" command to begin the frequency sweep.

START FREQUENCY SWEEP

This command start the frequency sweep routine. When the AD11/2043 receives this command, it starts counting a delay cycle that will gate the ADC conversion pulse. This delay cycle has already been pre-programmed as number of output cycles by the user.

INCREMENT FREQUENCY

The "Increment Frequency" command is used to step to the next frequency point in the sweep. This usually happens after data from the previous step has been transferred and verified by the DSP.

REPEAT FREQUENCY

Repeat frequency allows the user to repeat any given frequency if the data gets corrupted or the measurement sequence doesn't complete.

POWER DOWN

Power Down powers down all the blocks in the chip except the interface. All amplifiers and the oscillator will be powered off. The default on power-up of the AD11/2043 is power-down and the control register will contain the code 1010000000000000. In this mode both the output and input pins DDS_OUT and IN_ADC will be tied to GND.

STANDBY MODE

Powers the part up for general operation; all the amplifiers will be powered up but their outputs will be tied to GND. The internal oscillator will also be powered up and running.

READ TEMPERATURE

This initiates a temperature reading from the part. The part does not need to be in Power Up mode to perform a temperature reading. The block will power itself up, take the reading and then power down again.

ERROR CHECKING

Set bit in Control Register to enable this. Enable = "1"; Disable="0"

RESET

A Reset will Refresh all Memory, Reset ADC, Frequency reverts to the INITIAL start frequency

SYSTEM CLOCK

Allows the user to configure either the internal oscillator, an external reference clock or to allow an internal PLL to provide a clock for the system. In PLL mode the user will have to provide a stable ~32khz clock as reference to the PLL.

OUTPUT VOLTAGE

This allows the user to change the excitation voltage levels. There are for output ranges, 2v, 1v, 500mv, 200mv.

POST GAIN

Allows the user to multiply pre-amp the response signal by a multiplication factor of 5 into the ADC if required.

Performing a Frequency Sweep – Flow Chart

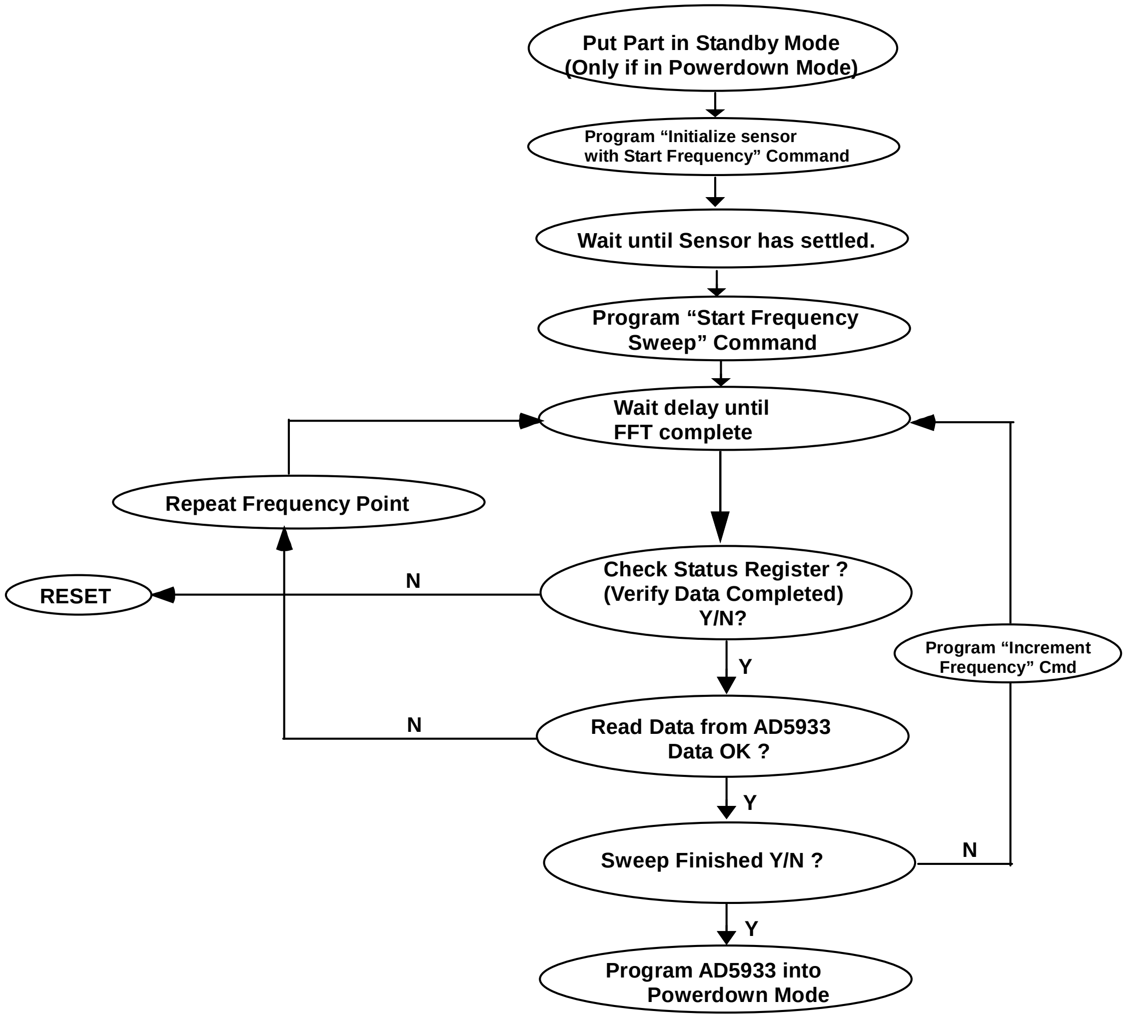

Figure 10.

SERIAL BUS INTERFACE

Control of the AD5933 is carried out via the 1^{2}C Serial Interface Protocol. The AD5933 is connected to this bus as a slave device, under the control of a master device.

The AD5933 has a 7-bit serial bus slave address. When the device is powered up, it will do so with a default serial bus address; 0001101

GENERAL I^{2}C TIMING

The diagram below shows the timing diagram for general read and write operations using the I^{2}C interface. The general I2C protocol operates as follows:

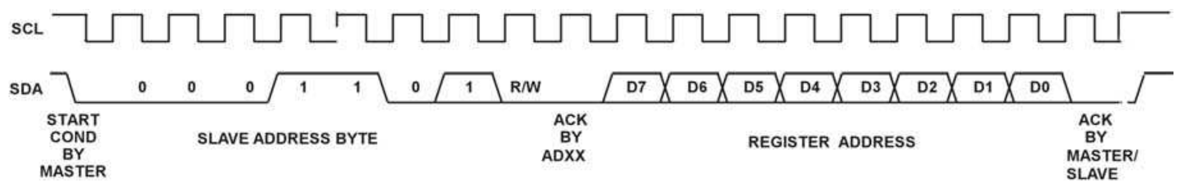

Figure 11.

1. The master initiates data transfer by establishing a START condition, defined as a high to low transition on the serial data line SDA while the serial clock line SCL remains high. This indicates that a data stream will follow. The slave responds to the START condition and shift in the next 8 bits, consisting of a 7-bit slave address (MSB first) plus an R/W bit, which determines the direction of the data transfer, i.e. whether data will be written to or read from the slave device (0 = write, 1 = read).

The slave responds by pulling the data line low during the low period before the ninth clock pulse, known as the acknowledge bit, and holding it low during the high period of this clock pulse. All other devices on the bus now remain idle while the selected device waits for data to be read from or written to it. If the R/W bit is a 0, then the master will write to the slave device. If the R/W bit is a 1, the master will read from the slave device.

2. Data is sent over the serial bus in sequences of nine clock pulses, 8 bits of data followed by an acknowledge bit, which can be from the master or slave device. Data transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, as a low to high transition when the clock is high may be interpreted as a STOP signal. If the operation is a write operation, the first data byte after the slave address is a command byte. This tells the slave device what to expect next. It may be an instruction telling the slave device to expect a block write, or it may simply be a register address that tells the slave where subsequent data is to be written. Since data can flow in only one direction as defined by the R/W bit, it is not possible to send a command to a slave device during a read operation. Before doing a read operation, it may first be necessary to do a write operation to tell the slave what sort of read operation to expect and/or the address from which data is to be read.

3. When all data bytes have been read or written, stop conditions are established. In WRITE mode, the master will pull the data line high during the 10th clock pulse to assert a STOP condition. In READ mode, the master device will release the SDA line during the low period before the 9th clock pulse, but the slave device will not pull it low. This is known as No Acknowledge. The master will then take the data line low during the low period before the 10th clock pulse, then high during the 10th clock pulse to assert a STOP condition.

WRITING/READING TO THE AD5933

The interface specification defines several different protocols for different types of read and write operations. The ones used in the AD5933 are discussed below. The following abbreviations are used:

S	-	Start
P	-	Stop
R	-	Read
W	-	Write
A	-	Acknowledge
	-	No Acknowledge

Write Byte/Command Byte

In this operation the master device sends a byte of data to the slave device. The write byte can either be a data byte write to a RAM location or can be a command operation.

To write data to a register the command sequence is as follows:

1. The master device asserts a start condition on SDA.

2. The master sends the 7-bit slave address followed by the write bit (low).

3. The addressed slave device asserts ACK on SDA.

4. The master sends a register address.

5. The slave asserts ACK on SDA.

6. The master sends a data byte.

7. The slave asserts ACK on SDA.

8. The master asserts a STOP condition on SDA to end the transaction.

S	SLAVE ADDRESS	W	A	REGISTER ADDRESS	A	REGISTER DATA	A	P

Figure 12. Writing Register Data to Register Address

In the AD5933, the write byte protocol is also used to set a pointer to a register location. This is used for a subsequent single byte read from the same address or block read or write starting at that address. This is done as follows:

To set a register pointer the following sequence is applied:

1. The master device asserts a start condition on SDA.

2. The master sends the 7-bit slave address followed by the write bit (low).

3. The addressed slave device asserts ACK on SDA.

4. The master sends a command code (pointer command 1011 0000).

5. The slave asserts ACK on SDA.

6. The master sends a data byte (register location pointer is to point to).

7. The slave asserts ACK on SDA.

8. The master asserts a STOP condition on SDA to end the transaction.

S	SLAVE ADDRESS	W	A	Pointer Command 1011 0000	A	Register Location to point to	A	P

Figure 13. Setting Pointer to Register Address

BLOCK WRITE

In this operation, the master device writes a block of data to a slave device. The start address for a block write must previously have been set. In the case of the AD5933 this is done by setting a pointer to set the RAM/OTP address.

1. The master device asserts a start condition on SDA.

2. The master sends the 7-bit slave address followed by the write bit (low).

3. The addressed slave device asserts ACK on SDA.

4 The master sends An 8 bit command code (10100000) that tells the slave device to expect a block write.

5. The slave asserts ACK on SDA.

6. The master sends a data byte that tells the slave device the number of data bytes will be sent to it.

7. The slave asserts ACK on SDA.

8. The master sends the data bytes.

9. The slave asserts ACK on SDA after each data byte.

10. The master asserts a STOP condition on SDA to end the transaction.

S	SLAVE ADDRESS	W	A	BLOCK WRITE	A	NUMBER BYTES WRITE	A	BYTE0	A	BYTE1	A	BYTE2	A	P

Figure 14. Writing a block write

AD5933 READ OPERATIONS

The AD5933 uses the following I2C read protocols:

Receive Byte

In this operation, the master device receives a single byte from a slave device as follows:

1. The master device asserts a START condition on SDA.

2. The master sends the 7-bit slave address followed by the read bit (high).

3. The addressed slave device asserts ACK on SDA.

4. The master receives a data byte.

5. The master asserts NO ACK on SDA. (Slave needs to check that master has received Data)

6. The master asserts a STOP condition on SDA and the transaction ends.

In the AD5933, the receive byte protocol is used to read a single byte of data from a RAM or OTP memory location whose address has previously been setting the address pointer.

Figure 15. Reading Register Data

Block Read

In this operation, the master device reads a block of data from a slave device. The start address for a block read must previously have been set. This is again done by setting a pointer to set the RAM/OTP address.

1. The master device asserts a START condition on SDA.

2. The master sends the 7-bit slave address followed by the write bit (low).

3. The addressed slave device asserts ACK on SDA.

4. The master sends a command code (10100001) that tells the slave device to expect a block read.

5. The slave asserts ACK on SDA.

6. The master sends a byte count data byte that tells the slave how many data bytes to expect.

7. The master asserts ACK on SDA.

8 . The master asserts a repeat start condition on SDA. (This is required to set Read bit high)

9. The master sends the 7-bit slave address followed by the read bit (high).

10. The slave asserts ACK on SDA.

11. The master receives the data bytes.

12. The master asserts ACK on SDA after each data byte.

14. A NACK is generated after the last byte to signal the end of the read.

15. The master asserts a STOP condition on SDA to end the transaction.

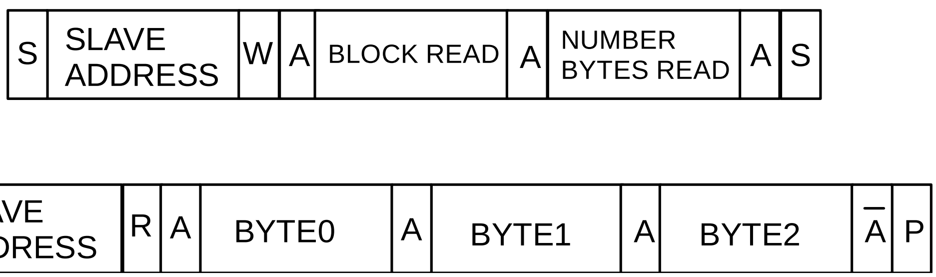

Figure 16. Performing a block read

ERROR CORRECTION

P.E.C.

The AD5933 provides the option of issuing a PEC (Packet Error Correction) byte after all commands. This enables the user to verify that the data received by or sent from the AD5933 is correct. The PEC byte is an optional byte sent after that last data byte has been written to or read from the AD5933. The protocol is as follows:

1. The AD5933 issues a PEC byte to the master. The master should check the PEC byte and issue another block read if the PEC byte is incorrect.

2. A NACK is generated after the PEC byte to signal the end of the read.

3. The PEC is generated per the following specifications.

Note: The PEC byte is calculated using CRC-8. The Frame Check Sequence (FCS) conforms to CRC-8 by the polynomial:

$$C(x) = x^8 + x^2 + x^1 + 1$$

CHECKSUM

A checksum register is available to allow the user to verify the correct contents of the frequency register, frequency increment register, and number of increments. The checksum register is based on a error checking algorithm from the above registers. TBD. The user reads this checksum register and verifies contents are correct.

USER COMMAND CODES

These command codes are used for reading/writing to the interface and the memory. They are further explained in the appropriate sections but are grouped here for ease of reference.

Table 7.

Command Code	Code Name	Code Description.
1010 0000	Block Write	This command is used when writing multiple bytes to the RAM. See block write section for further explanations.
1010 0001	Block Read	This command is used when reading multiple bytes from the RAM/Memory. See block write section for further explanations.
1011 0000	Address Pointer	This command enables the user to set the address pointer to any location in the memory. The data will contain the address register of the register the pointer should be pointing to.

OUTLINE DIMENSIONS

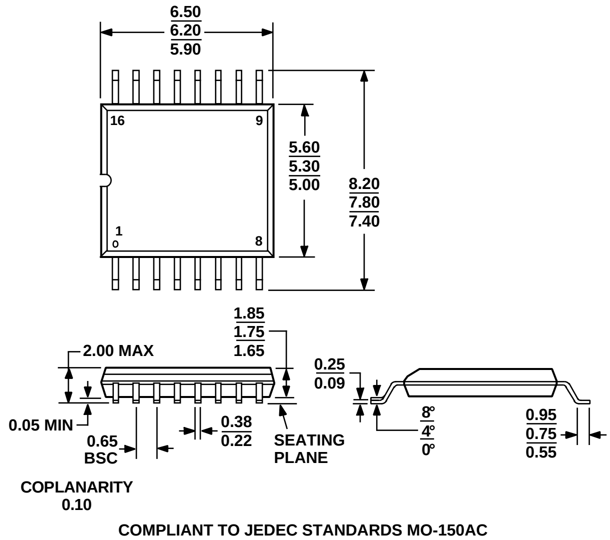

Figure 17 16-Lead Shrink Small Outline Package [SSOP]
(RS-16)
Dimensions shown in millimeters

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PR05324-0-12/04(PrA)

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