256-Position SPI Compatible Digital Potentiometer

AD5160

FEATURES

256-position
End-to-end resistance 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ
Compact SOT-23-8 (2.9 mm × 3 mm) package
SPI compatible interface
Power-on preset to midscale
Single supply 2.7 V to 5.5 V
Low temperature coefficient 45 ppm/°C
Low power, I_{DD} = 8 µA
Wide operating temperature –40°C to +125°C
Evaluation board available

APPLICATIONS

Mechanical potentiometer replacement in new designs
Transducer adjustment of pressure, temperature, position, chemical, and optical sensors
RF amplifier biasing
Automotive electronics adjustment
Gain control and offset adjustment

GENERAL OVERVIEW

The AD5160 provides a compact 2.9 mm × 3 mm packaged solution for 256-position adjustment applications. These devices perform the same electronic adjustment function as mechanical potentiometers or variable resistors, with enhanced resolution, solid-state reliability, and superior low temperature coefficient performance.

The wiper settings are controllable through an SPI compatible digital interface. The resistance between the wiper and either end point of the fixed resistor varies linearly with respect to the digital code transferred into the RDAC latch.

Operating from a 2.7 V to 5.5 V power supply and consuming less than 5 µA allows for usage in portable battery-operated applications.

FUNCTIONAL BLOCK DIAGRAM

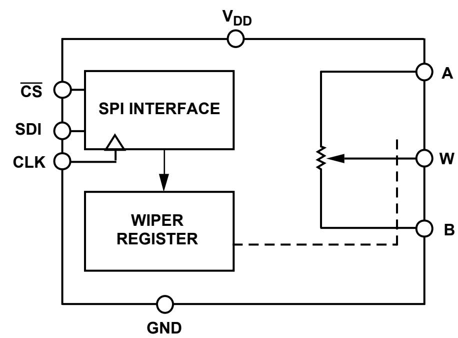

Figure 1.

PIN CONFIGURATION

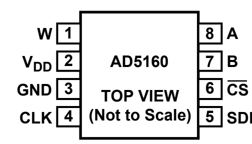

Figure 2.

Note:
The terms *digital potentiometer*, *VR*, and *RDAC* are used interchangeably.

Rev. 0

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REVISION HISTORY

Revision 0: Initial Version

ELECTRICAL CHARACTERISTICS—5 kΩ VERSION

(V_{DD} = 5 V ± 10%, or 3 V ± 10%; V_A = +V_{DD}; V_B = 0 V; –40°C < T_A < +125°C; unless otherwise noted.)

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect	–1.5	±0.1	+1.5	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	–4	±0.75	+4	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = 25°C	–30		+30	%
Resistance Temperature Coefficient	$\Delta R_{AB}/\Delta T$	V_{AB} = V_{DD}, Wiper = no connect		45		ppm/°C
Wiper Resistance	R_W			50	120	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (Specifications apply to all VRs)						
Resolution	N				8	Bits
Differential Nonlinearity[4]	DNL		–1.5	±0.1	+1.5	LSB
Integral Nonlinearity[4]	INL		–1.5	±0.6	+1.5	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 0x80		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0xFF	–6	–2.5	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	+2	+6	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A,B,W}$		GND		V_{DD}	V
Capacitance[6] A, B	$C_{A,B}$	f = 1 MHz, measured to GND, Code = 0x80		45		pF
Capacitance[6] W	C_W	f = 1 MHz, measured to GND, Code = 0x80		60		pF
Shutdown Supply Current[7]	I_{DD_SD}	V_{DD} = 5.5 V		0.01	1	µA
Common-Mode Leakage	I_{CM}	V_A = V_B = V_{DD}/2		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}		2.4			V
Input Logic Low	V_{IL}				0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		3	8	µA
Power Dissipation[8]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			0.2	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = +5 V ± 10%, Code = Midscale		±0.02	±0.05	%/%
DYNAMIC CHARACTERISTICS[6, 9]						
Bandwidth –3dB	BW_5K	R_{AB} = 5 kΩ, Code = 0x80		1.2		MHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz		0.05		%
V_W Settling Time	t_S	V_A= 5 V, V_B = 0 V, ±1 LSB error band		1		µs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 2.5 kΩ, RS = 0		6		nV/√Hz

ELECTRICAL CHARACTERISTICS—10 kΩ, 50 kΩ, 100 kΩ VERSIONS

(V_{DD} = 5 V ± 10%, or 3 V ± 10%; V_A = V_{DD}; V_B = 0 V; −40°C < T_A < +125°C; unless otherwise noted.)

Table 2.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS—RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = no connect	−1	±0.1	+1	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = no connect	−2	±0.25	+2	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = 25°C	−30		+30	%
Resistance Temperature Coefficient	$\Delta R_{AB}/\Delta T$	V_{AB} = V_{DD}, Wiper = no connect		45		ppm/°C
Wiper Resistance	R_W	V_{DD} = 5 V		50	120	Ω
DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE (Specifications apply to all VRs)						
Resolution	N				8	Bits
Differential Nonlinearity[4]	DNL		−1	±0.1	+1	LSB
Integral Nonlinearity[4]	INL		−1	±0.3	+1	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 0x80		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = 0xFF	−3	−1	0	LSB
Zero-Scale Error	V_{WZSE}	Code = 0x00	0	1	3	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A,B,W}$		GND		V_{DD}	V
Capacitance[6] A, B	$C_{A,B}$	f = 1 MHz, measured to GND, Code = 0x80		45		pF
Capacitance[6] W	C_W	f = 1 MHz, measured to GND, Code = 0x80		60		pF
Shutdown Supply Current[7]	I_{DD_SD}	V_{DD} = 5.5 V		0.01	1	μA
Common-Mode Leakage	I_{CM}	V_A = V_B = $V_{DD}/2$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}		2.4			V
Input Logic Low	V_{IL}				0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V			0.6	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±1	μA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	$V_{DD\ RANGE}$		2.7		5.5	V
Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V		3	8	μA
Power Dissipation[8]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			0.2	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = +5 V ± 10%, Code = Midscale		±0.02	±0.05	%/%
DYNAMIC CHARACTERISTICS[6, 9]						
Bandwidth −3dB	BW	R_{AB} = 10 kΩ/50 kΩ/100 kΩ, Code = 0x80		600/100/40		kHz
Total Harmonic Distortion	THD_W	V_A =1 V rms, V_B = 0 V, f = 1 kHz, R_{AB} = 10 kΩ		0.05		%
V_W Settling Time (10 kΩ/50 kΩ/100 kΩ)	t_S	V_A = 5 V, V_B = 0 V, ±1 LSB error band		2		μs
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 5 kΩ, RS = 0		9		nV/√Hz

TIMING CHARACTERISTICS—5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ VERSIONS

(V_{DD} = +5V ± 10%, or +3V ± 10%; V_A = V_{DD}; V_B = 0 V; –40°C < T_A < +125°C; unless otherwise noted.)

Table 3.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
SPI INTERFACE TIMING CHARACTERISTICS[6, 10] (Specifications Apply to All Parts)						
Clock Frequency	f_{CLK}				25	MHz
Input Clock Pulsewidth	t_{CH}, t_{CL}	Clock level high or low	20			ns
Data Setup Time	t_{DS}		5			ns
Data Hold Time	t_{DH}		5			ns
$\overline{CS}$ Setup Time	t_{CSS}		15			ns
$\overline{CS}$ High Pulsewidth	t_{CSW}		40			ns
CLK Fall to $\overline{CS}$ Fall Hold Time	t_{CSH0}		0			ns
CLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH1}		0			ns
$\overline{CS}$ Rise to Clock Rise Setup	t_{CS1}		10			ns

NOTES
[1] Typical specifications represent average readings at +25°C and V_{DD} = 5 V.
[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.
[3] V_{AB} = V_{DD}, Wiper (V_W) = no connect.
[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. VA = V_{DD} and V_B = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
[5] Resistor terminals A, B, W have no limitations on polarity with respect to each other.
[6] Guaranteed by design and not subject to production test.
[7] Measured at the A terminal. The A terminal is open circuited in shutdown mode.
[8] P_{DISS} is calculated from (I_{DD} × V_{DD}). CMOS logic level inputs result in minimum power dissipation.
[9] All dynamic characteristics use V_{DD} = 5 V.
[10] See timing diagram for location of measured values. All input control voltages are specified with t_R = t_F = 2 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C, unless otherwise noted.)

Table 4.

Parameter	Value
V_{DD} to GND	–0.3 V to +7 V
V_A, V_B, V_W to GND	V_{DD}
I_{MAX}[1]	±20 mA
Digital Inputs and Output Voltage to GND	0 V to +7 V
Operating Temperature Range	–40°C to +125°C
Maximum Junction Temperature (T_{JMAX})	150°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Thermal Resistance[2] θ_{JA}: MSOP-10	230°C/W

NOTES
[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.
[2] Package power dissipation = (T_{JMAX} – T_A)/θ_{JA}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS

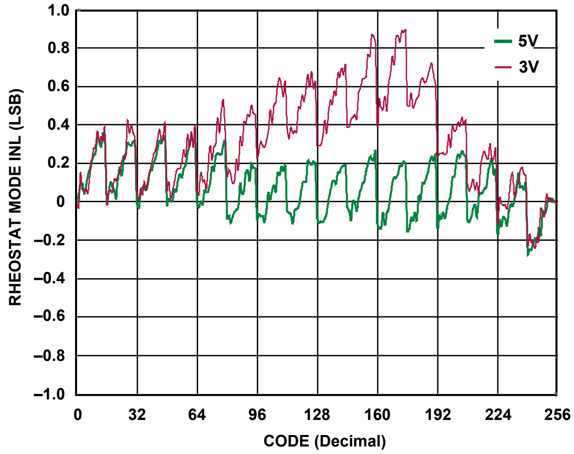

Figure 3. R-INL vs. Code vs. Supply Voltages

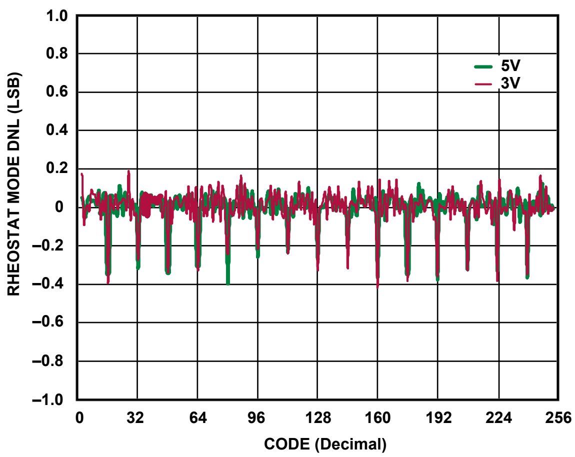

Figure 4. R-DNL vs. Code vs. Supply Voltages

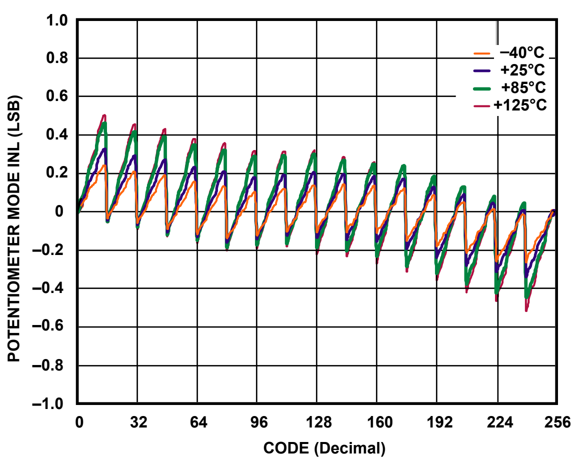

Figure 5. INL vs. Code, V_{DD} = 5 V

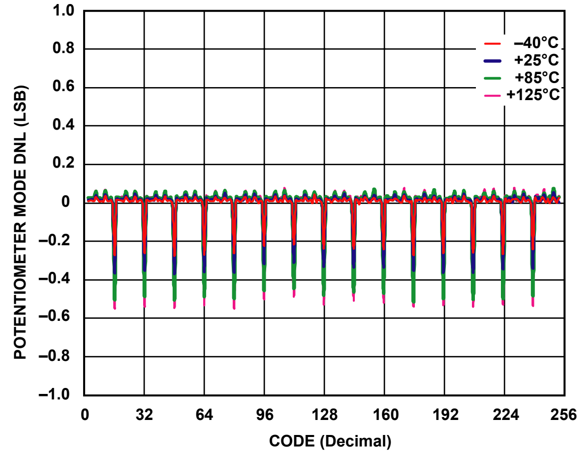

Figure 6. DNL vs. Code, V_{DD} = 5 V

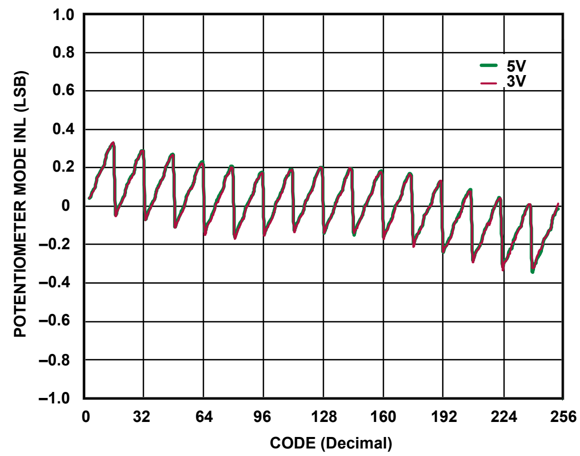

Figure 7. INL vs. Code vs. Supply Voltages

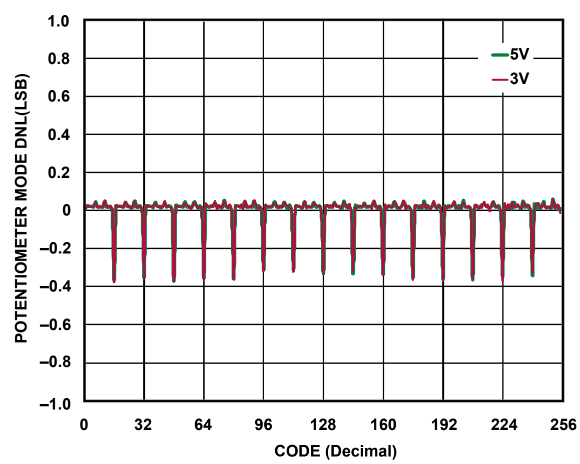

Figure 8. DNL vs. Code vs. Supply Voltages

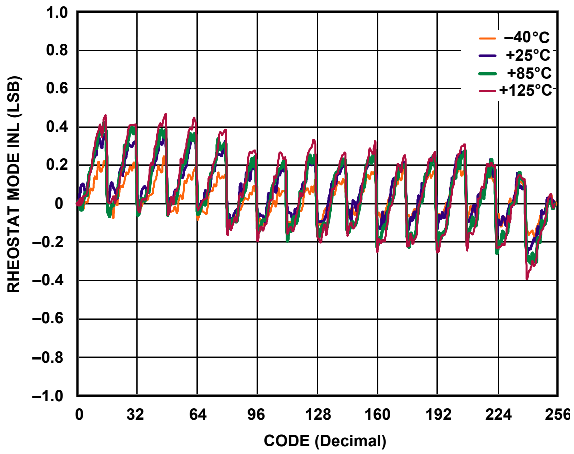

Figure 9. R-INL vs. Code, V_{DD} = 5 V

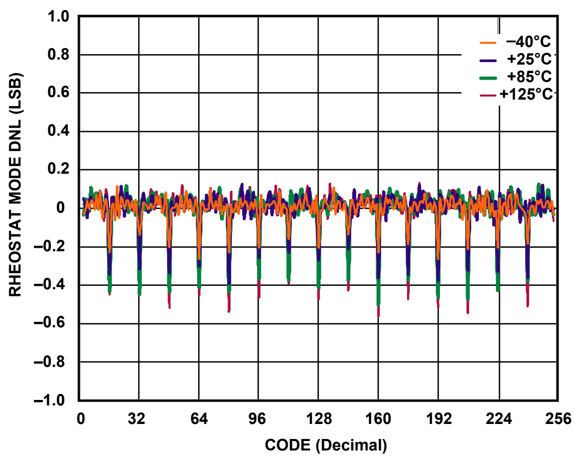

Figure 10. R-DNL vs. Code, V_{DD} = 5 V

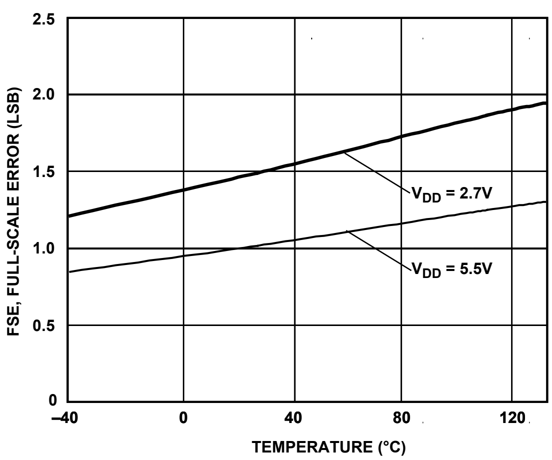

Figure 11. Full-Scale Error vs. Temperature

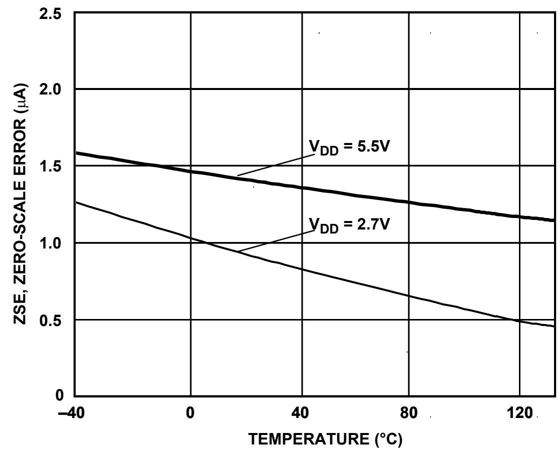

Figure 12. Zero-Scale Error vs. Temperature

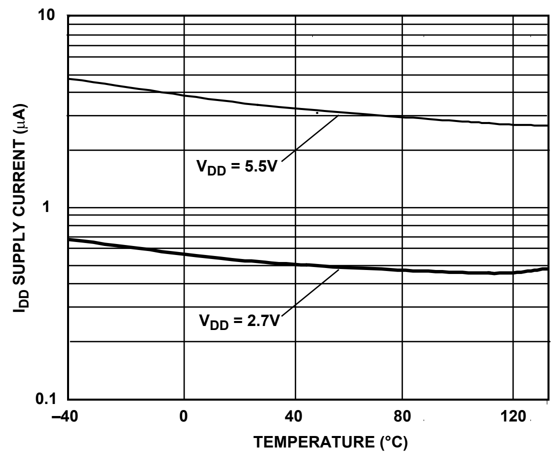

Figure 13. Supply Current vs. Temperature

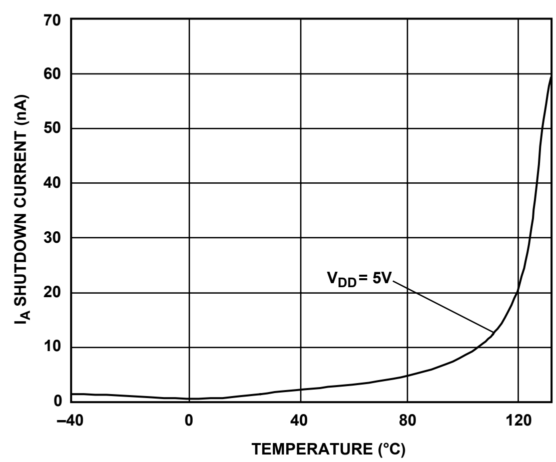

Figure 14. Shutdown Current vs. Temperature

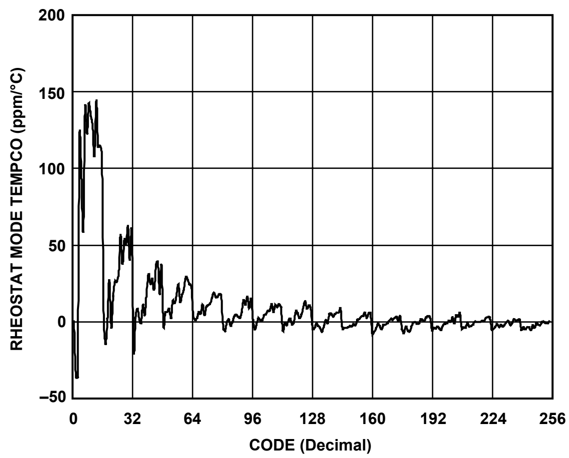

Figure 15. Rheostat Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code

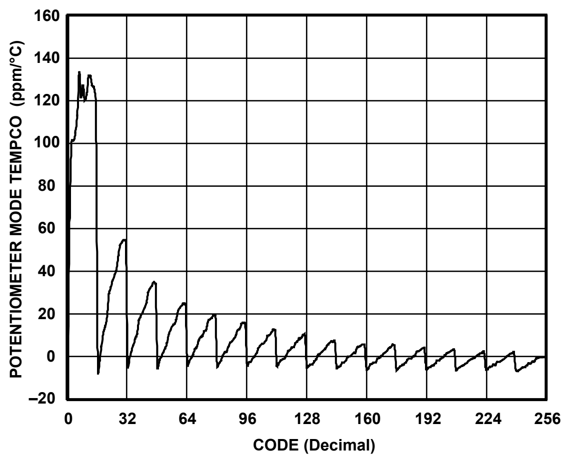

Figure 16. Potentiometer Mode Tempco $\Delta V_{WB}/\Delta T$ vs. Code

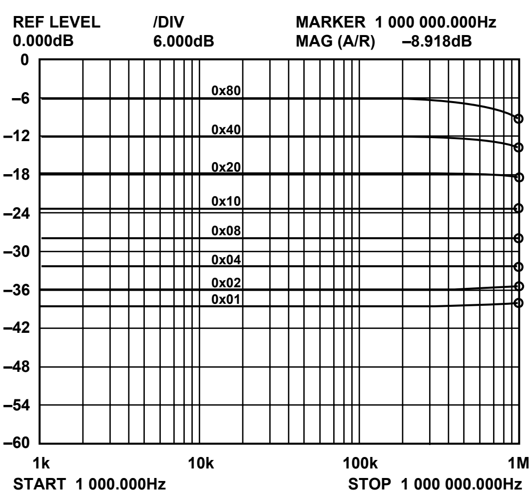

Figure 17. Gain vs. Frequency vs. Code, R_{AB} = 5 kΩ

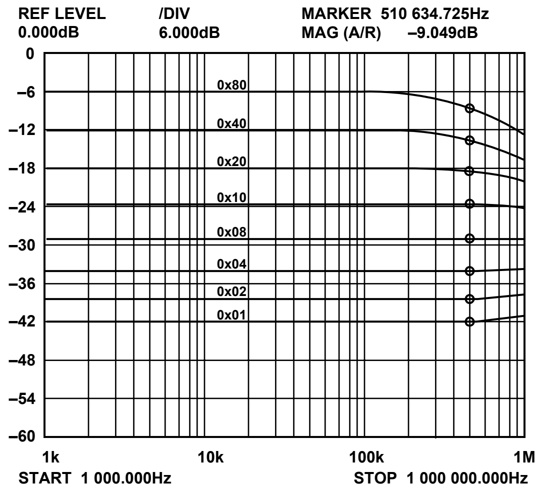

Figure 18. Gain vs. Frequency vs. Code, R_{AB} = 10 kΩ

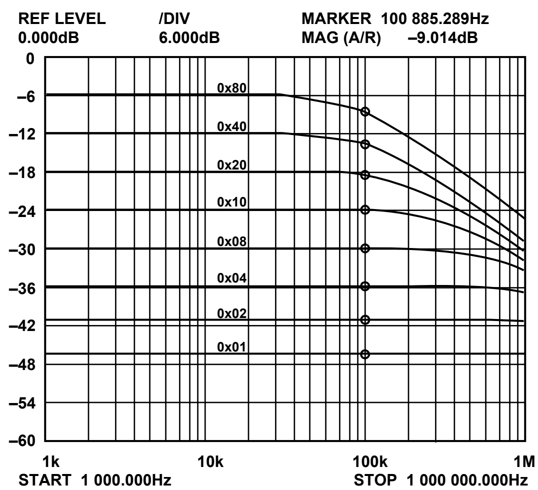

Figure 19. Gain vs. Frequency vs. Code, R_{AB} = 50 kΩ

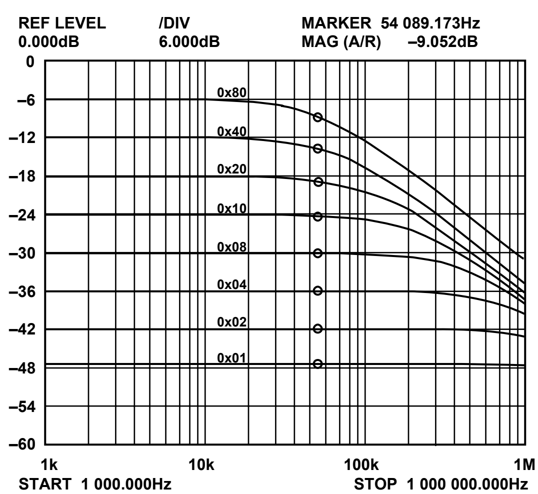

Figure 20. Gain vs. Frequency vs. Code, R_{AB} = 100 kΩ

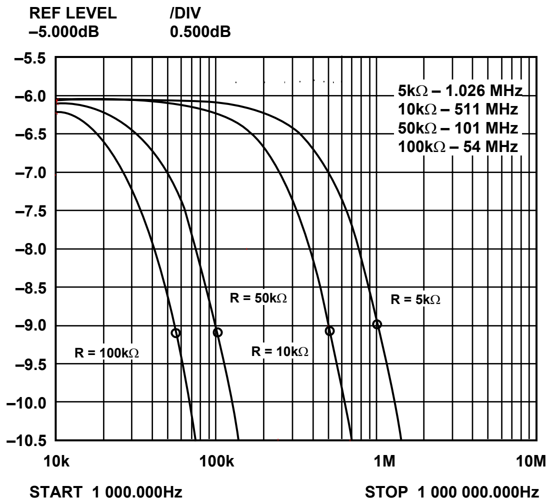

Figure 21. –3 dB Bandwidth @ Code = 0x80

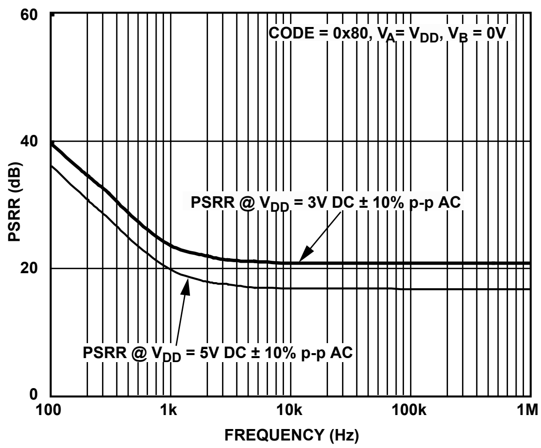

Figure 22. PSRR vs. Frequency

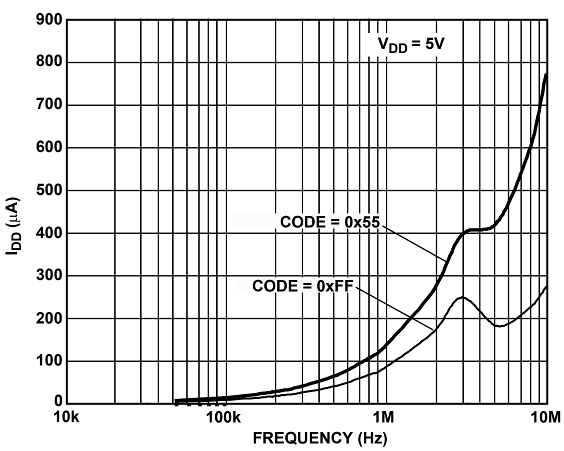

Figure 23. I_{DD} vs. Frequency

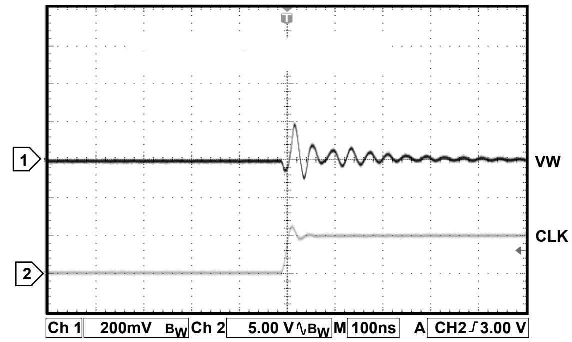

Figure 24. Digital Feedthrough

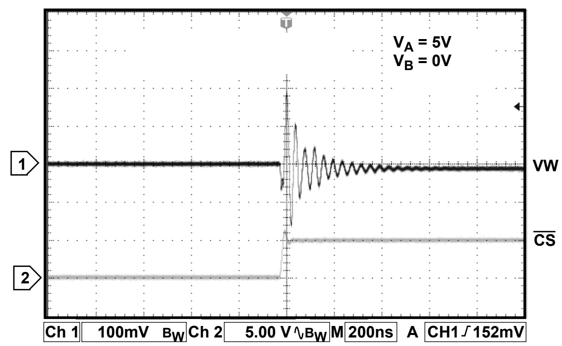

Figure 25. Midscale Glitch, Code 0x80–0x7F

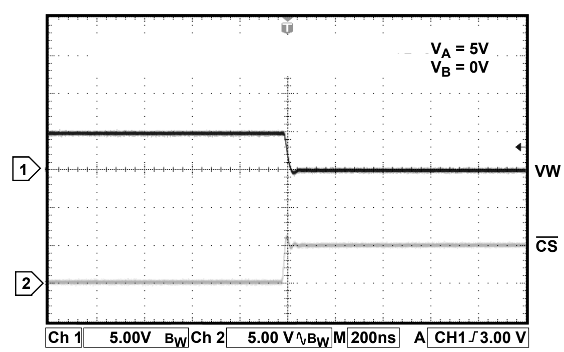

Figure 26. Large Signal Settling Time, Code 0xFF–0x00

TEST CIRCUITS

Figure 27 to Figure 35 illustrate the test circuits that define the test conditions used in the product specification tables.

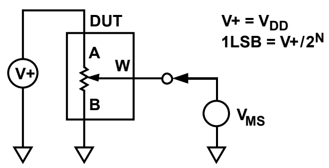

Figure 27. Test Circuit for Potentiometer Divider Nonlinearity Error (INL, DNL)

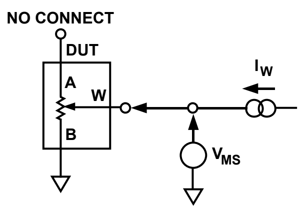

Figure 28. Test Circuit for Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

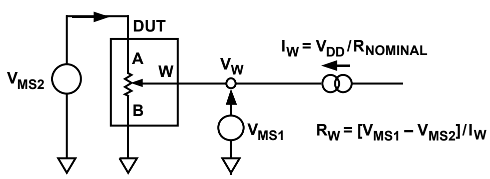

Figure 29. Test Circuit for Wiper Resistance

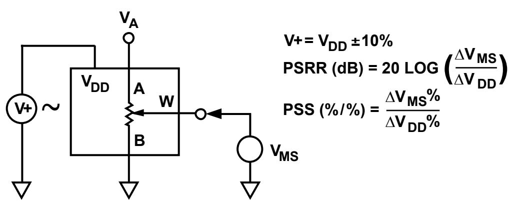

Figure 30. Test Circuit for Power Supply Sensitivity (PSS, PSSR)

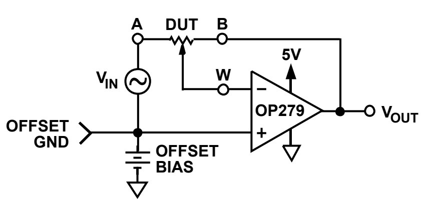

Figure 31. Test Circuit for Inverting Gain

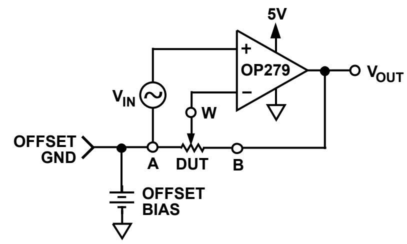

Figure 32. Test Circuit for Noninverting Gain

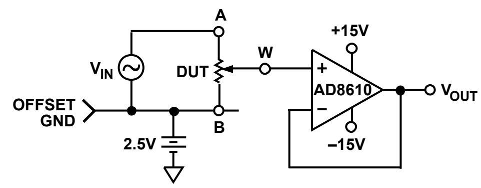

Figure 33. Test Circuit for Gain vs. Frequency

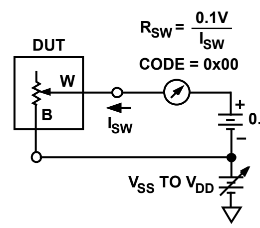

Figure 34. Test Circuit for Incremental ON Resistance

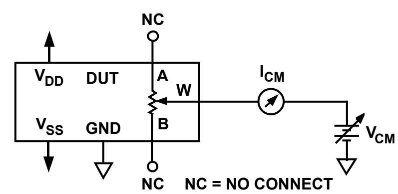

Figure 35. Test Circuit for Common-Mode Leakage current

SPI INTERFACE

Table 5. AD5160 Serial Data-Word Format

B7	B6	B5	B4	B3	B2	B1	B0
D7 MSB 2^7	D6	D5	D4	D3	D2	D1	D0 LSB 2^0

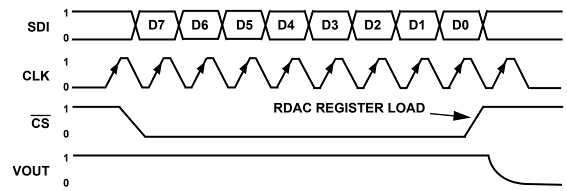

Figure 36. AD5160 SPI Interface Timing Diagram (V_A = 5 V, V_B = 0 V, V_W = V_{OUT})

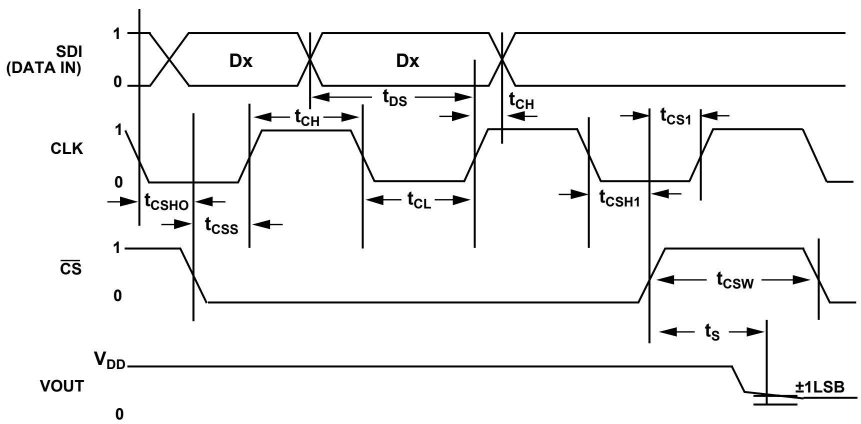

Figure 37. SPI Interface Detailed Timing Diagram (V_A = 5 V, V_B = 0 V, V_W = V_{OUT})

OPERATION

The AD5160 is a 256-position digitally controlled variable resistor (VR) device.

An internal power-on preset places the wiper at midscale during power-on, which simplifies the fault condition recovery at power-up.

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistance of the RDAC between terminals A and B is available in 5 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ. The final two or three digits of the part number determine the nominal resistance value, e.g., 10 kΩ = 10; 50 kΩ = 50. The nominal resistance (R_{AB}) of the VR has 256 contact points accessed by the wiper terminal, plus the B terminal contact. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible settings. Assume a 10 kΩ part is used, the wiper's first connection starts at the B terminal for data 0x00. Since there is a 60 Ω wiper contact resistance, such connection yields a minimum of 60 Ω resistance between terminals W and B. The second connection is the first tap point, which corresponds to 99 Ω ($R_{WB} = R_{AB}/256 + R_W$ = 39 Ω + 60 Ω) for data 0x01. The third connection is the next tap point, representing 177 Ω (2 × 39 Ω + 60 Ω) for data 0x02, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 9961 Ω (R_{AB} – 1 LSB + R_W). Figure 38 shows a simplified diagram of the equivalent RDAC circuit where the last resistor string will not be accessed; therefore, there is 1 LSB less of the nominal resistance at full scale in addition to the wiper resistance.

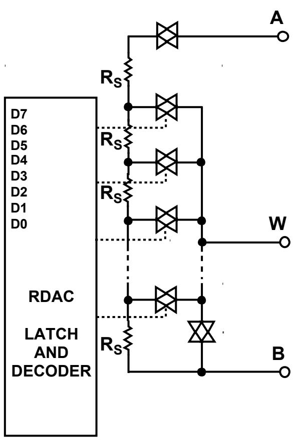

Figure 38. AD5160 Equivalent RDAC Circuit

The general equation determining the digitally programmed output resistance between W and B is

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + R_W \tag{1}$$

where D is the decimal equivalent of the binary code loaded in the 8-bit RDAC register, R_{AB} is the end-to-end resistance, and R_W is the wiper resistance contributed by the on resistance of the internal switch.

In summary, if R_{AB} = 10 kΩ and the A terminal is open circuited, the following output resistance R_{WB} will be set for the indicated RDAC latch codes.

Table 6. Codes and Corresponding R_{WB} Resistance

D (Dec.)	R_{WB} (Ω)	Output State
255	9,961	Full Scale (R_{AB} – 1 LSB + R_W)
128	5,060	Midscale
1	99	1 LSB
0	60	Zero Scale (Wiper Contact Resistance)

Note that in the zero-scale condition a finite wiper resistance of 60 Ω is present. Care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the wiper W and terminal A also produces a digitally controlled complementary resistance R_{WA}. When these terminals are used, the B terminal can be opened. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{256} \times R_{AB} + R_W \tag{2}$$

For R_{AB} = 10 kΩ and the B terminal open circuited, the following output resistance R_{WA} will be set for the indicated RDAC latch codes.

Table 7. Codes and Corresponding R_{WA} Resistance

D (Dec.)	R_{WA} (Ω)	Output State
255	99	Full Scale
128	5,060	Midscale
1	9,961	1 LSB
0	10,060	Zero Scale

Typical device to device matching is process lot dependent and may vary by up to ±30%. Since the resistance element is processed in thin film technology, the change in R_{AB} with temperature has a very low 45 ppm/°C temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at wiper-to-B and wiper-to-A proportional to the input voltage at A-to-B. Unlike the polarity of V_{DD} to GND, which must be positive, voltage across A-B, W-A, and W-B can be at either polarity.

If ignoring the effect of the wiper resistance for approximation, connecting the A terminal to 5 V and the B terminal to ground produces an output voltage at the wiper-to-B starting at 0 V up to 1 LSB less than 5 V. Each LSB of voltage is equal to the voltage applied across terminal AB divided by the 256 positions of the potentiometer divider. The general equation defining the output voltage at V_W with respect to ground for any valid input voltage applied to terminals A and B is

$$V_W(D) = \frac{D}{256} V_A + \frac{256 - D}{256} V_B \quad (3)$$

For a more accurate calculation, which includes the effect of wiper resistance, V_W, can be found as

$$V_W(D) = \frac{R_{WB}(D)}{256} V_A + \frac{R_{WA}(D)}{256} V_B \quad (4)$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent mainly on the ratio of the internal resistors R_{WA} and R_{WB} and not the absolute values. Therefore, the temperature drift reduces to 15 ppm/°C.

SPI COMPATIBLE 3-WIRE SERIAL BUS

The AD5160 contains a 3-wire SPI compatible digital interface (SDI, $\overline{CS}$, and CLK). The 8-bit serial word must be loaded MSB first. The format of the word is shown in Table 5.

The positive-edge sensitive CLK input requires clean transitions to avoid clocking incorrect data into the serial input register. Standard logic families work well. If mechanical switches are used for product evaluation, they should be debounced by a flip-flop or other suitable means. When $\overline{CS}$ is low, the clock loads data into the serial register on each positive clock edge (see Figure 36).

The data setup and data hold times in the specification table determine the valid timing requirements. The AD5160 uses an 8-bit serial input data register word that is transferred to the internal RDAC register when the $\overline{CS}$ line returns to logic high. Extra MSB bits are ignored.

ESD PROTECTION

All digital inputs are protected with a series input resistor and parallel Zener ESD structures shown in Figure 39 and Figure 40. This applies to the digital input pins SDI, CLK, and $\overline{CS}$.

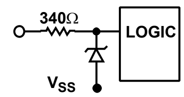

Figure 39. ESD Protection of Digital Pins

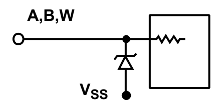

Figure 40. ESD Protection of Resistor Terminals

TERMINAL VOLTAGE OPERATING RANGE

The AD5160 V_{DD} and GND power supply defines the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on terminals A, B, and W that exceed V_{DD} or GND will be clamped by the internal forward biased diodes (see Figure 41).

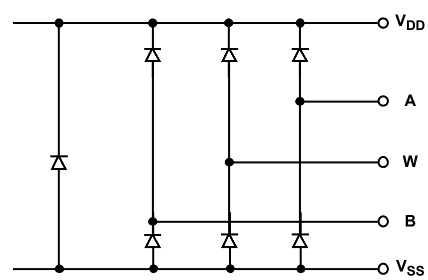

Figure 41. Maximum Terminal Voltages Set by V_{DD} and V_{SS}

POWER-UP SEQUENCE

Since the ESD protection diodes limit the voltage compliance at terminals A, B, and W (see Figure 41), it is important to power V_{DD}/GND before applying any voltage to terminals A, B, and W; otherwise, the diode will be forward biased such that V_{DD} will be powered unintentionally and may affect the rest of the user's circuit. The ideal power-up sequence is in the following order: GND, V_{DD}, digital inputs, and then $V_{A/B/W}$. The relative order of powering V_A, V_B, V_W, and the digital inputs is not important as long as they are powered after V_{DD}/GND.

LAYOUT AND POWER SUPPLY BYPASSING

It is a good practice to employ compact, minimum lead length layout design. The leads to the inputs should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also a good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with disc or chip ceramic capacitors of 0.01 µF to 0.1 µF. Low ESR 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at the supplies to minimize any transient disturbance and low frequency ripple (see Figure 42). Note that the digital ground should also be joined remotely to the analog ground at one point to minimize the ground bounce.

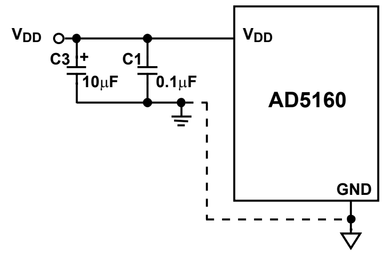

Figure 42. Power Supply Bypassing

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

PIN CONFIGURATION

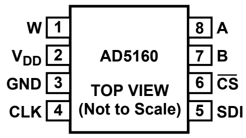

Figure 43.

PIN FUNCTION DESCRIPTIONS

Table 8.

Pin	Name	Description
1	W	W Terminal.
2	V_{DD}	Positive Power Supply.
3	GND	Digital Ground.
4	CLK	Serial Clock Input. Positive edge triggered.
5	SDI	Serial Data Input.
6	$\overline{CS}$	Chip Select Input, Active Low. When $\overline{CS}$ returns high, data will be loaded into the DAC register.
7	B	B Terminal.
8	A	A Terminal.

OUTLINE DIMENSIONS

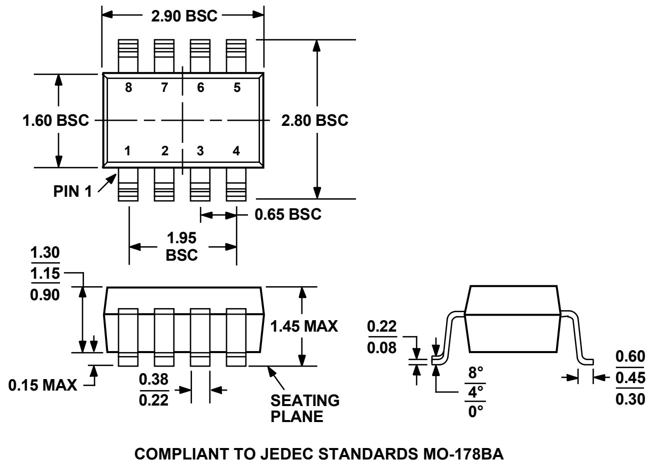

Figure 44. 8-Lead Small Outline Transistor Package [SOT-23]
(RJ-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	R_{AB} (Ω)	Temperature	Package Description	Package Option	Branding
AD5160BRJ5-R2	5k	–40°C to +125°C	SOT-23-8	RJ-8	D08
AD5160BRJ5-RL7	5k	–40°C to +125°C	SOT-23-8	RJ-8	D08
AD5160BRJ10-R2	10k	–40°C to +125°C	SOT-23-8	RJ-8	D09
AD5160BRJ10-RL7	10k	–40°C to +125°C	SOT-23-8	RJ-8	D09
AD5160BRJ50-R2	50k	–40°C to +125°C	SOT-23-8	RJ-8	D0A
AD5160BRJ50-RL7	50k	–40°C to +125°C	SOT-23-8	RJ-8	D0A
AD5160BRJ100-R2	100k	–40°C to +125°C	SOT-23-8	RJ-8	D0B
AD5160BRJ100-RL7	100k	–40°C to +125°C	SOT-23-8	RJ-8	D0B
AD5160EVAL	See Note 1		Evaluation Board		

[1]The evaluation board is shipped with the 10 kΩ R_{AB} resistor option; however, the board is compatible with all available resistor value options.

The AD5160 contains 2532 transistors. Die size: 30.7 mil × 76.8 mil = 2,358 sq. mil.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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