High Voltage, Quad Channel 12-Bit Voltage Output DAC

Preliminary Technical Data

AD5504

FEATURES

Quad channel high voltage DAC
12-bit resolution
Pin selectable 30 V or 60 V output range
Integrated Precision Reference
Low power serial interface with readback capability
Integrated Temperature Sensor Alarm function
Power-On Reset
Simultaneous updating via $\overline{\text{LDAC}}$
Wide operating temperature: –40°C to +105°C

APPLICATIONS

Programmable voltage source
Programmable current source
High Voltage LED Driver
Receiver bias in optical communications

FUNCTIONAL BLOCK DIAGRAM

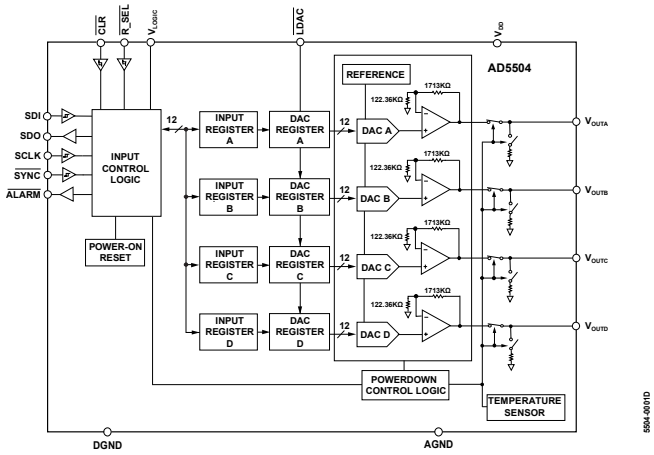

Figure 1.

GENERAL DESCRIPTION

The AD5504 is a four channel, 12-bit, serial input, digital-to-analog converter with on-chip high voltage output amplifiers and an integrated precision reference. The DAC output voltage ranges are programmable via the range-select pin ($\overline{\text{R\_SEL}}$).If $\overline{\text{R\_SEL}}$ is held high the DAC output ranges are 0 V to 30 V. If $\overline{\text{R\_SEL}}$ is held low the DAC output ranges are 0 V to 60 V. The on-chip output amplifiers allow an output swing within the range of AGND + 0.2 V and V_{DD} –0.5 V.

The AD5504 has a high-speed serial interface, which is compatible with SPI®, QSPI™ ,MICROWIRE™ ,and DSP interface standards and can handle clock speeds of up to 30MHz. The serial interface offers the user the capability of both writing-to and reading-from most or the internal registers. To reduce power consumption on power up, only the digital section of the AD5504 is powered up initially. This gives the user the ability to program the DAC registers to the required value while only consuming typically 23 µA of supply current. The AD5504 incorporates power-on-reset circuitry which ensures the DAC registers powers up in a known condition and remains there until a valid write to the device has taken place.

The analog section is powered up by issuing a power-up command via the SPI interface. The AD5504 provides software-selectable output loads while in the power-down mode.

The AD5504 has on-chip temperature sensor. If the temperature on the die exceeds 130ºC the $\overline{\text{ALARM}}$ pin, an active low CMOS output pin, flags an alarm and the AD5504 enters a temperature power-down mode disconnecting the output amplifier thus removing the short circuit condition. The AD5504 remains in power down mode until a software power-up command is executed.

The AD5504 is available in a compact 16-lead TSSOP. The AD5504 is guaranteed to operate over the extended temperature range of –40°C to +105°C.

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REVISION HISTORY

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SPECIFICATIONS

V_{DD} = 10 V to 62 V; V_{LOGIC} = 2.3 V to 5.5 V; R_L = 60kΩ .C_L = 200pF; −40°C < T_A < +105°C, unless otherwise noted

Table 1.

Parameter	Min	Typ[1]	Max	Unit	Test Conditions / Comments
ACCURACY[2]					
Resolution		12		Bits	
Differential Nonlinearity (DNL)	−1		1	LSB	
Integral Nonlinearity (INL)	−1		1	LSB	
V_{OUTX} Temperature Coefficient[3,4,5]		50		ppm/°C	DAC-code = half scale
Zero Scale Error (V_{ZSE})			50	mV	
Zero Scale Error Drift		TBD		µV/°C	
Full Scale Error (V_{FSE})			150	mV	
Full Scale Error Drift		TBD		µV/°C	
Gain Error			±0.03	% of FSR	
Gain Temperature Coefficient		TBD		ppm of FSR/°C	
DC Crosstalk					R_L=60KΩ to AGND or V_{DD}
Due to single channel full-scale output change		4		mV	60V mode
Due to powering down (per channel)		15		mV	60V mode
OUTPUT CHARACTERISTICS					
Output Voltage Range[6]	AGND + 0.2		V_{DD} − 0.5	V	
Short Circuit Current[4,7]		2		mA	On any single channel
Capacitive Load Stability[4]					
R_L = ∞			1	nF	
R_L = 60KΩ		TBD		nF	
Load Current[4]	−1		1	mA	On any single channel
DC Output Impedance[4]			TBD	Ω	
DC Output Leakage		10		µA	
DIGITAL INPUTS					JEDEC compliant
Input Logic High (V_{IH})	2.0			V	V_{LOGIC} = 4.5 V to 5.5 V
	1.8			V	V_{LOGIC} = 2.3 V to 3.6 V
Input Logic Low (V_{IL})			0.8	V	V_{LOGIC} = 2.3 V to 5.5 V
Input Current (I_{IL})			±1	µA	
Input Capacitance (I_{IC})[4]		5		pF	
DIGITAL OUTPUTS					
Output High Voltage (V_{OH})	V_{LOGIC} − 0.4 V			V	I_{SOURCE} = 200µA
Output Low Voltage (V_{OL})			DGND +0.4 V	V	I_{SINK} = 200µA
Three state Leakage Current	−1		1	µA	
Output Capacitance[4]		5		pF	

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Parameter	Min	Typ[1]	Max	Unit	Test Conditions / Comments
POWER SUPPLIES					
V_{DD}	10		62	V	
V_{LOGIC}	2.3		5.5	V	
Quiescent Supply Current ($I_{QUIESCENT}$)		2.5	TBD	mA	Static conditions
Logic Supply Current (I_{LOGIC})		1.5	50	µA	$V_{IH} = V_{LOGIC}$; V_{IL} = DGND
DC PSRR		80		dB	DAC output = full-scale
POWERDOWN MODE					
Supply current (I_{DD_PWD})					
Software powerdown mode		23	50	µA	
Thermal shutdown mode		125	150	µA	
Junction Temperature (T_J)[7]			130	°C	$T_J = T_A + P_{TOTAL} \times \theta_{JA}$

[1] Typical specifications represent average readings at 25°C, V_{DD} = 30.5 V and V_{LOGIC} = 5 V.
[2] Valid in output voltage range of (V_{DD} – 0.5 V) to (AGND + 0.2 V). Outputs are unloaded.
[3] Includes linearity, offset and gain drift.
[4] Guaranteed by design and characterization. Not production tested.
[5] V_{OUTX} refers to V_{OUTA}, V_{OUTB}, V_{OUTC} or V_{OUTD}
[6] The DAC architecture gives a fixed linear voltage output range of 0 V to 30 V if $\overline{R\_SEL}$ is held high and 0V to 60V if $\overline{R\_SEL}$ is held low. As the output voltage range is limited by output amplifier compliance. V_{DD} should be set to at least 0.5 V higher than the maximum output voltage to ensure compliance.
[7] If the die temperature exceeds 130°C the AD5504 enters a temperature power-down mode putting the DAC outputs into a high impedance state thus removing the short circuit condition. Overheating caused by long term short circuit condition(s) is detected by an integrated thermal sensor. After power-down the AD5504 stays powered down until a software power-up command is executed.

AC CHARACTERISTICS

V_{DD} = 10 V to 62 V; V_{LOGIC} = 2.3 V to 5.5 V; R_L = 60KΩ; C_L = 200pF; −40°C < T_A < +105°C, unless otherwise noted.

Table 2.

Parameter[1, 2]	Min	Typ	Max	Unit	Conditions/Comments[3]
Output Voltage Settling Time		35	45	µs	¼ to ¾ scale settling to ±1 LSB,R_L = 60kΩ
Slew Rate		TBD		V/µs	
Digital-to-Analog Glitch Energy		450		nV-s	1 LSB change around major carry in 60 V mode
Glitch Impulse Peak Amplitude		200		mV	60 V mode
Digital Feedthrough		TBD		nV-s	
Digital Crosstalk		TBD		nV-s	
Analog Crosstalk		TBD		nV-s	
DAC-to-DAC Crosstalk		TBD		nV-s	
AC PSRR		TBD		dB	100Hz to 500KHz
Peak-to-Peak Noise		65		µV p-p	0.1 Hz to 10 Hz
		60		nV/√Hz	DAC code = 0x800, 10 kHz
Output Noise		10		µV p-p	0.1 Hz to 10 Hz

[1] Guaranteed by design and characterization; not production tested.
[2] See the Terminology section.
[3] Temperature range is −40°C to + 105°C, typical at 25°C.

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TIMING CHARACTERISTICS

V_{DD} = 30 V, V_{LOGIC} = 2.3 V to 5.5 V and −40°C < T_A < +105°C. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Limit[1]	Unit	Test Conditions/Comments
t_1[2]	33	ns min	SCLK cycle time
t_2	10	ns min	SCLK high time
t_3	10	ns min	SCLK low time
t_4	10	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5	5	ns min	Data setup time
t_6	7.5	ns min	Data hold time
t_7	0	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	20	ns min	Minimum $\overline{SYNC}$ high time
t_9	9	ns min	$\overline{SYNC}$ rising edge to next SCLK falling edge ignore
t_{10}	TBD	ns min	SCLK falling edge to $\overline{SYNC}$ fall ignore
t_{11}	TBD	ns min	$\overline{LDAC}$ pulse width low
t_{12}	TBD	ns min	SCLK falling edge to $\overline{LDAC}$ rising edge
t_{13}	TBD	ns min	$\overline{CLR}$ pulse width low
t_{14}	TBD	ns min	SCLK falling edge to $\overline{LDAC}$ falling edge
t_{15}	TBD	ns typ	$\overline{CLR}$ pulse activation time
t_{16}	TBD	ns typ	$\overline{ALARM}$ clear time
t_{17}[3]	45	ns max	SCLK rising edge to SDO valid
t_{18}[3]	50	ns min	SCLK to SDO Data hold time
t_{19}	9	ns min	$\overline{SYNC}$ rising edge to SCLK rising edge ignore
t_{20}[4]	TBD(20)	us max	Power-On-Reset time. (not shown)
t_{21}[5]	TBD(200)	us max	Power-on time. (not shown)

[1] All input signals are specified with tr = tf = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
[2] Maximum SCLK frequency is 30 MHz.
[3] Under load conditions outlined in Figure 2
[4] Time from V_{DD}/V_{LOGIC} supplies powered-up to when a digital interface command can be executed.
[5] Time required from execution of power-on software command to when the DAC outputs have settled.

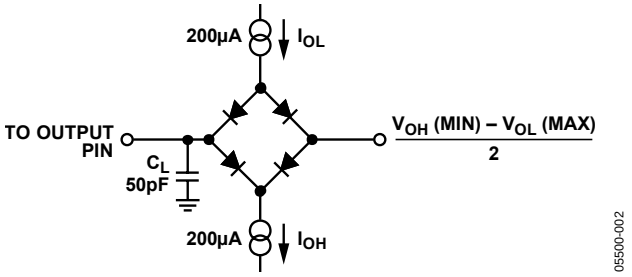

Figure 2. Load Circuit for SDO Timing Diagram

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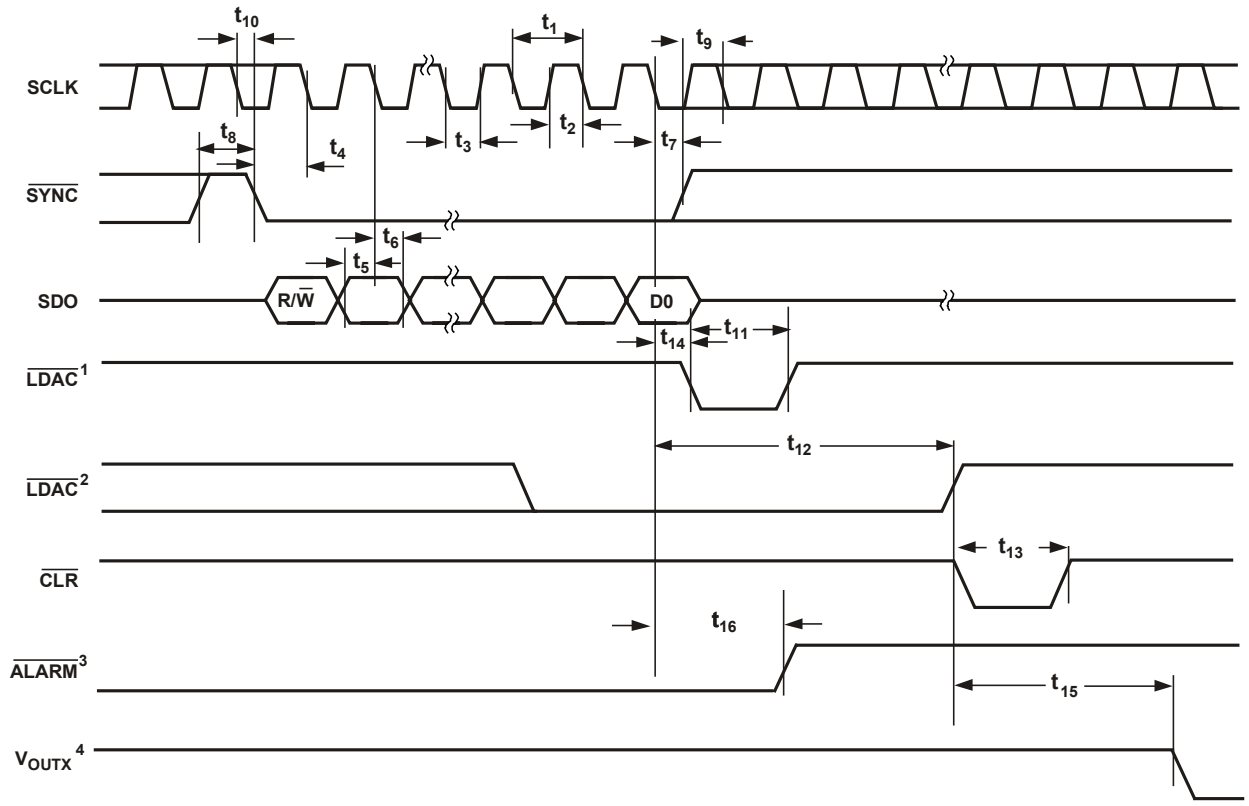

[1] ASYNCHRONOUS LDAC UPDATE MODE
[2] SYNCHRONOUS LDAC UPDATE MODE
[3] IN THE EVENT OF OVER-TEMPERATURE CONDITION
[4] V_{OUTX} REFERS TO ANY OF V_{OUTA}, V_{OUTB}, V_{OUTC} OR V_{OUTD}

Figure 3. Write Timing Diagram

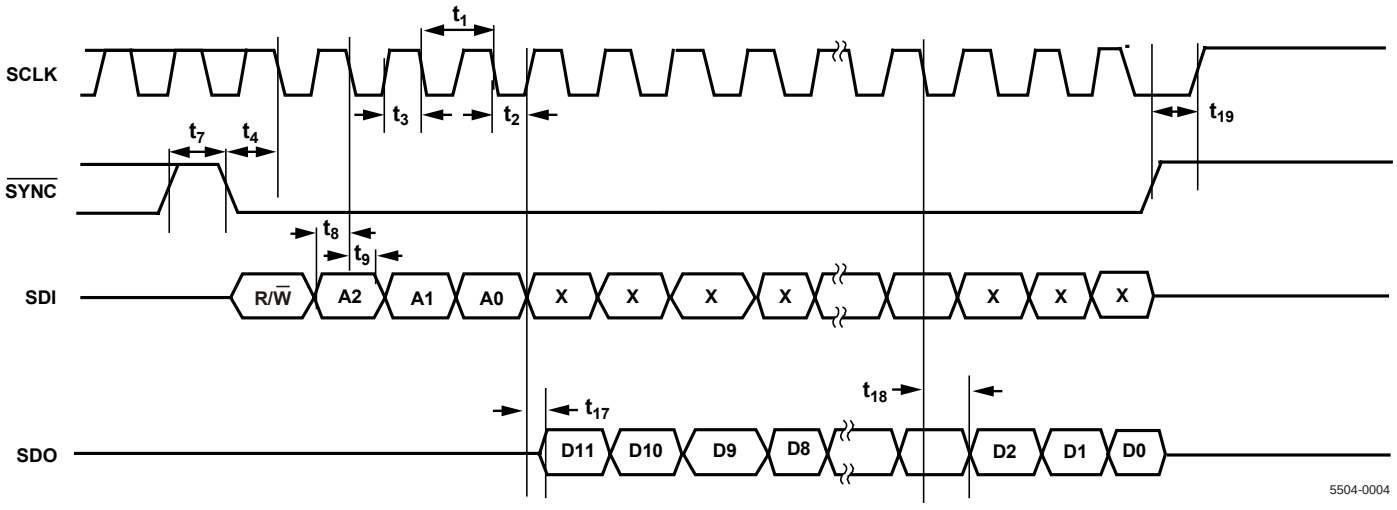

Figure 4. Read Timing Diagram

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ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to AGND	-0.3 V, +TBD V
V_{LOGIC} to DGND	-0.3 V to +7 V
V_{OUTX} to AGND[1]	-0.3 V to V_{DD} +0.3 V
Digital Input to DGND	-0.3 V to V_{LOGIC} + 0.3 V
SDO Output to DGND	-0.3 V to V_{LOGIC} + 0.3 V
AGND to DGND	-0.3 V to + 0.3 V
Maximum Junction Temperature (T_J max)	150°C
Storage Temperature Range	–65°C to +150°C
Reflow Soldering	
Peak Temperarure	260°C
Time at Peak Temperature	20 sec to 40 sec
Thermal Resistance Junction-to-Ambient θ_{JA}[2]	
16-lead TSSOP	112.60°C/W

[1] V_{OUTX} refers to V_{OUTA}, V_{OUTB}, V_{OUTC} or V_{OUTD}
[2] Thermal Resistance (JEDEC 4 layer(2S2P) board).

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

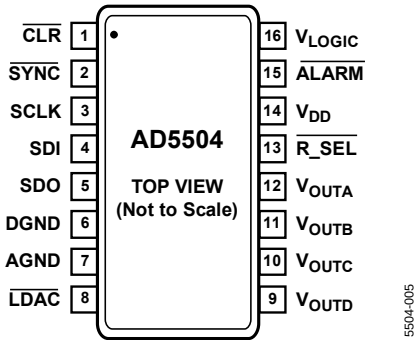

Figure 5. TSSOP Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{CLR}$	Asynchronous Clear Input. The $\overline{CLR}$ input is falling edge sensitive. When $\overline{CLR}$ is low, all $\overline{LDAC}$ pulses are ignored. When $\overline{CLR}$ is activated, the Input register and the DAC register are set to 0x000 and the outputs to zeroscale.
2	$\overline{SYNC}$	Falling Edge Synchronisation Signal. This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it enables the input shift register and data is transferred in on the falling edges of the following clocks. The selected DAC register is updated following the 16th clock cycle unless $\overline{SYNC}$ is taken high before this edge, in which case the rising edge of $\overline{SYNC}$ acts as an interrupt, and the write sequence is ignored by the DAC.
3	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 30 MHz.
4	SDI	Serial Data Input. This part has a 16-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
5	SDO	Serial Data Output. CMOS output. Serves as readback function for all DAC and Contol registers. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK
6	DGND	Digital Ground Pin.
7	AGND	Analog Ground Pin.
8	$\overline{LDAC}$	Load DAC Input. Pulsing this pin low allows any or all DAC registers to be updated if the Input registers have new data. This allows all DAC outputs to update simultaneously. Alternatively, this pin can be tied permanently low.
9	V_{OUTD}	Buffered Analog Output Voltage from DAC D
10	V_{OUTC}	Buffered Analog Output Voltage from DAC C
11	V_{OUTB}	Buffered Analog Output Voltage from DAC B
12	V_{OUTA}	Buffered Analog Output Voltage from DAC A
13	$\overline{R\_SEL}$	Range Select Pin. Tying this pin to DGND selects a DAC output range of 0 V to 60 V, alternatively tying $\overline{R\_SEL}$ to VLOGIC select a DAC output range of 0V to 30V.
14	V_{DD}	Positive Analog Power Supply; 10 V to 62 V for the specified performance. This pin should be decoupled with 0.1µF ceramic capacitors and 10 µF capacitors.
15	$\overline{ALARM}$	Active Low CMOS Output Pin. This pin flags an alarm if the temperature on the die exceeds 130°C.
16	V_{LOGIC}	Logic Power Supply; 2.3 V to 5.5 V. This pin should be decoupled with 0.1µF ceramic capacitors and 10 µF capacitors.

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TYPICAL PERFORMANCE CHARACTERISTICS

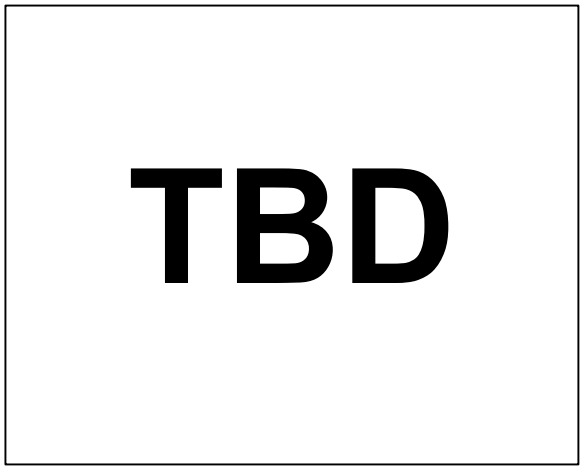

Figure 6

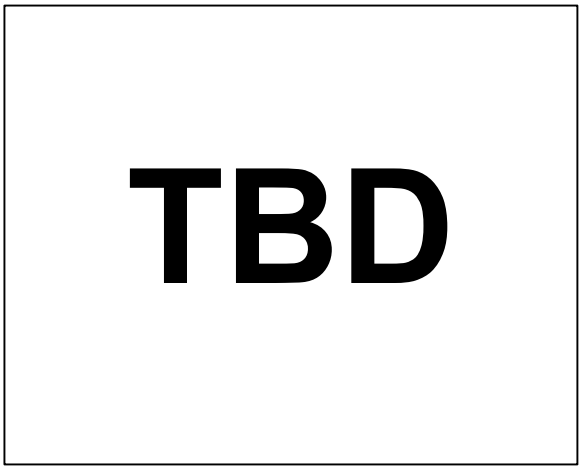

Figure 9

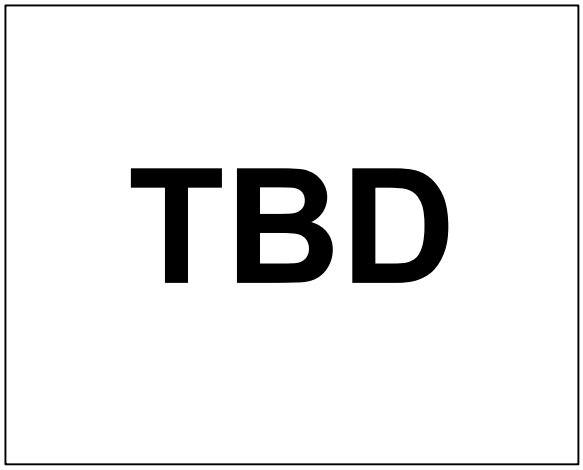

Figure 7

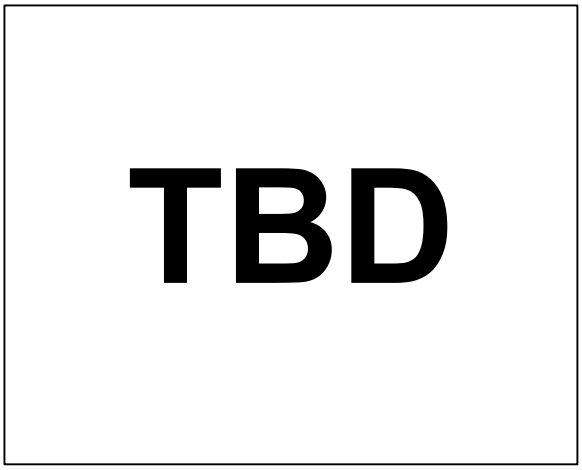

Figure 10

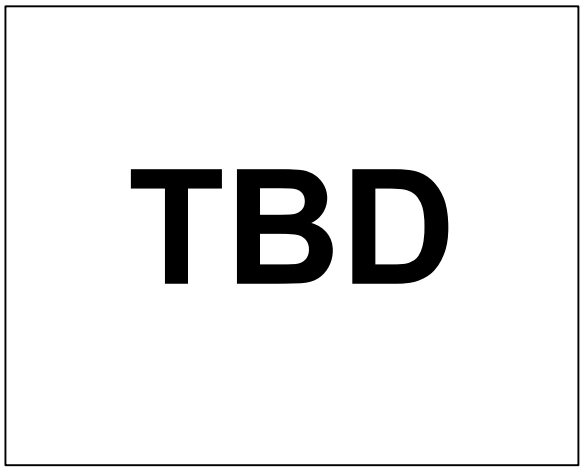

Figure 8

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TERMINOLOGY

Relative Accuracy
For the DAC, relative accuracy, or integral nonlinearity (INL), is a measure of the maximum deviation in LSBs from a straight line passing through the endpoints of the DAC transfer function.

Differential Nonlinearity
Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design.

Zero-Code Error
Zero-code error is a measure of the output error when zero code (0x000) is loaded into the DAC register. Ideally, the output should be 0 V. The zero-code error is always positive in the AD5504, because the output of the DAC cannot go below 0 V. It is due to a combination of the offset errors in the DAC and output amplifier. Zero-code error is expressed in millivolts.

Gain Error

Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal, expressed as a percentage of the full-scale range.

Zero-Code Error Drift

Zero-code error drift is a measure of the change in zero-code error with a change in temperature. It is expressed in µV/°C.

Gain Error Drift

Gain error drift is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Full-Scale Error
Full-scale error is a measure of the output error when full-scale code (0xFFF) is loaded into the DAC register. Full-scale error is expressed in mV.

Digital-to-Analog Glitch Impulse

Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s and is measured when the digital input code is changed by 1 LSB at the major carry transition (TBD).

DC Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUTA}, V_{OUTB}, V_{OUTC} or V_{OUTD} to a change in V_{DD} for full-scale output of the DAC. It is measured in decibels. V_{DD} is DC varied ±10%.

AC Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUTA}, V_{OUTB}, V_{OUTC} or V_{OUTD} to a change in V_{DD} for full-scale output of the DAC. It is measured in decibels. V_{DD} is AC varied ±10% .

DC Crosstalk
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC kept at midscale. It is expressed in millivolts.

DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has to another DAC kept at midscale. It is expressed in microvolts per milliamp.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of a DAC from the digital input pins of the device, but is measured when the DAC is not being written to ($\overline{SYNC}$ held high). It is specified in nV-s and measured with a full-scale change on the digital input pins, that is, from all 0s to all 1s or vice versa.

Analog Crosstalk
Analog crosstalk is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the Input registers with a full-scale code change (all 0s to all 1s or vice versa) while keeping $\overline{LDAC}$ high, and then pulsing $\overline{LDAC}$ low and monitoring the output of the DAC whose digital code has not changed. The area of the glitch is expressed in nV-s.

DAC-to-DAC Crosstalk
DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s or vice versa) with $\overline{LDAC}$ low and monitoring the output of another DAC. The energy of the glitch is expressed in nV-s.

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THEORY OF OPERATION

The AD5504 contains 4 DACs, 4 output amplifiers and a precision reference in a single package. The architecture of a single DAC channel consists of a 12-bit resistor-string DAC followed by an output buffer amplifier. The part operates from a single supply voltage of 10 V to 62 V. The DAC output voltage range is selected via the range-select, $\overline{\text{R\_SEL}}$, pin. The DAC output range is 0 V to 30 V if $\overline{\text{R\_SEL}}$ is held high and 0 V to 60 V if $\overline{\text{R\_SEL}}$ is held low. Data is written to the AD5504 in a 16-bit word format (see Table 7), via a serial interface.

POWER-UP STATE

On power-up, the Power-on-Reset circuitry clears the bits of the Control register (see Table 9) to 0. This ensures that the analog section is initially powered down, which helps reduce power consumption, and that the thermal shutdown mode is enabled but not activated. This allows the user to program the DAC registers to the required values while typically consuming only TBD µA of supply current. The power-on-reset circuitry also ensures that all the input and DAC registers power up in a known condition, 0x000, and remain there until a valid write to the device has taken place. The analog section can be powered up by setting any or all of bits C2 to C5 of the Control register to 1.

POWER-DOWN MODE

Each DAC channel can be individually powered up or powered down in groups by programming the Control register (see Table 9). When the DAC channel is powered down the associated analog circuitry is turn off to reduce power consumption. The digital section of the AD5504 remains powered up. The output of the DAC amplifier can be three-stated or connected to AGND via an internal 20KΩ resistor depending on the state of bit C6 in the Control register. The power-down mode does not change the contents of the DAC register. This ensures that the DAC channel returns to its previous voltage when the power-down bit is set to 1. The AD5504 also offers the user the flexibility of updating the DAC registers during power-down. The Control register can be read back at any time to check the status of the bits.

DAC CHANNEL ARCHITECTURE

The architecture of a single DAC channel consists of a 12-bit resistor-string DAC followed by an output buffer amplifier (see Figure 7). The resistor-string section is simply a string of resistors, each of value R, from V_{REF}, generated by the precision reference, to AGND. This type of architecture guarantees DAC monotonicity. The 12-bit binary digital code loaded to the DAC register determines at which node on the string the voltage is tapped off before being fed into the output amplifier. The data format for the AD5504 is straight binary as shown in Table 6. The output amplifier multiplies the DAC output voltage to give a fixed linear voltage output range of 0 V to 60 V if $\overline{\text{R\_SEL}}$=0 or 0 V to 30 V if $\overline{\text{R\_SEL}}$=1. Each output amplifier is capable of driving a 40KΩ load while allowing an output swing within the range of AGND +TBD V and V_{DD} – TBD V.

As the DAC architecture gives a fixed voltage output range of 0 to 30 V or 0 to 60 V the user should set V_{DD} to at least 30.5 V or 60.5 V to use the maximum DAC resolution.

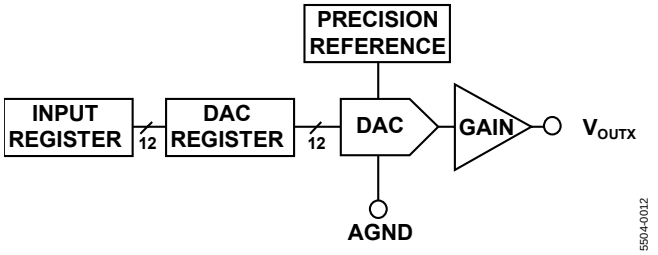

Figure 11. DAC Channel Architecture (Single Channel Shown)

Table 6. DAC Data Format

DAC Value	Output Voltage	
	30 V Mode	60 V Mode
0b0000 0000 0000	0.000000000	0.000000000
0b0000 0000 0001	0.007324219	0.014648438
0b0000 0000 0010	0.014648438	0.029296875
0b0111 1111 1111	14.99267578	29.98535156
0b1000 0000 0000	15.00000000	30.00000000
0b1111 1111 1110	29.98535156	59.97070313
0b1111 1111 1111	29.99267578	59.98535156

SELECTING THE OUTPUT RANGE

The output range of the DACs is selected by the $\overline{\text{R\_SEL}}$ pin. When the $\overline{\text{R\_SEL}}$ pin is connected to logic 1 the DAC output voltages can be set between 0 V and 30 V. When the $\overline{\text{R\_SEL}}$ pin is connected to logic 0 the DAC output voltages can be set between 0 V and 60 V. The state of $\overline{\text{R\_SEL}}$ can be changed any time when the serial interface is not being used, i.e. not during a read or write operation. When the $\overline{\text{R\_SEL}}$ pin is changed, the voltage on the output pin remains the same until the next write to the DAC register (and $\overline{\text{LDAC}}$ is brought low). For example, if the user writes 0x800 to the DAC register when in 30 V mode ($\overline{\text{R\_SEL}}$=1) the output voltage is 15 V (assuming $\overline{\text{LDAC}}$ is low or has been pulsed low). When the user switches to 60 V mode ($\overline{\text{R\_SEL}}$=0) the output stays at 15 V until the user writes a new value to the DAC register. $\overline{\text{LDAC}}$ must be low or be pulsed low for the output to change.

$\overline{\text{CLR}}$ FUNCTION

The AD5504 has a hardware $\overline{\text{CLR}}$ pin that is an asynchronous clear input. The $\overline{\text{CLR}}$ input is falling edge sensitive. Bringing the $\overline{\text{CLR}}$ line low clears the contents of the Input register and the DAC registers to 0x000. The $\overline{\text{CLR}}$ pulse activation time, i.e. the falling edge of $\overline{\text{CLR}}$ to when the output starts to change, is typically TBD ns.

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$\overline{\text{LDAC}}$ FUNCTION

The DAC outputs can be updated using the hardware $\overline{\text{LDAC}}$ pin. $\overline{\text{LDAC}}$ is normally high. On the falling edge of $\overline{\text{LDAC}}$ data is copied from the Input registers to the DAC registers and the DAC outputs are updated simultaneously (Asynchronous update mode, see Figure 3). If the $\overline{\text{LDAC}}$ is kept low, or is low on the falling edge of the 16th SCLK the appropriate DAC register and DAC output are updated automatically (Synchronous update mode, see Figure 3).

TEMPERATURE SENSOR

The AD5504 can be programmed to enter thermal shutdown mode if the temperature on the die exceeds 130°C. Setting bit 1 of the Control register (see Table 9) to 0 enables this function (enabled by default on power-up). In thermal shutdown mode the analog section of the device is powered down, the DAC outputs are disconnected but the digital section remains operational, which is equivalent to setting the power-down bit in the Control register. To indicate that the AD5504 has entered temperature shutdown mode, bit 0 of the Control register is set to 1 and the $\overline{\text{ALARM}}$ pin goes low. The AD5504 remains in temperature shutdown mode with bit 0 set to 1 and the $\overline{\text{ALARM}}$ pin low, even if the die temperature falls, until bit 0 in the Control register is cleared to 0.

POWER DISSIPATION

Drawing current from any of the voltage output pins causes a temperature rise in the die and package of the AD5504. The die temperature (T_J) should not exceed 130°C for normal operation. If bit 1 of the Control register is set and the die temperature exceeds 130°C the AD5504 enters thermal shutdown mode as described in the previous section. The amount of heat generated can be calculated using the formula

$$T_J = T_A + (P_{TOTAL} \times \theta_{JA})$$

Where:

T_J is the package junction temperature
T_A is the ambient temperature
P_{TOTAL} is the total power being consumed by the AD5504
θ_{JA} is the thermal impedance of the AD5504 package (see the Absolute Maximum Ratings for this value).

POWER SUPPLY SEQUENCING

The power supplies for the AD5504 can be applied in any order without affecting the device. However, in order to ensure that the serial interface operates correctly after power up the digital input pins should not be allowed to float. Floating pins may be interpreted as SCLK, SDI or $\overline{\text{SYNC}}$ pulses by the AD5504 if they cross the switching thresholds of the digital input circuitry. The digital input pins can be connected to pull-up (to V_{LOGIC}) or pull-down (to DGND) resistors as required.

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SERIAL INTERFACE

The AD5504 has a serial interface ($\overline{SYNC}$, SCLK, SDI and SDO), which is compatible with SPI interface standards, as well as most DSPs. The AD5504 allows writing of data, via the serial interface, to the Input and Control registers. The DAC registers are not directly writeable or readable.

The input shift register is 16 bits wide (see Table 7). The 16-bit word consists of one read/write (R/$\overline{W}$) control bit, followed by three address bits and twelve DAC data bits. Data is loaded MSB first.

WRITE MODE

To write to a register the R/$\overline{W}$ bit should be 0. The three address bits then determine the register to update. The address bits (A2-A0) are used for either DAC register selection or for writing to the Control register (see Table 8). Data is clocked into the selected register during the remaining twelve clocks of the same frame. Figure 3 shows a timing diagram of a typical AD5504 write sequence. The write sequence begins by bringing the $\overline{SYNC}$ line low. Data on the SDI line is clocked into the 16-bit shift register on the falling edge of SCLK. On the 16th falling clock edge, the last data bit is clocked in and the programmed function is executed (that is, a change in the selected DAC/DACs Input register/registers or a change in the mode of operation). The AD5504 does not require a continuous SCLK and dynamic power can be saved by only transmitting clock pulses during a serial write. At this stage, the $\overline{SYNC}$ line can be kept low or be brought high. In either case, it must be brought high for a minimum of 20 ns before the next write sequence so that a falling edge of $\overline{SYNC}$ can initiate the next write sequence. All interface pins should be operated at close to the supply rails to minimize power consumption in the digital input buffers.

READ MODE

The AD5504 allows data readback via the serial interface from every register directly accessible to the serial interface, which is all registers except the DAC registers. In order to read back a register, it is first necessary to tell the AD5504 that a readback is required. This is achieved by setting the R/$\overline{W}$ bit to 1. The three address bits then determine the register from which data is to be read back. Data from the selected register is then be clocked out of the SDO pin on the next twelve clocks of the same frame.

The SDO pin is three-stated or connected to DGND via a 20KΩ resistor (as determined by bit C6 of the Control register) but becomes driven on the rising edge of the fifth clock pulse. The pin remains driven until the registers data has been clocked out or the $\overline{SYNC}$ pin is returned high. Figure 4 shows the timing requirements during a read operation. Note that due to timing requirements of t_{17} TBD(25ns) the maximum speed of the SPI interface during a read operation should not exceed 20MHz

Table 7. Input Register Format

DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R/$\overline{W}$	A2	A1	A0	Data											

Table 8. Input Register Bit Functions

Bit	Description			
R/$\overline{W}$	Indicates a read from or a write to the addressed register.			
A2,A1,A0	These bits determine if the Input registers or the Control register are to be accessed.			
	A2	A1	A0	Function/Address
	0	0	0	No Operation
	0	0	1	DAC A Input register
	0	1	0	DAC B Input register
	0	1	1	DAC C Input register
	1	0	0	DAC D Input register
	1	0	1	Write Data contents to all 4 DAC Input registers
	1	1	0	Reserved
	1	1	1	Control register
D11:D0	Data Bits			

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Table 9. Control Register Functions

DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R/$\overline{W}$	1	1	1	X	X	X	X	X	C6	C5	C4	C3	C2	C1	C0

Read only bit. This bit should be 0 when writing to the Control register
C0 = 0 : device is not in thermal shutdown mode
C0 = 1 : device is in thermal shutdown mode
C1 = 0 : enable thermal shutdown mode(Default)
C1 =1 : disable thermal shutdown mode
C2 = 0 : DAC channel A power-down (Default)
C2 = 1 : DAC channel A power-up
C3 = 0 : DAC channel B power-down (Default)
C3 = 1 : DAC channel B power-up
C4 = 0 : DAC channel C power-down (Default)
C4 = 1 : DAC channel C power-up
C5 = 0 : DAC channel D power-down (Default)
C5 = 1 : DAC channel D power-up
C6 = 0 : Ouputs connected to AGND through a 20KΩ resistor (Default)
C6 = 1 : Outputs are three-stated
(If bits C2 to C5 are set to 0 then the part is placed in power-down mode)

INTERFACING EXAMPLES

The SPI interface of the AD5504 is designed to allow the it to be easily connected to industry-standard DSPs and microcontrollers. Figure 12 shows how the AD5504 can be connected to the Analog Devices, Inc., Black*fin*® DSP. The Black*fin* has an integrated SPI port that can be connected directly to the SPI pins of the AD5504, as well as programmable input/output pins that can be used to set or read the state of the digital input or output pins associated with the interface.

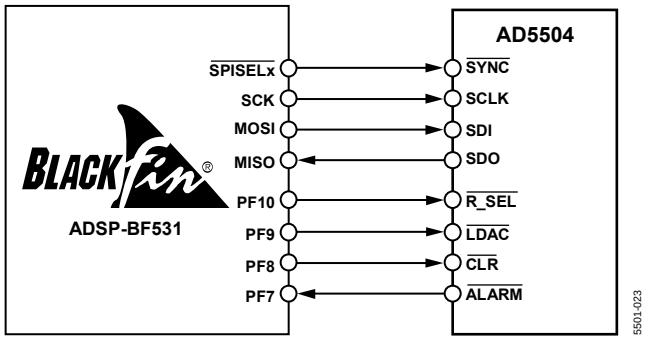

Figure 12. Interfacing to a Blackfin DSP

The Analog Devices ADSP-21065L is a floating point DSP with two serial ports (SPORTs). Figure 13 shows how one SPORT can be used to control the AD5504. In this example, the transmit frame synchronization (TFS) pin is connected to the receive frame synchronization (RFS) pin. The transmit and receive clocks (TCLK and RCLK) are also connected together. The user can write to the AD5504 by writing to the transmit register. If a read operation is being performed the data is clocked out of the AD5504 on the last 12 SCLKs. The DSP receive interrupt can be used to indicate when the read operation is complete.

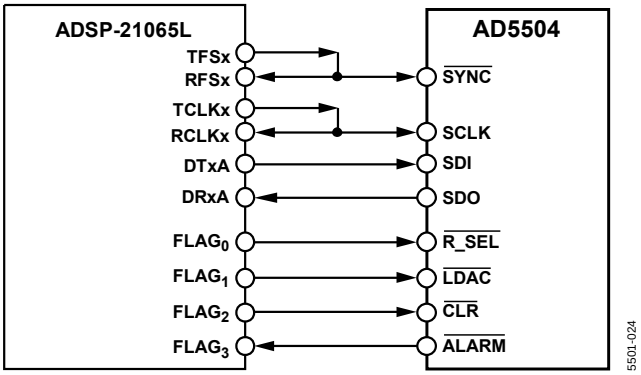

Figure 13. Interfacing to an ADSP-21065L DSP

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OUTLINE DIMENSIONS

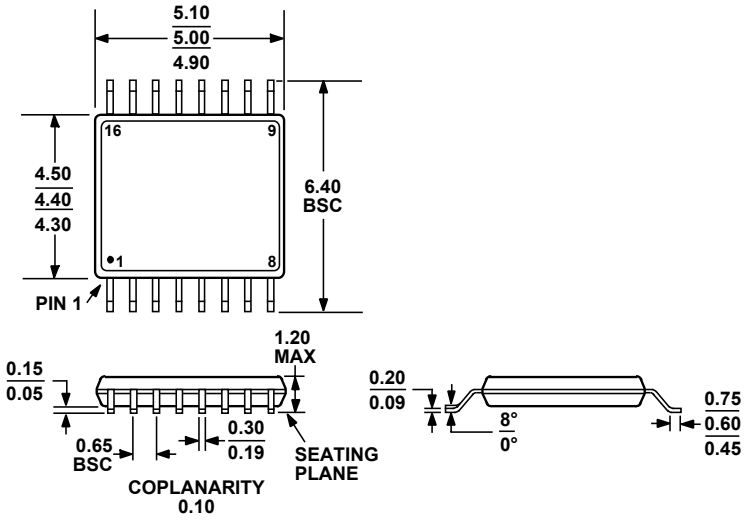

Figure 14. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)
Dimensions shown in millimeters

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PR07994-0-12/08(PrB)

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