ANALOG DEVICES

# Dual Ultrafast Voltage Comparator

## Preliminary Technical Data AD53519

**FEATURES**
**Robust Input Protection**
**300 ps Propagation Delay Input to Output**
**75 ps Propagation Delay Variation**
**Differential ECL Compatible Outputs**
**Differential Latch Control**
**Power Supply Rejection Greater than 70 dB**
**200ps Minimum Pulse Width (Bandwidth > 2.5 GHz)**
**5 Gbps Toggle Rate**
**Typical Output Rise/Fall of 150 ps**

**APPLICATIONS**
**Automatic Test Equipment**
**High Speed Instrumentation**
**Scope & Logic Analyzers Front End**
**Window Comparators**
**High Speed Line Receivers**
**Threshold Detection**
**Peak Detection**
**High Speed Triggers**
**Patient Diagnostics**
**Disk Drive Read Channel Detection**
**Hand-Held Test Instruments**
**Zero Crossing Detectors**
**Line Receivers & Signal Restoration**
**Clock Driver**
**Upgrade for SPT9689 Designs**
**Upgrade for AD96687 Designs**

**FUNCTIONAL BLOCK DIAGRAM**

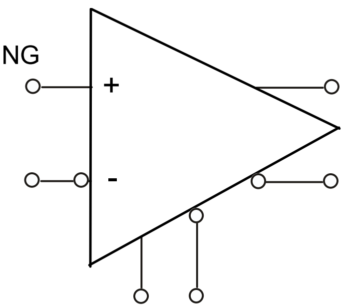


Figure 1

**GENERAL DESCRIPTION**

The AD53519 is an ultrafast voltage comparator fabricated on ADI's proprietary XFCB process. The device features 300 ps propagation delay with better than 75 ps overdrive dispersion. Dispersion is a particularly important characteristic of high speed comparators. It is a measure of the difference in propagation delay under differing overdrive conditions.

A fast, high precision differential input stage permits consistent propagation delay with a wide variety of signals in the common mode range from –2.0 V to +3.0 V. Outputs are complementary digital signals fully compatible with ECL 10 K and 10 KH logic families. The outputs provide sufficient drive current to directly drive transmission lines terminated in 50 Ω to –2 V. A latch input is included which permits tracking, track-hold, or sample-hold modes of operation.

The AD53519 is available in a 20-lead PLCC package.

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**AD53519 ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +5.0V, $V_{EE}$ = -5.2V, $T_A$ = +25°C unless otherwise noted)

| PARAMETER | SYMBOL | CONDITION | Min | Typ | Max | UNITS |
|---|---|---|---|---|---|---|
| **INPUT CHARACTERISTICS** | | | | | | |
| Input Offset Voltage | $V_{OS}$ | | -10.0 | ±3.0 | 10.0 | mV |
| Input Offset Voltage Channel Matching | | | | | | mV |
| Offset Voltage Tempco | $DV_{OS}/d_T$ | | | 10.0 | | µV/°C |
| Input Bias Current | $I_{BC}$ | | | ±16 | ±25.0 | µA |
| Input Bias Current Tempco | | | | | | nA/°C |
| Input Offset Current | | | | ±1.0 | ±3.0 | µA |
| Input Voltage Range | | | -2.0 | | 3.0 | V |
| Input Capacitance | $C_{IN}$ | | | | | pF |
| Input Resistance | $R_{ins}$ | | | | | kΩ |
| Input Resistance, Differential Mode | | | | 40 | | kΩ |
| Input Resistance, Common Mode | | | | | | kΩ |
| Input Common Mode Range | $V_{CM}$ | | -2.0 | | 3.0 | V |
| Open Loop Gain | | | | 60 | | dB |
| Common Mode Rejection Ratio | CMRR | $V_{CM}$ = -1.0 V to +3.0 V | | 70 | | dB |
| Input Differential Voltage | | | | | | V |
| Hysteresis Skew | | | | | | mV |
| | | | | | | |
| **ENABLE INPUT CHARACTERISTICS** | | | | | | |
| Latch Enable Common Mode Range | $V_{LCM}$ | | -2.0 | | 0 | V |
| Latch Enable Differential Input Voltage | $V_{LD}$ | | 0.4 | | 2.0 | V |
| Input HIGH Voltage | $V_{IH}$ | | | | | V |
| Input LOW Voltage | $V_{IL}$ | | | | | V |
| Input HIGH Current | | @ 0.0 Volts | | | | µA |
| Input LOW Current | | @ -2.0 Volts | | | | µA |
| Latch Set-up Time | $t_S$ | 250 mV Over Drive | | 150 | | ps |
| Latch to Output Rise Delay | $t_{PLOH}$ | 250 mV Over Drive | | 375 | | ps |
| Latch to Output Fall Delay | $t_{PLOL}$ | 250 mV Over Drive | | 375 | | ps |
| Latch Pulse Width | $t_{PL}$ | 250 mV Over Drive | | 150 | | ps |
| Latch Hold Time | $t_H$ | 250 mV Over Drive | | 0 | | ps |
| | | | | | | |
| **OUTPUT CHARACTERISTICS** | | | | | | |
| Output Voltage - High Level | $V_{OH}$ | ECL 50 Ohms to –2.0 V | -1.00 | | -0.81 | V |
| Output Voltage - Low Level | $V_{OL}$ | ECL 50 Ohms to –2.0 V | -1.95 | | -1.54 | V |
| | | | | | | |
| **SWITCHING PERFORMANCE** | | | | | | |
| Propagation Delay – Input to Output – Rise | $t_{PDR}$ | | | 300 | | ps |
| Propagation Delay – Input to Output – Fall | $t_{PDF}$ | | | 300 | | ps |

| | | | | | | |
|---|---|---|---|---|---|---|
| Propagation Delay – Input to Output – Rise | $t_{PDR}$ | 20 mV Over Drive | | 375 | | ps |
| Propagation Delay – Input to Output – Fall | $t_{PDF}$ | 20 mV Over Drive | | 375 | | ps |
| Propagation Delay – Tempco | | | | 2 | | ps/°C |
| Rise Time | $t_R$ | 20% to 80% | | 150 | | ps |
| Fall Time | $t_F$ | 20% to 80% | | 150 | | ps |
| Equivalent Bandwidth | BW | | | 2500 | | MHz |
| Toggle Rate | | | | 5 | | Gbps |
| Prop Delay vs. Duty Cycle | | | | 10 | | ps |
| Prop Delay vs. Duty Cycle Slow Edge | | | | 20 | | ps |
| Prop Delay vs. Over Drive (20mV to 1.5V) | | | | 75 | | ps |
| Prop Delay Skew | | | | | | ps |
| Dispersion - Slew Rate | | | | 25 | | ps |
| Within Device Skew, Channel to Channel Prop Delay Match | | | | | | ps |
| Prop Delay Dispersion Overdrive | | | | | | ps |
| Prop Delay Dispersion Common Mode Voltage | | | | | | ps |
| Prop Delay Dispersion Input Slew Rate | | | | | | ps |
| Prop Delay Dispersion Input Duty Cycle | | | | | | ps |
| Prop Delay Dispersion Input Pulse Width | | | | | | ps |
| Unit to Unit Prop Delay | | | | | | ps |
| Minimum Pulse Width - Pos | $PW_H$ | | | 200 | | ps |
| Minimum Pulse Width - Neg | $PW_L$ | | | 200 | | ps |
| | | | | | | |
| **POWER SUPPLY** | | | | | | |
| Positive Supply Current | $I_{VCC}$ | @ +5.0 Volts | | | | mA |
| Negative Supply Current | $I_{VEE}$ | @ -5.2 Volts | | | | mA |
| Positive Supply Voltage | VCC | Dual | 4.75 | 5.0 | 5.25 | V |
| Negative Supply Voltage | VEE | Dual | -4.96 | -5.2 | -5.45 | V |
| Power Dissipation | | Dual, Without Load | | | | mW |
| Power Dissipation | | Dual, With Load | | 550 | | mW |
| Power Supply Sensitivity – VCC | $PSS_{VCC}$ | | | 70 | | dB |
| Power Supply Sensitivity – VEE | $PSS_{VEE}$ | | | 70 | | dB |
| | | | | | | |

**NOTES:**

1. Under no circumstances should the input voltages exceed the supply voltages
2.

# AD53519

## ABSOLUTE MAXIMUM RATINGS

**Supply Voltages**
Positive Supply Voltage ($V_{CC}$ to GND)...............–0.5V to +6.0V
Negative Supply Voltage ($V_{EE}$ to GND) .............-6.0V to +0.5V
Ground Voltage Differential................................–0.5V to +0.5V

**Input Voltages**
Input Common Mode Voltage .............................–2.0V to +3.0V
Differential Input Voltage ...................................–3.0V to +3.0V
Input Voltage, Latch Controls .................................... VEE to 0V

**Output**
Output Current.....................................................................30mA

**Temperature**
Operating Temperature, ambient ............................ 0°C to +70°C
Operating Temperature, junction..................................... +150°C
Storage Temperature Range ............................. –65°C to +150°C
Lead Temperature (10 sec).............................................. +300°C

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ORDERING GUIDE

| | TEMP | Package |
|---|---|---|
| MODEL | RANGE | Description |
| AD53519JP | 0/+70°C | PLCC-20 |
| | | |

## AD53519 PIN DESCRIPTION

| PIN# | Name | Function |
|---|---|---|
| 1 | NC | No Connect. Leave pin unconnected. |
| 2 | QA | One of two complementary outputs for channel A. QA will be at logic HIGH if the analog voltage at the NONINVERTING INPUT is greater than the analog voltage at the INVERTING INPUT (provided the comparator is in the "compare" mode). See LATCH ENABLE channel A for additional information |
| 3 | /QA | One of two complementary outputs for channel A. /QA will be at logic LOW if the analog voltage at the NONINVERTING INPUT is greater than the analog voltage at the INVERTING INPUT (provided the comparator is in the "compare" mode). See LATCH ENABLE channel A for additional information. |
| 4 | GND | Analog ground. |
| 5 | LEA | One of two complementary inputs for channel A Latch Enable. In the "compare" mode (logic HIGH), the output will track changes at the input of the comparator. In the "latch" mode (logic LOW), the output will reflect the input state just prior to the comparator being placed in the "latch" mode. /LEA must be driven in conjunction with LEA. |
| 6 | NC | No Connect. Leave pin unconnected. |
| 7 | /LEA | One of two complementary inputs for channel A Latch Enable. In the "compare" mode (logic LOW), the output will track changes at the input of the comparator. In the "latch" mode (logic HIGH), the output will reflect the input state just prior to the comparator being placed in the "latch" mode. LEA must be driven in conjunction with /LEA. |
| 8 | $V_{EE}$ | Negative Supply Terminal |
| 9 | -INA | Inverting analog input of the differential input stage for channel A. The INVERTING A INPUT must be driven in conjunction with the NONINVERTING A INPUT. |
| 10 | +INA | Noninverting analog input of the differential input stage for channel A. The NONINVERTING A INPUT must be driven in conjunction with the INVERTING A INPUT. |
| 11 | NC | No Connect. Leave pin unconnected. |
| 12 | +INB | Noninverting analog input of the differential input stage for channel B. The NONINVERTING B INPUT must be driven in conjunction with the INVERTING B INPUT. |
| 13 | -INB | Inverting analog input of the differential input stage for channel B. The INVERTING B INPUT must be driven in conjunction with the NONINVERTING B INPUT. |
| 14 | $V_{CC}$ | Positive Supply Terminal. |
| 15 | /LEB | One of two complementary inputs for channel B Latch Enable. In the "compare" mode (logic LOW), the output will track changes at the input of the comparator. In the "latch" mode (logic HIGH), the output will reflect the input state just prior to the comparator being placed in the "latch" mode. LEB must be driven in conjunction with /LEB. |
| 16 | NC | No Connect. Leave pin unconnected. |
| 17 | LEB | One of two complementary inputs for channel B Latch Enable. In the "compare" mode (logic HIGH), the output will track changes at the input of the comparator. In the "latch" mode (logic LOW), the output will reflect the input state just prior to the comparator being placed in the "latch" mode. /LEB must be driven in conjunction with LEB. |
| 18 | GND | Analog ground. |
| 19 | /QB | One of two complementary outputs for channel B. /QB will be at logic LOW if the analog voltage at the NONINVERTING INPUT is greater than the analog voltage at the INVERTING INPUT (provided the comparator is in the "compare" mode). See LATCH ENABLE channel B for additional information |
| 20 | QB | One of two complementary outputs for channel B. QB will be at logic HIGH if the analog voltage at the NONINVERTING INPUT is greater than the analog voltage at the INVERTING INPUT (provided the comparator is in the "compare" mode). See LATCH ENABLE channel B for additional information |

## AD53519 PIN CONFIGURATION

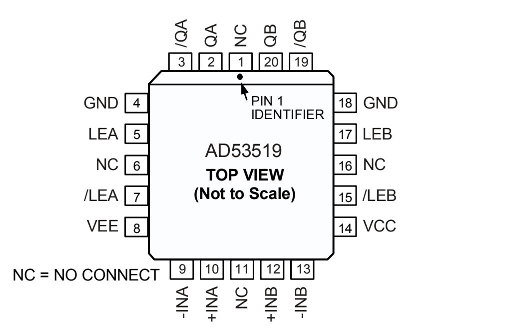



Figure 2

## TIMING INFORMATION

The timing diagram is presented to illustrate the AD53519 compare and latch features.

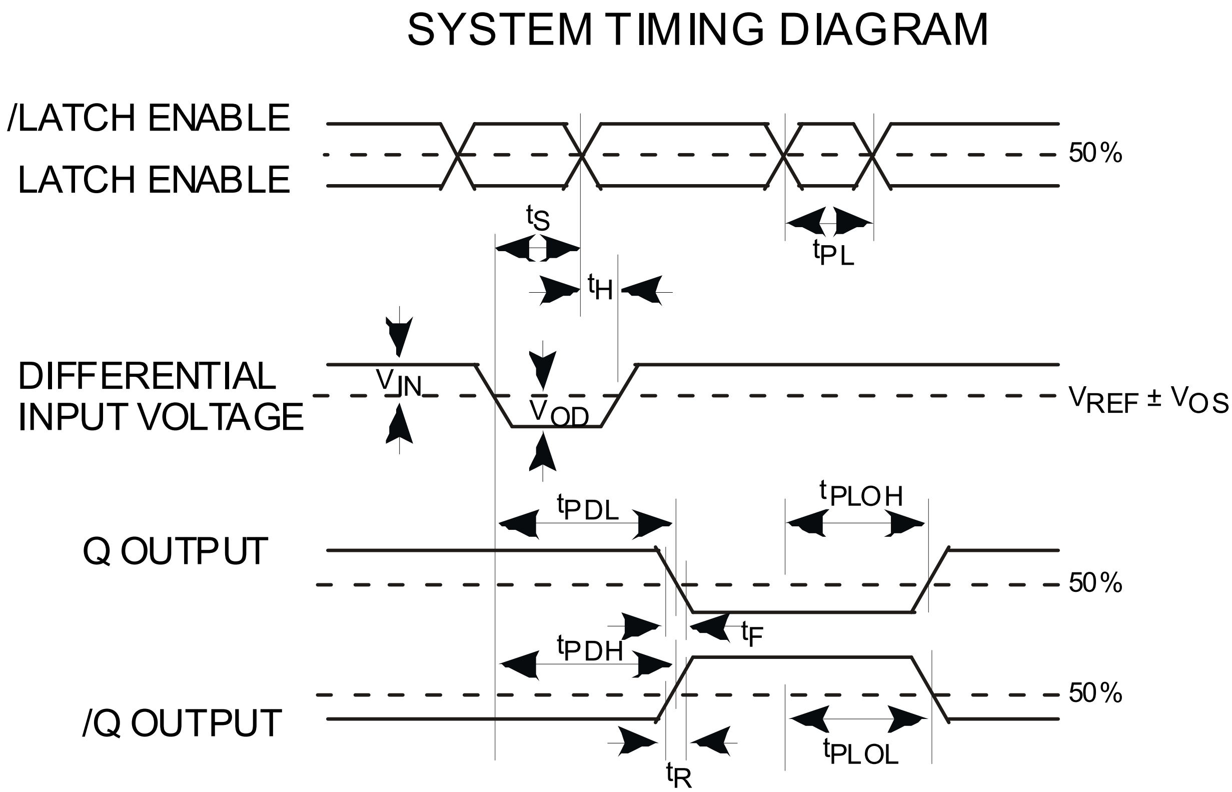



Figure 3

Terms used in timing diagrams:

| | | |
|---|---|---|
| $t_{PDH}$ | INPUT TO OUTPUT HIGH DELAY | The propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output LOW to HIGH transition |
| $t_{PDL}$ | INPUT TO OUTPUT LOW DELAY | The propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output HIGH to LOW transition |
| $t_{PLOH}$ | LATCH ENABLE TO OUTPUT HIGH DELAY | The propagation delay measure from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output LOW to HIGH transition |
| $t_{PLOL}$ | LATCH ENABLE TO OUTPUT LOW DELAY | The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output HIGH to LOW transition |
| $t_H$ | MINIMUM HOLD TIME | The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs |
| $t_{PL}$ | MINIMUM LATCH ENABLE PULSE WIDTH | The minimum time that the Latch Enable signal must be HIGH in order to acquire and input signal change |
| $t_S$ | MINIMUM SETUP TIME | The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs |
| $t_R$ | OUTPUT RISE TIME | The amount of time required to transition from a LOW to HIGH output as measured at the 20 and 80% points |
| $t_F$ | OUTPUT FALL TIME | The amount of time required to transition from a HIGH to LOW output as measured at the 20 and 80% points |
| $V_{OD}$ | VOLTAGE OVERDRIVE | The difference between the differential input and reference input voltages |
| | | |

## APPLICATIONS INFORMATION

The AD53519 comparators are very high speed devices. Consequently, high speed design techniques must be employed to achieve the best performance. The most critical aspect of any AD53519 design is the use of low impedance ground plane. A ground plane, as part of a multilayer board, is recommended for proper high speed performance. Using a continuous conductive plane over the surface of the circuit board can create this, only allowing breaks in the plane for necessary current paths. The ground plane provides a low inductance ground, eliminating any potential differences at different ground points throughout the circuit board caused by "ground bounce". A proper ground plane also minimizes the effects of stray capacitance on the circuit board.

It is also important to provide bypass capacitors for the power supply in a high speed application. A 1μF electrolytic bypass capacitor should be placed within 0.5 inches of each power supply pin to ground. These capacitors will reduce any potential voltage ripples from the power supply. In addition, a 10nF ceramic capacitor should be placed as close as possible from the power supply pins on the AD53519 to ground. These capacitors act as a charge reservoir for the device during high frequency switching.

The LATCH ENABLE input is active LOW (latched). If the latching function is not used, the LATCH ENABLE input should be grounded (ground is an ECL logic HIGH). The complimentary input, /LATCH ENABLE, should be tied to –2.0 V to disable the latching function.

Occasionally, one of the two comparator stages within the AD53519 will not be used. The inputs of the unused comparator should not be allowed to "float". The high internal gain may cause the output to oscillate (possibly affecting the other comparator which is being used) unless the output is forced into a fixed state. This is easily accomplished by insuring that the two inputs are at least one diode drop apart, while also appropriately connecting the LATCH ENABLE and /LATCH ENABLE inputs as described above.

The best performance will be achieved with the use of proper ECL terminations. The open-emitter outputs of the AD53519 are designed to be terminated through 50Ω resistors to –2.0 V, or any other equivalent ECL termination. If a –2.0 V supply is not available, an 82Ω resistor to ground and a 130Ω resistor to –5.2 V provides a suitable equivalent. If high speed ECL signals must be routed more than a centimeter, microstrip or stripline techniques may be required to insure proper transition times and prevent output ringing.

### Clock Timing Recovery

Comparators are often used in digital systems to recover clock timing signals. High-speed square waves transmitted over a distance, even tens of centimeters, can become distorted due to stray capacitance and inductance. Poor layout or improper termination can also cause reflections on the transmission line, further distorting the signal waveform. A high-speed comparator can be used to recover the distorted waveform while maintaining a minimum of delay.

## OPTIMIZING HIGH SPEED PERFORMANCE

As with any high speed comparator or amplifier, proper design and layout techniques should be used to ensure optimal performance from the AD53519. The performance limits of high speed circuitry can easily be a result of stray capacitance, improper ground impedance or other layout issues.

Minimizing resistance from source to the input is an important consideration in maximizing the high speed operation of the AD53519. Source resistance in combination with equivalent input capacitance could cause a lagged response at the input, thus delaying the output. The input capacitance of the AD53519 in combination with stray capacitance from an input pin to ground could result in several picofarads of equivalent capacitance. A combination of 3 kΩ source resistance and 5 pF of input capacitance yield a time constant of 15ns, which is significantly slower than the sub 500 ps capability of the AD53519. Source impedances should be significantly less than 100 Ω for best performance.

Sockets should be avoided due to stray capacitance and inductance. If proper high speed techniques are used, the AD53519 should be free from oscillation when the comparator input signal passes through the switching threshold.

## COMPARATOR PROPAGATION DELAY DISPERSION

The AD53519 has been specifically designed to reduce propagation delay dispersion over an input overdrive range of 100 mV to 1 V. Propagation delay dispersion is the change in propagation delay which results from a change in the degree of overdrive (how far the switching point is exceeded by the input). The overall result is a higher degree of timing accuracy since the AD53519 is far less sensitive to input variations than most comparator designs.

Propagation delay dispersion is a specification, which is important in critical timing application such as ATE, bench instruments and nuclear instrumentation. Dispersion is defined as the variation in propagation delay as the input overdrive conditions are changed. For the AD53519 dispersion is typically 50 ps as the overdrive is changed from 100 mV to 1 V. This specification applies for both positive and negative overdrive since the AD53519 has equal delays for positive and negative going inputs.

The 50 ps propagation delay dispersion of the AD53519 offers considerable improvement of the 100 ps dispersion of other similar series comparators.

PROPAGATION DELAY DISPERSION

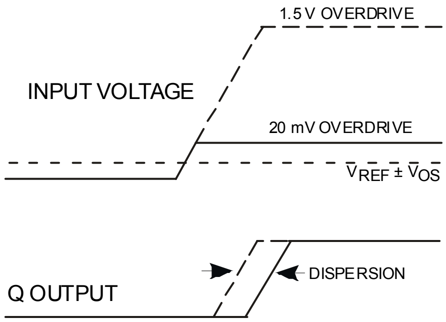



Figure 4

## COMPARATOR HYSTERESIS

The addition of hysteresis to a comparator is often useful in a noisy environment or where it is not desirable for the comparator to toggle between states when the input signal is at the switching threshold. The transfer function for a comparator with hysteresis is shown in Figure 4 below. If the input voltage approaches the threshold from the negative direction, the comparator will switch from a "0" to a "1" when the input crosses $+V_H/2$. The "new" switching threshold now becomes $-V_H/2$. The comparator will remain in a "1" state until the threshold $-V_H/2$ is crossed coming from the positive direction. In this manner, noise centered around 0 V input will not cause the comparator to switch states unless it exceeds the region bounded by $\pm V_H/2$.

Positive feedback from the output to the input is often used to produce hysteresis in a comparator.

COMPARATOR HYSTERESIS TRANSFER FUNCTION

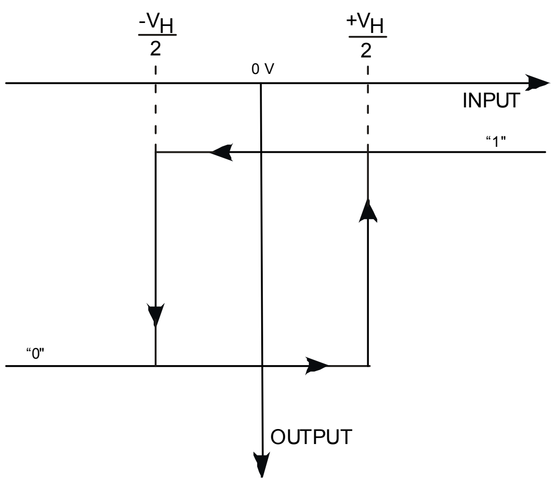



Figure 5

The customary technique for introducing hysteresis into a comparator uses positive feedback. The major problems with this approach are that the amount of hysteresis varies with the output logic levels resulting in a hysteresis that is not symmetrical around zero.

Another method to implement hysteresis is generated by introducing a differential voltage between LATCH ENABLE and /LATCH ENABLE as shown in Figure X.X. Hysteresis generated in this manner is independent of output swing and is symmetrical around zero. The variation of hysteresis with input voltage is shown in Figure 5.

COMPARATOR HYSTERESIS TRANSFER FUNCTION USING LATCH ENABLE INPUT

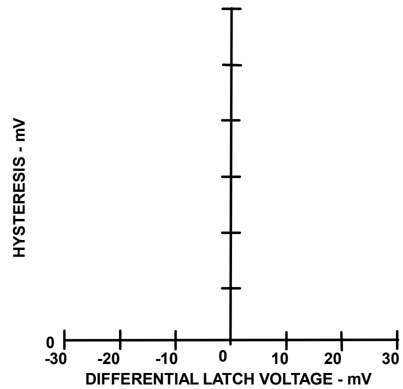



Figure 6

## THERMAL CONSIDERATIONS

The AD53519 PLCC package option has a theta JA (junction to ambient thermal resistance) of 89.4 °C /W in still air.

## Upgrading the SPT9689 and AD96687

The AD53519 dual comparator is pin-for-pin compatible with the SPT9689 and AD96687 and offers many improvements over these devices. The most notable difference is in propagation delay. The SPT9689 and AD96687 can be easily replaced with the higher performance AD53519, but there are differences and it is useful to check that these ensure proper operation.

The major differences between the SPT9689 and AD53519 include Propagation Delay, Latch to Output Delay, Bandwidth, Rise Time, Fall Time, Input Offset Voltage (SPT9689B) and Offset Voltage Tempco (SPT9689B).

## TYPCIAL APPLICATION CIRCUITS

HIGH SPEED SAMPLING CIRCUIT

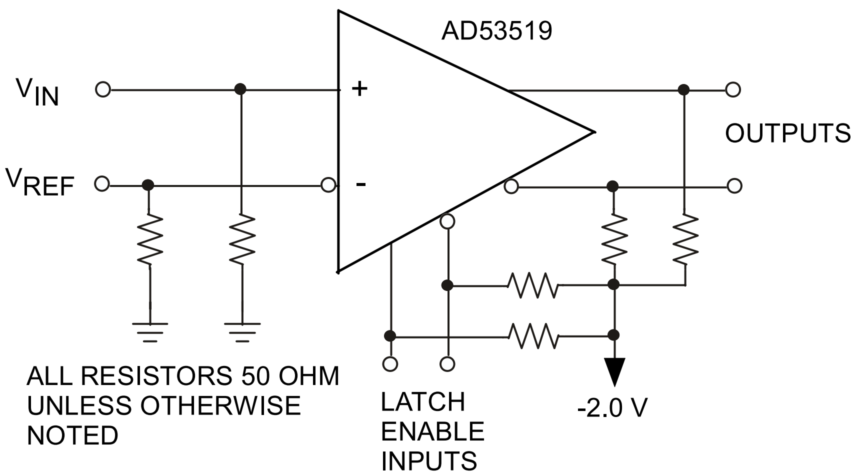
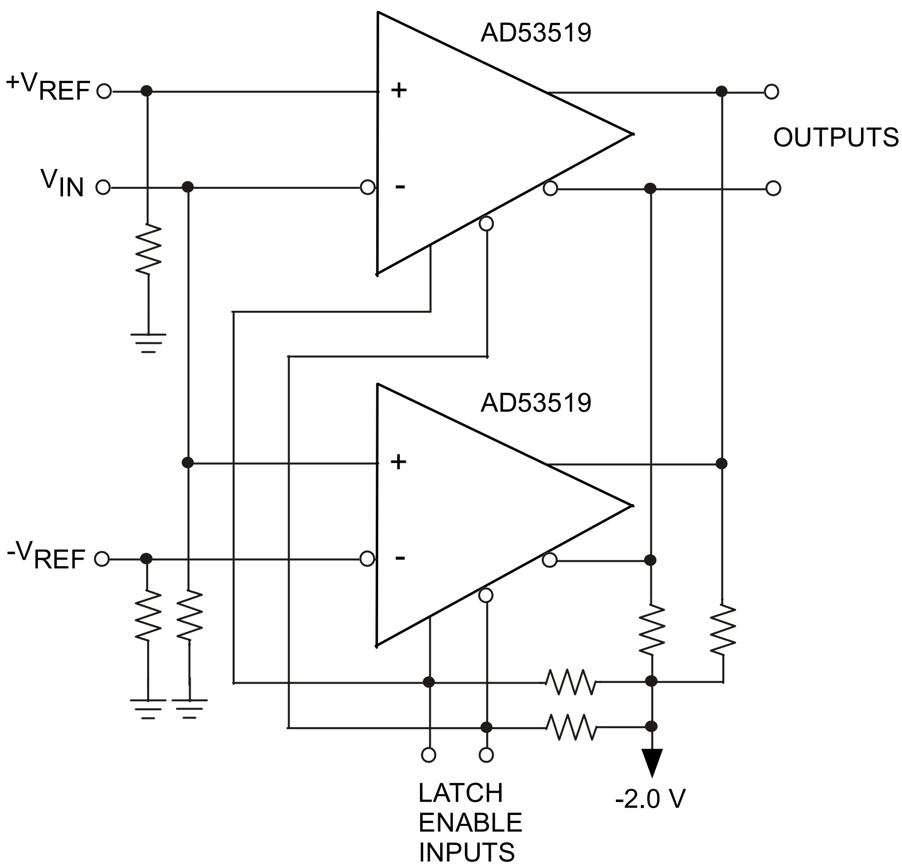



Figure 7

HIGH SPEED WINDOW COMPARATOR




ALL RESISTORS 50 OHM UNLESS OTHERWISE NOTED

Figure 8

HYSTERESIS USING POSITIVE FEEDBACK

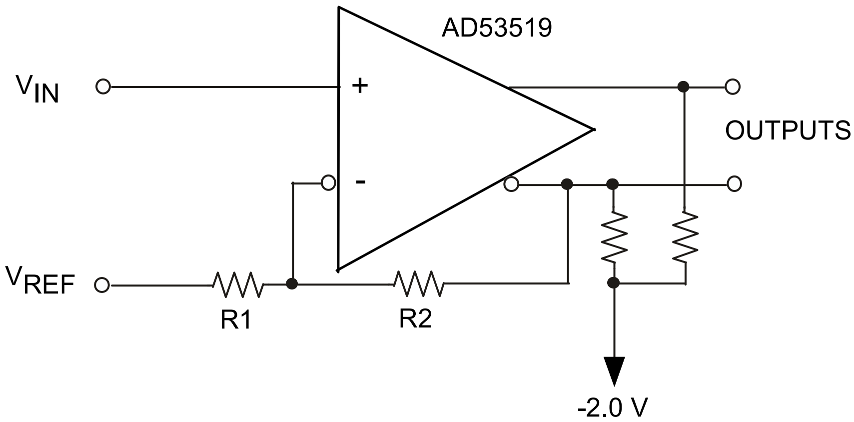



Figure 9

HYSTERESIS USING LATCH ENABLE INPUT

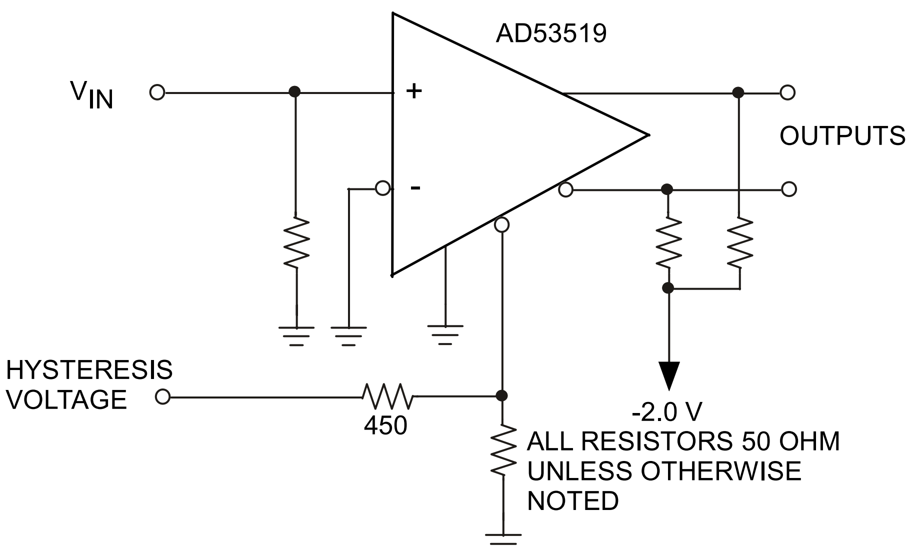



Figure 10

HOW TO INTERFACE AN ECL OUTPUT TO AN INSTRUMENT WITH A 50 OHM TO GROUND INPUT

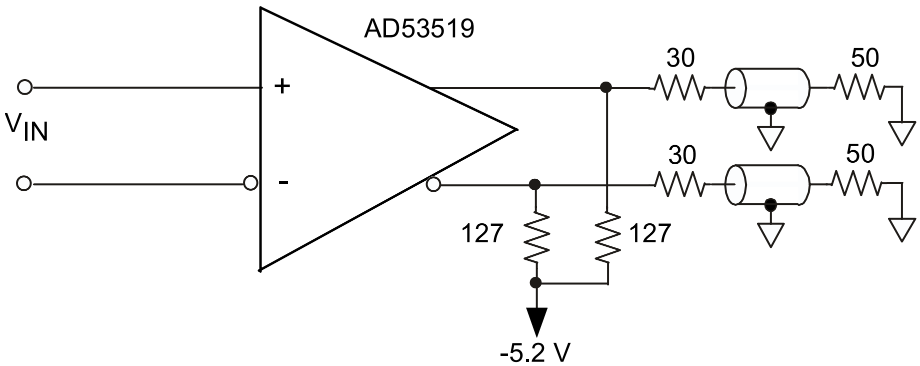



Figure 11

## ESD PROTECTION CIRCUITS

All input and output pins contain ADI Proprietary ESD protection diodes.

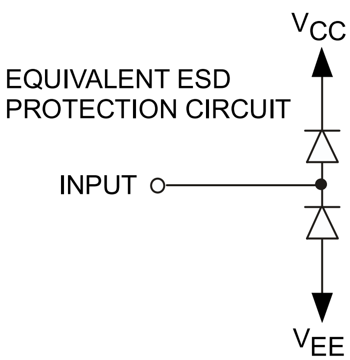
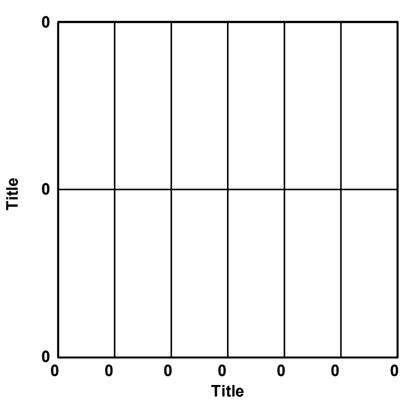



Figure 12

**ESD WARNING!!! ESD (Electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD53519 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.**

**TYPICAL PERFORMANCE CHARACTERISTICS** ($V_{CC}$ = +5.0V, $V_{EE}$ = -5.20V, $T_A$ = +25°C UNLESS OTHERWISE NOTED)




POSSIBLE CHARTS TO BE ADDED.

- **Propagation Delay vs. Overdrive Voltage**
- **Propagation Delay vs. Temperature**
- **Propagation Delay vs. Common Mode Voltage**
- **Rise Time vs. Temperature**
- **Hysteresis vs. ΔLatch**
- **Rise and Fall of Outputs vs. Time Crossover**
- **Fall Time vs. Temperature**
- **Input Bias Current vs. Common Mode Voltage**
- **Input Bias Current vs. Input Voltage**
- **Input Bias Current vs. Temperature**
- **Input Offset Voltage vs. Temperature**

## Mechanical Outline Dimensions

Dimensions shown in inches and (mm).

### 20-Pin PLCC