

# Voltage to Frequency Converter

# AD537

### 1.0 SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. <u>http://www.analog.com/aerospace</u>

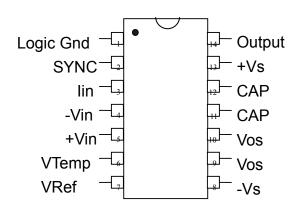
This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at <u>www.analog.com/AD537</u>

2.0 **Part Number**. The complete part number(s) of this specification follow:

Part NumberDescriptionAD537-703DVoltage to Frequency Converter with 0 to 150kHz frequency range

### 2.1 Case Outline.

LetterDescriptive designatorCase Outline (Lead Finish per MIL-PRF-38535)XGDIP1-T14 or CDIP2-T1414-Lead side-brazed ceramic dual-in-line package





3.0	Absolute Maximum Ratings. ( $T_A = 25^{\circ}C$ , unless otherwise noted)		
	Voltage, Rated Performance Single Supply	4.5 to 36V	
	Voltage, Rated Performance Dual Supply	$\dots \pm 5V$ to $\pm 18V$	
	Operating Temperature Range	55°C to +125°C	
	Storage Temperature Range	65°C to +150°C	
	Lead Temperature (Soldering, 10 sec.)	+300°C	

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#### **Thermal Characteristics:** 3.1

Thermal Resistance, 14 DIP (X) Package Junction-to-Case ( $\Theta_{JC}$ ) = 25°C/W Max Junction-to-Ambient ( $\Theta_{JA}$ ) = 95°C/W Max

#### **4.0** Table I. Electrical Table:

		Table I				
Parameter	Symbol	Conditions	Sub-	Limit	Limit	Units
See notes at end of table		Note 1/	group	Min	Max	
Frequency Range	Fo		1	0	150	Khz
Linearity Error (Nonlinearity)	LE	$F_o = 10 Khz$	1		0.07	%
Ellicanty Error (Nonlinearity)	LD	$F_o = 100 Khz$	4		0.1	%
Gain Error (Full-Scale Calibration Error)	$\mathbf{A}_{\mathrm{E}}$	C=0.01uF, Iin=1.00mA	1	-5	5	%
Gain vs. Supply	$\Delta A_{\rm E} / \Delta V s$	$F_0 = 10 Khz, 15 V < Vs < 20 V$	1		0.1	%/V
Gain Drift		+25C to +125C	2	-250	250	ppm/C
Gain Dint	$\Delta A_E / \Delta T$	+25C to -55C	3	-250	250	
Voltage Input Range	V <sub>IR</sub>	Vs Single Supply	1	0	+Vs-4	V
Voltage input Kange	V IR	Vs Dual Supply	1	-Vs	+Vs-4	V
Input Bias Current	I <sub>IB</sub>		1	-100	+100	nA
Input Resistance 4/	R <sub>I</sub>			250		Mohms
Input Offset Voltage 2/	V <sub>os</sub>		1		2	mV
Offset vs. Supply	$\Delta V_{os}/\Delta Vs$	15V <vs<20v< td=""><td>1</td><td></td><td>100</td><td>uV/V</td></vs<20v<>	1		100	uV/V
Offset Drift	$\Delta V_{os} / \Delta T$	+25C to +125C	2	-10	10	uV/C
		+25C to -55C	3	-10	10	
Voltage Ref Absolute Value 3/	V <sub>REF</sub>		1	-5	5	%
V <sub>REF</sub> vs. Temp	$\Delta \mathrm{V_{REF}}$ /	+25C to +125C	2	-100	100	ppm/C
v <sub>REF</sub> vs. remp	$\Delta T$	+25C to -55C	3	-100	100	ppm/C
V <sub>REF</sub> vs. Supply	$\Delta V_{REF}$ /	15V <vs<35v< td=""><td>1</td><td></td><td>0.03</td><td>%/V</td></vs<35v<>	1		0.03	%/V
V <sub>REF</sub> vs. Suppry	$\Delta Vs$				0.03	70/ V
Initial Calibration - Absolute	V		1	278	318	mV
Temperature Reference	V <sub>Temp</sub>					111 V
Output Voltage Logic Low	V <sub>OL</sub>	$I_{SINK} = 10 mA$	1,2,3		0.4	V
Output Leakage Current	I <sub>OH</sub>	Logic 1	1,2,3		2	uA
Quiescent Current	I <sub>S</sub>	Vs = 5V & 36V	1,2,3		2.5	mA

#### TABLE I NOTES:

- Ta = +25C,  $V_S = +15V$ , C = 0.01uF unless otherwise noted
- $\frac{\frac{1}{2}}{\frac{3}{4}}$ Trimmable for 14 pin DIP package only.
- Nominal value 1.00V.
- Guaranteed by design

#### 4.1 Table II. Electrical Test Requirements:

Table II	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3, 4 <u>1</u> / <u>2</u> /
Group A Test Requirements	1, 2, 3, 4
Group C end-point electrical parameters	1 <u>2</u> /
Group D end-point electrical parameters	1
Group E end-point electrical parameters	N/A

Notes:

1/ PDA applies to subgroup 1. Delta's excluded from PDA.

2/ See table III for delta limits.

	-	Table III		
TEST TITLE	BURN-IN ENDPOINT	LIFETEST ENDPOINT	DELTA LIMIT	UNITS
Is@15V	2.5	2.5	±0.3	mA
Vos	2	2	±1	mV

#### 4.2 Table III. Burn-in test delta limits.

#### 5.0 Life Test/Burn-In Circuit:

- 5.1 HTRB is not applicable for this drawing.
- 5.2 Burn-in is per MIL-STD-883 Method 1015 test condition B.
- 5.3 Steady state life test is per MIL-STD-883 Method 1005, test condition B.

### 6.0 MIL-STD-38535 QMLV exceptions:

**6.1** Full WLA per MIL-STD-883 TM 5007 is not available for this product. SEM Inspection only is available per MIL-STD-883, TM2018.

## AD537

Rev	Description of Change	Date
Α	Initiate	July 17, 2007
В	Update header/footer and add to 1.0 Scope description.	March 6, 2008

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