2.5 V to 5.5 V, 115 μA, Parallel Interface Single Voltage-Output 8-/10-/12-Bit DACs

AD5330/AD5331/AD5340/AD5341*

FEATURES

AD5330: Single 8-Bit DAC in 20-Lead TSSOP
AD5331: Single 10-Bit DAC in 20-Lead TSSOP
AD5340: Single 12-Bit DAC in 24-Lead TSSOP
AD5341: Single 12-Bit DAC in 20-Lead TSSOP
Low Power Operation: 115 μA @ 3 V, 140 μA @ 5 V
Power-Down to 80 nA @ 3 V, 200 nA @ 5 V via $\overline{PD}$ Pin
2.5 V to 5.5 V Power Supply
Double-Buffered Input Logic
Guaranteed Monotonic by Design Over All Codes
Buffered/Unbuffered Reference Input Options
Output Range: 0–V_{REF} or 0–2 V_{REF}
Power-On Reset to Zero Volts
Simultaneous Update of DAC Outputs via $\overline{LDAC}$ Pin
Asynchronous $\overline{CLR}$ Facility
Low Power Parallel Data Interface
On-Chip Rail-to-Rail Output Buffer Amplifiers
Temperature Range: –40°C to +105°C

APPLICATIONS

Portable Battery-Powered Instruments
Digital Gain and Offset Adjustment
Programmable Voltage and Current Sources
Programmable Attenuators
Industrial Process Control

GENERAL DESCRIPTION

The AD5330/AD5331/AD5340/AD5341 are single 8-, 10-, and 12-bit DACs. They operate from a 2.5 V to 5.5 V supply consuming just 115 μA at 3 V, and feature a power-down mode that further reduces the current to 80 nA. These devices incorporate an on-chip output buffer that can drive the output to both supply rails, while the AD5330, AD5340, and AD5341 allow a choice of buffered or unbuffered reference input.

The AD5330/AD5331/AD5340/AD5341 have a parallel interface. $\overline{CS}$ selects the device and data is loaded into the input registers on the rising edge of $\overline{WR}$.

The GAIN pin allows the output range to be set at 0 V to V_{REF} or 0 V to $2 \times V_{REF}$.

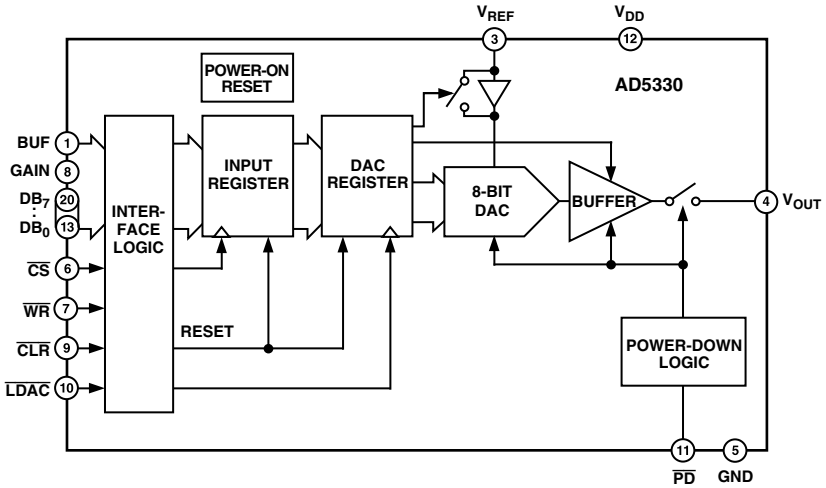
Input data to the DACs is double-buffered, allowing simultaneous update of multiple DACs in a system using the $\overline{LDAC}$ pin.

An asynchronous $\overline{CLR}$ input is also provided, which resets the contents of the Input Register and the DAC Register to all zeros. These devices also incorporate a power-on reset circuit that ensures that the DAC output powers on to 0 V and remains there until valid data is written to the device.

The AD5330/AD5331/AD5340/AD5341 are available in Thin Shrink Small Outline Packages (TSSOP).

AD5330 FUNCTIONAL BLOCK DIAGRAM

(Other Diagrams Inside)



*Protected by U.S. Patent Number 5,969,657; other patents pending.

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703
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AD5330/AD5331/AD5340/AD5341–SPECIFICATIONS

(V_{DD} = 2.5 V to 5.5 V, V_{REF} = 2 V. R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter[1]	B Version[2] Min	Typ	Max	Unit	Conditions/Comments
DC PERFORMANCE[3, 4]					
AD5330					
Resolution		8		Bits	
Relative Accuracy		±0.15	±1	LSB	
Differential Nonlinearity		±0.02	±0.25	LSB	Guaranteed Monotonic By Design Over All Codes
AD5331					
Resolution		10		Bits	
Relative Accuracy		±0.5	±4	LSB	
Differential Nonlinearity		±0.05	±0.5	LSB	Guaranteed Monotonic By Design Over All Codes
AD5340/AD5341					
Resolution		12		Bits	
Relative Accuracy		±2	±16	LSB	
Differential Nonlinearity		±0.2	±1	LSB	Guaranteed Monotonic By Design Over All Codes
Offset Error		±0.4	±3	% of FSR	
Gain Error		±0.15	±1	% of FSR	
Lower Deadband[5]		10	60	mV	Lower Deadband Exists Only if Offset Error Is Negative
Upper Deadband		10	60	mV	V_{DD} = 5 V. Upper Deadband Exists Only if $V_{REF} = V_{DD}$
Offset Error Drift[6]		–12		ppm of FSR/°C	
Gain Error Drift[6]		–5		ppm of FSR/°C	
DC Power Supply Rejection Ratio[6]		–60		dB	ΔV_{DD} = ±10%
DAC REFERENCE INPUT[6]					
V_{REF} Input Range	1		V_{DD}	V	Buffered Reference (AD5330, AD5340, and AD5341)
	0.25		V_{DD}	V	Unbuffered Reference
V_{REF} Input Impedance		>10		MΩ	Buffered Reference (AD5330, AD5340, and AD5341)
		180		kΩ	Unbuffered Reference. Gain = 1, Input Impedance = R_{DAC}
		90		kΩ	Unbuffered Reference. Gain = 2, Input Impedance = R_{DAC}
Reference Feedthrough		–90		dB	Frequency = 10 kHz
OUTPUT CHARACTERISTICS[6]					
Minimum Output Voltage[4, 7]		0.001		V min	Rail-to-Rail Operation
Maximum Output Voltage[4, 7]		V_{DD}–0.001		V max	
DC Output Impedance		0.5		Ω	
Short Circuit Current		25		mA	V_{DD} = 5 V
		15		mA	V_{DD} = 3 V
Power-Up Time		2.5		µs	Coming Out of Power-Down Mode. V_{DD} = 5 V
		5		µs	Coming Out of Power-Down Mode. V_{DD} = 3 V
LOGIC INPUTS[6]					
Input Current		±1		µA	
V_{IL}, Input Low Voltage			0.8	V	V_{DD} = 5 V ± 10%
			0.6	V	V_{DD} = 3 V ± 10%
			0.5	V	V_{DD} = 2.5 V
V_{IH}, Input High Voltage	2.4			V	V_{DD} = 5 V ± 10%
	2.1			V	V_{DD} = 3 V ± 10%
	2.0			V	V_{DD} = 2.5 V
Pin Capacitance		3		pF	
POWER REQUIREMENTS					
V_{DD}	2.5		5.5	V	
I_{DD} (Normal Mode)					DACs active and excluding load currents. Unbuffered
V_{DD} = 4.5 V to 5.5 V		140	250	µA	Reference. $V_{IH} = V_{DD}$, V_{IL} = GND.
V_{DD} = 2.5 V to 3.6 V		115	200	µA	I_{DD} increases by 50 µA at $V_{REF} > V_{DD}$ – 100 mV. In Buffered Mode extra current is (5 + V_{REF}/R_{DAC}) µA, where R_{DAC} is the resistance of the resistor string.
I_{DD} (Power-Down Mode)					
V_{DD} = 4.5 V to 5.5 V		0.2	1	µA	
V_{DD} = 2.5 V to 3.6 V		0.08	1	µA	

NOTES

[1]See Terminology section.

[2]Temperature range: B Version: –40°C to +105°C; typical specifications are at 25°C.

[3]Linearity is tested using a reduced code range: AD5330 (Code 8 to 255); AD5331 (Code 28 to 1023); AD5340/AD5341 (Code 115 to 4095).

[4]DC specifications tested with output unloaded.

[5]This corresponds to x codes. x = Deadband voltage/LSB size.

[6]Guaranteed by design and characterization, not production tested.

[7]In order for the amplifier output to reach its minimum voltage, Offset Error must be negative. In order for the amplifier output to reach its maximum voltage, $V_{REF} = V_{DD}$ and "Offset plus Gain" Error must be positive.

Specifications subject to change without notice.

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AC CHARACTERISTICS[1] (V_{DD} = 2.5 V to 5.5 V. R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter[2]	B Version[3] Min	Typ	Max	Unit	Conditions/Comments
Output Voltage Settling Time					V_{REF} = 2 V. See Figure 20
AD5330		6	8	µs	1/4 Scale to 3/4 Scale Change (40 H to C0 H)
AD5331		7	9	µs	1/4 Scale to 3/4 Scale Change (100 H to 300 H)
AD5340		8	10	µs	1/4 Scale to 3/4 Scale Change (400 H to C00 H)
AD5341		8	10	µs	1/4 Scale to 3/4 Scale Change (400 H to C00 H)
Slew Rate		0.7		V/µs	
Major Code Transition Glitch Energy		6		nV-s	1 LSB Change Around Major Carry
Digital Feedthrough		0.5		nV-s	
Multiplying Bandwidth		200		kHz	V_{REF} = 2 V ± 0.1 V p-p. Unbuffered Mode
Total Harmonic Distortion		–70		dB	V_{REF} = 2.5 V ± 0.1 V p-p. Frequency = 10 kHz

NOTES
[1]Guaranteed by design and characterization, not production tested.
[2]See Terminology section.
[3]Temperature range: B Version: –40°C to +105°C; typical specifications are at 25°C.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2, 3] (V_{DD} = 2.5 V to 5.5 V, All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Condition/Comments
t_1	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_3	20	ns min	$\overline{WR}$ Pulsewidth
t_4	5	ns min	Data, GAIN, BUF, HBEN Setup Time
t_5	4.5	ns min	Data, GAIN, BUF, HBEN Hold Time
t_6	5	ns min	Synchronous Mode. $\overline{WR}$ Falling to $\overline{LDAC}$ Falling.
t_7	5	ns min	Synchronous Mode. $\overline{LDAC}$ Falling to $\overline{WR}$ Rising.
t_8	4.5	ns min	Synchronous Mode. $\overline{WR}$ Rising to $\overline{LDAC}$ Rising.
t_9	5	ns min	Asynchronous Mode. $\overline{LDAC}$ Rising to $\overline{WR}$ Rising.
t_{10}	4.5	ns min	Asynchronous Mode. $\overline{WR}$ Rising to $\overline{LDAC}$ Falling.
t_{11}	20	ns min	$\overline{LDAC}$ Pulsewidth
t_{12}	20	ns min	$\overline{CLR}$ Pulsewidth
t_{13}	50	ns min	Time Between $\overline{WR}$ Cycles

NOTES
[1]Guaranteed by design and characterization, not production tested.
[2]All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
[3]See Figure 1.

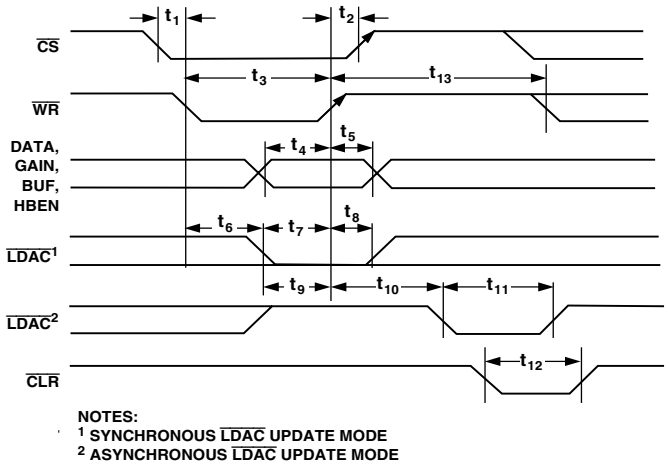

Figure 1. Parallel Interface Timing Diagram

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ABSOLUTE MAXIMUM RATINGS*
(T_A = 25°C unless otherwise noted)

V_{DD} to GND . . . . . –0.3 V to +7 V
Digital Input Voltage to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to GND . . . . –0.3 V to V_{DD} + 0.3 V
V_{OUT} to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Industrial (B Version) . . . . . –40°C to +105°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . 150°C
TSSOP Package
Power Dissipation . . . . . (T_J max – T_A)/θ_{JA} mW
θ_{JA} Thermal Impedance (20-Lead TSSOP) . . . . . 143°C/W
θ_{JA} Thermal Impedance (24-Lead TSSOP) . . . . . 128°C/W
θ_{JA} Thermal Impedance (20-Lead TSSOP) . . . . . 45°C/W
θ_{JC} Thermal Impedance (24-Lead TSSOP) . . . . . 42°C/W
Reflow Soldering
Peak Temperature . . . . . 220 +5/–0°C
Time at Peak Temperature . . . . . 10 sec to 40 sec

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD5330BRU	–40°C to +105°C	TSSOP (Thin Shrink Small Outline Package)	RU-20
AD5331BRU	–40°C to +105°C	TSSOP (Thin Shrink Small Outline Package)	RU-20
AD5340BRU	–40°C to +105°C	TSSOP (Thin Shrink Small Outline Package)	RU-24
AD5341BRU	–40°C to +105°C	TSSOP (Thin Shrink Small Outline Package)	RU-20

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5330/AD5331/AD5340/AD5341 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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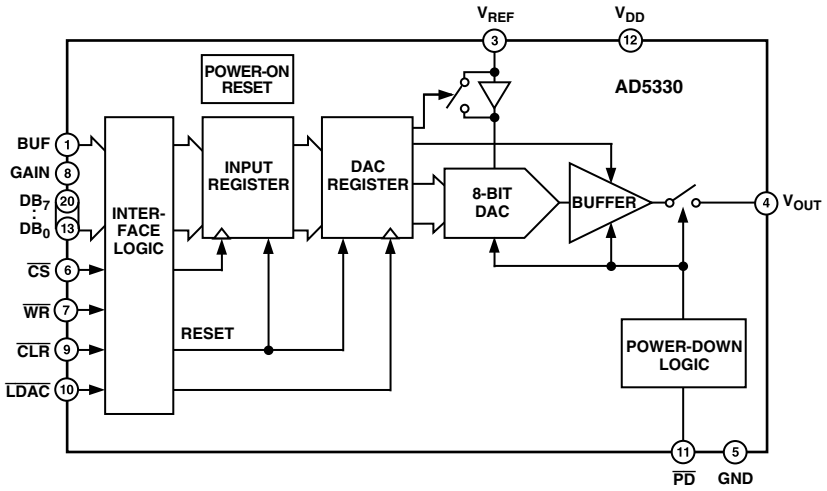
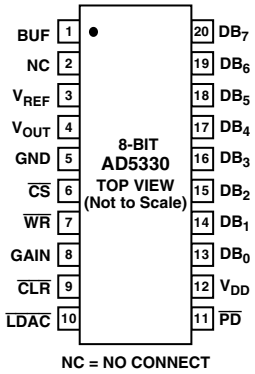
AD5330 FUNCTIONAL BLOCK DIAGRAM



AD5330 PIN CONFIGURATION



AD5330 PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	BUF	Buffer Control Pin. This pin controls whether the reference input to the DAC is buffered or unbuffered.
2	NC	No Connect.
3	V_{REF}	Reference Input.
4	V_{OUT}	Output of DAC. Buffered output with rail-to-rail operation.
5	GND	Ground reference point for all circuitry on the part.
6	$\overline{CS}$	Active Low Chip Select Input. This is used in conjunction with $\overline{WR}$ to write data to the parallel interface.
7	$\overline{WR}$	Active Low Write Input. This is used in conjunction with $\overline{CS}$ to write data to the parallel interface.
8	GAIN	Gain Control Pin. This controls whether the output range from the DAC is 0–V_{REF} or 0–2 V_{REF}.
9	$\overline{CLR}$	Asynchronous active low control input that clears all input registers and DAC registers to zero.
10	$\overline{LDAC}$	Active low control input that updates the DAC registers with the contents of the input registers.
11	$\overline{PD}$	Power-Down Pin. This active low control pin puts the DAC into power-down mode.
12	V_{DD}	Power Supply Input. These parts can operate from 2.5 V to 5.5 V and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
13–20	DB_0–DB_7	Eight Parallel Data Inputs. DB_7 is the MSB of these eight bits.

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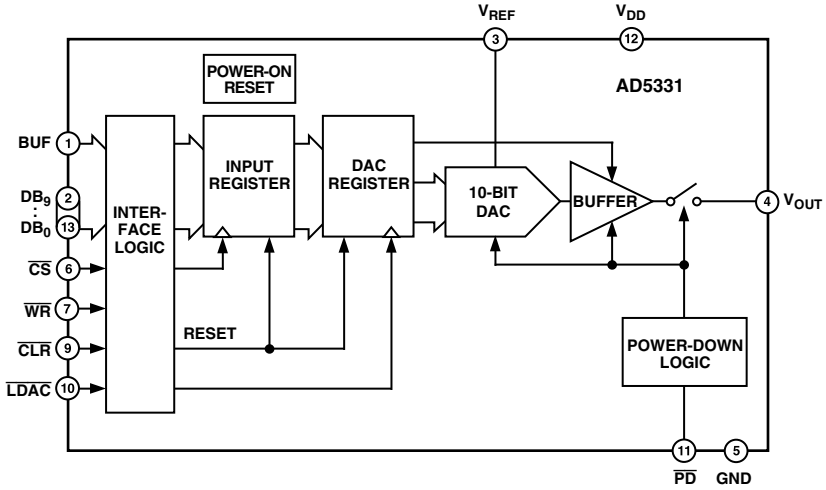
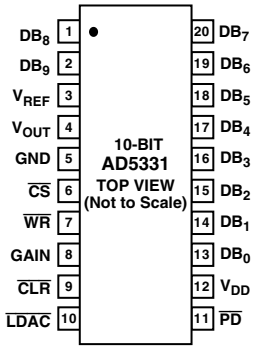
AD5331 FUNCTIONAL BLOCK DIAGRAM



AD5331 PIN CONFIGURATION



AD5331 PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	DB_8	Parallel Data Input.
2	DB_9	Most Significant Bit of Parallel Data Input.
3	V_{REF}	Unbuffered Reference Input.
4	V_{OUT}	Output of DAC. Buffered output with rail-to-rail operation.
5	GND	Ground reference point for all circuitry on the part.
6	$\overline{CS}$	Active Low Chip Select Input. This is used in conjunction with $\overline{WR}$ to write data to the parallel interface.
7	$\overline{WR}$	Active Low Write Input. This is used in conjunction with $\overline{CS}$ to write data to the parallel interface.
8	GAIN	Gain Control Pin. This controls whether the output range from the DAC is 0–V_{REF} or 0–2 V_{REF}.
9	$\overline{CLR}$	Active low control input that clears all input registers and DAC registers to zero.
10	$\overline{LDAC}$	Active low control input that updates the DAC registers with the contents of the input registers.
11	$\overline{PD}$	Power-Down Pin. This active low control pin puts the DAC into power-down mode.
12	V_{DD}	Power Supply Input. These parts can operate from 2.5 V to 5.5 V and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
13–20	DB_0–DB_7	Eight Parallel Data Inputs.

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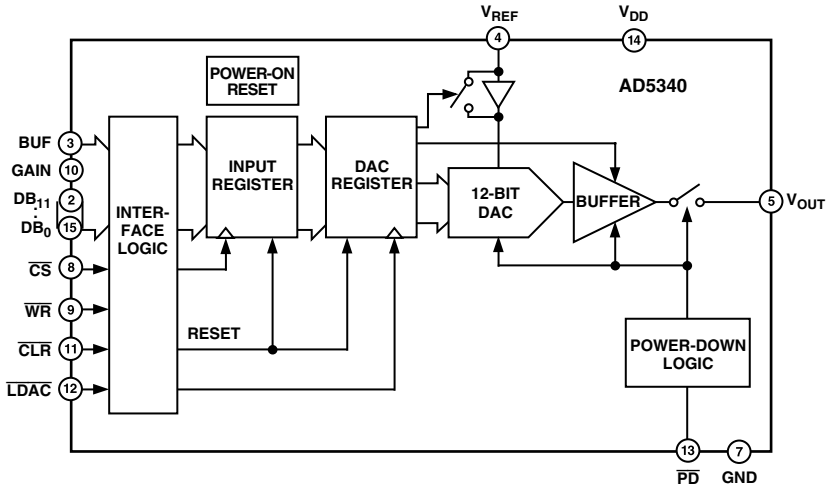
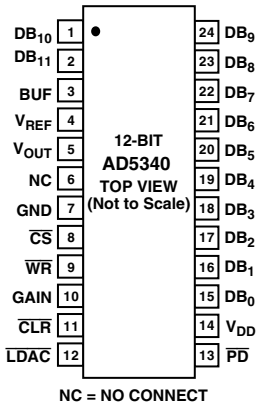
AD5340 FUNCTIONAL BLOCK DIAGRAM



AD5340 PIN CONFIGURATION



NC = NO CONNECT

AD5340 PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	DB_{10}	Parallel Data Input.
2	DB_{11}	Most Significant Bit of Parallel Data Input.
3	BUF	Buffer Control Pin. This pin controls whether the reference input to the DAC is buffered or unbuffered.
4	V_{REF}	Reference Input.
5	V_{OUT}	Output of DAC. Buffered output with rail-to-rail operation.
6	NC	No Connect.
7	GND	Ground reference point for all circuitry on the part.
8	$\overline{CS}$	Active Low Chip Select Input. This is used in conjunction with $\overline{WR}$ to write data to the parallel interface.
9	$\overline{WR}$	Active Low Write Input. This is used in conjunction with $\overline{CS}$ to write data to the parallel interface.
10	GAIN	Gain Control Pin. This controls whether the output range from the DAC is 0–V_{REF} or 0–2 V_{REF}.
11	$\overline{CLR}$	Asynchronous active low control input that clears all input registers and DAC registers to zero.
12	$\overline{LDAC}$	Active low control input that updates the DAC registers with the contents of the input registers.
13	$\overline{PD}$	Power-Down Pin. This active low control pin puts the DAC into power-down mode.
14	V_{DD}	Power Supply Input. These parts can operate from 2.5 V to 5.5 V and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
15–24	DB_0–DB_9	10 Parallel Data Inputs.

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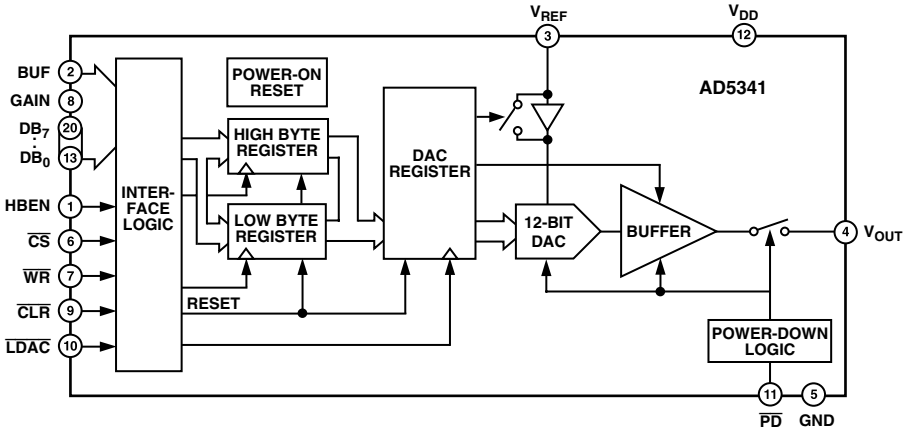
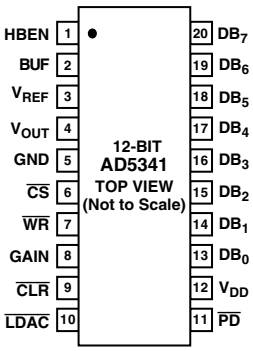
AD5341 FUNCTIONAL BLOCK DIAGRAM



AD5341 PIN CONFIGURATION



AD5341 PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	HBEN	High Byte Enable Pin. This pin is used when writing to the device to determine if data is written to the high byte register or the low byte register.
2	BUF	Buffer Control Pin. This pin controls whether the reference input to the DAC is buffered or unbuffered.
3	V_{REF}	Reference Input.
4	V_{OUT}	Output of DAC. Buffered output with rail-to-rail operation.
5	GND	Ground reference point for all circuitry on the part.
6	$\overline{CS}$	Active low Chip Select Input. This is used in conjunction with $\overline{WR}$ to write data to the parallel interface.
7	$\overline{WR}$	Active Low Write Input. This is used in conjunction with $\overline{CS}$ to write data to the parallel interface.
8	GAIN	Gain Control Pin. This controls whether the output range from the DAC is 0–V_{REF} or 0–2 $V_{REF.}$
9	$\overline{CLR}$	Asynchronous active low control input that clears all input registers and DAC registers to zero.
10	$\overline{LDAC}$	Active low control input that updates the DAC registers with the contents of the input registers.
11	$\overline{PD}$	Power-Down Pin. This active low control pin puts the DAC into power-down mode.
12	V_{DD}	Power Supply Input. These parts can operate from 2.5 V to 5.5 V and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
13–20	DB_0–DB_7	Eight Parallel Data Inputs. DB_7 is the MSB of these eight bits.

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TERMINOLOGY

RELATIVE ACCURACY

For the DAC, Relative Accuracy or Integral Nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the actual endpoints of the DAC transfer function. Typical INL versus Code plot can be seen in Figures 5, 6, and 7.

DIFFERENTIAL NONLINEARITY

Differential Nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. Typical DNL versus Code plot can be seen in Figures 8, 9, and 10.

GAIN ERROR

This is a measure of the span error of the DAC (including any error in the gain of the buffer amplifier). It is the deviation in slope of the actual DAC transfer characteristic from the ideal expressed as a percentage of the full-scale range. This is illustrated in Figure 2.

OFFSET ERROR

This is a measure of the offset error of the DAC and the output amplifier. It is expressed as a percentage of the full-scale range.

If the offset voltage is positive, the output voltage will still be positive at zero input code. This is shown in Figure 3. Because the DACs operate from a single supply, a negative offset cannot appear at the output of the buffer amplifier. Instead, there will be a code close to zero at which the amplifier output saturates (amplifier footroom). Below this code there will be a deadband over which the output voltage will not change. This is illustrated in Figure 4.

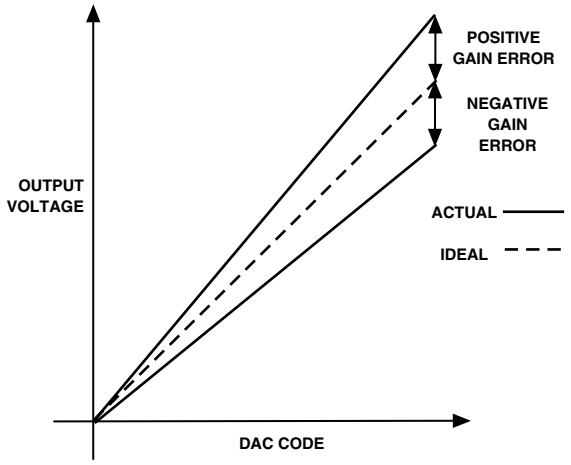

Figure 2. Gain Error

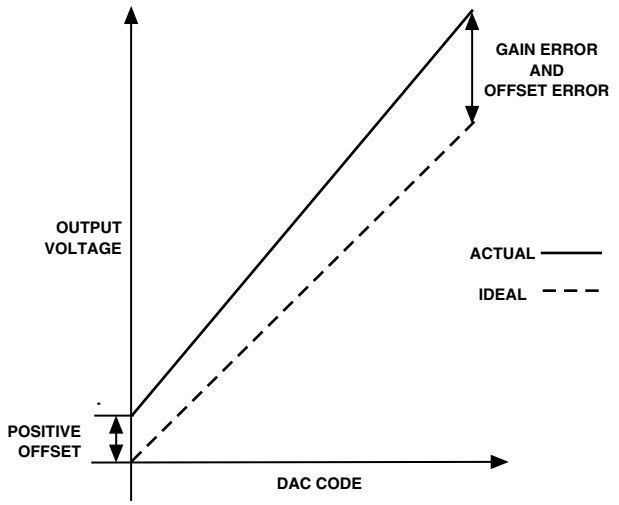

Figure 3. Positive Offset Error and Gain Error

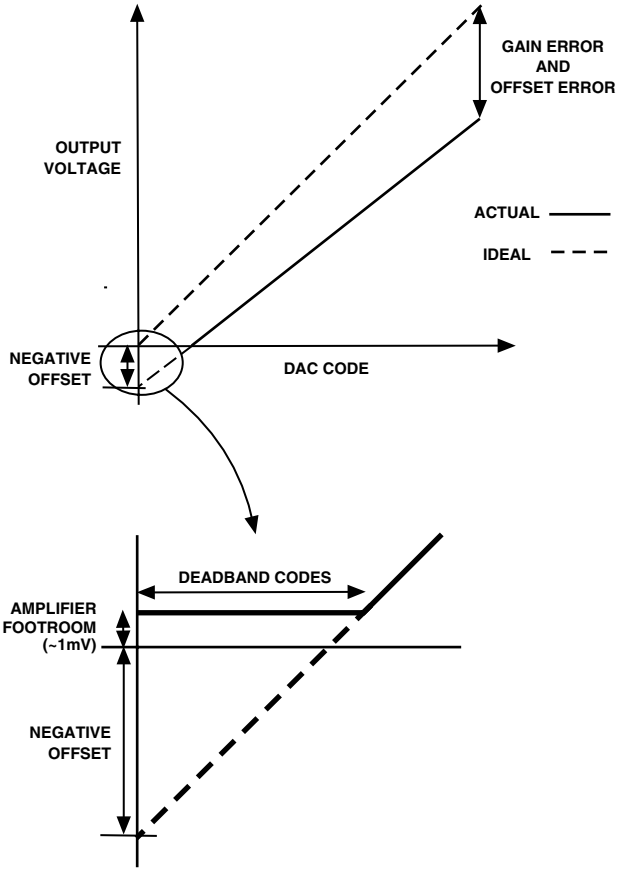

Figure 4. Negative Offset Error and Gain Error

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OFFSET ERROR DRIFT
This is a measure of the change in Offset Error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

GAIN ERROR DRIFT
This is a measure of the change in Gain Error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

POWER-SUPPLY REJECTION RATIO (PSRR)
This indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in dBs. V_{REF} is held at 2 V and V_{DD} is varied ±10%.

REFERENCE FEEDTHROUGH
This is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated (i.e., $\overline{\text{LDAC}}$ is high). It is expressed in dBs.

MAJOR-CODE TRANSITION GLITCH ENERGY
Major-Code Transition Glitch Energy is the energy of the impulse injected into the analog output when the DAC changes state. It is normally specified as the area of the glitch in nV secs and is measured when the digital code is changed by 1 LSB at the major carry transition (011 . . . 11 to 100 . . . 00 or 100 . . . 00 to 011 . . . 11).

DIGITAL FEEDTHROUGH
Digital Feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital input pins of the device, but is measured when the DAC is not being written to ($\overline{\text{CS}}$ held high). It is specified in nV secs and is measured with a full-scale change on the digital input pins, i.e., from all 0s to all 1s and vice versa.

MULTIPLYING BANDWIDTH
The amplifiers within the DAC have a finite bandwidth. The Multiplying Bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The Multiplying Bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

TOTAL HARMONIC DISTORTION
This is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC and the THD is a measure of the harmonics present on the DAC output. It is measured in dBs.

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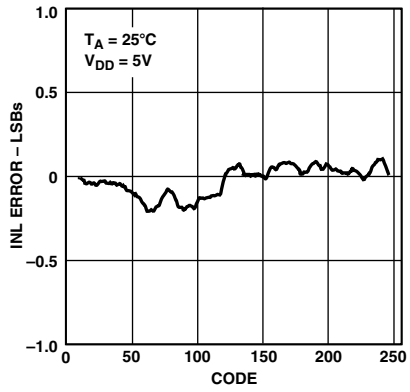

Figure 5. AD5330 Typical INL Plot

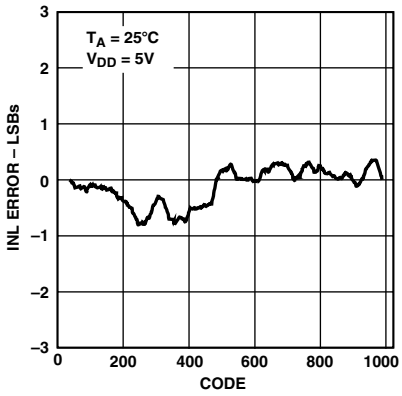

Figure 6. AD5331 Typical INL Plot

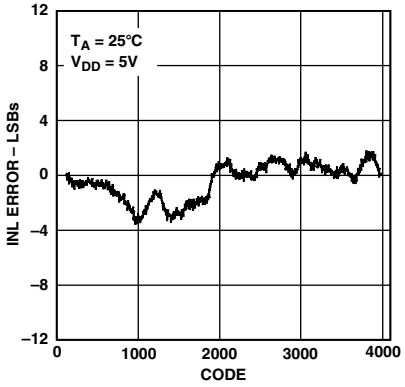

Figure 7. AD5340 Typical INL Plot

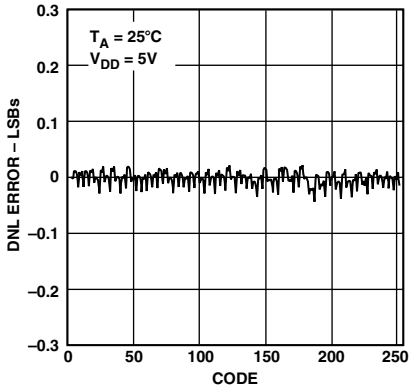

Figure 8. AD5330 Typical DNL Plot

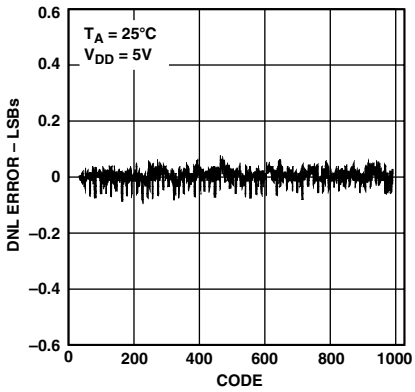

Figure 9. AD5331 Typical DNL Plot

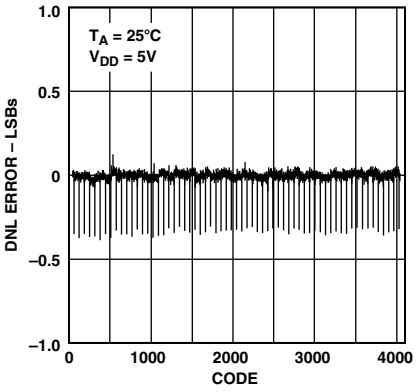

Figure 10. AD5340 Typical DNL Plot

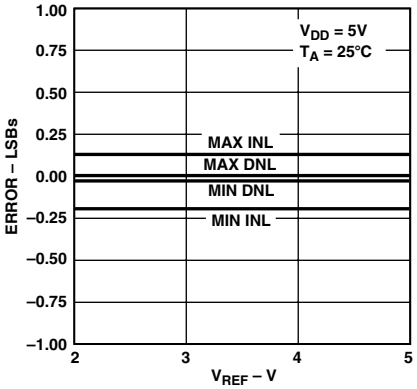

Figure 11. AD5330 INL and DNL Error vs. V_{REF}

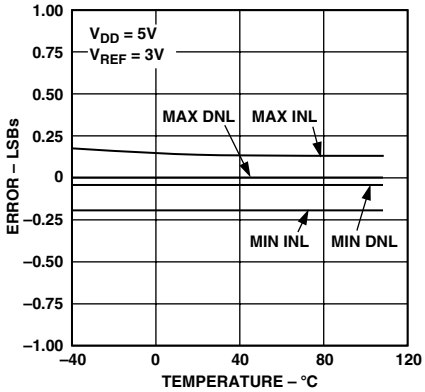

Figure 12. AD5330 INL Error and DNL Error vs. Temperature

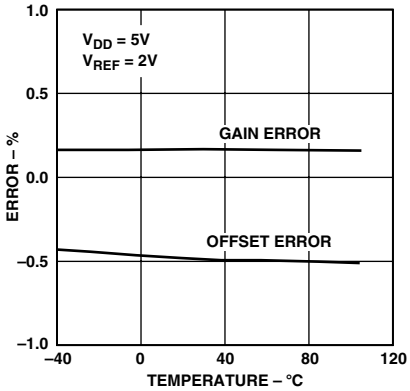

Figure 13. AD5330 Offset Error and Gain Error vs. Temperature

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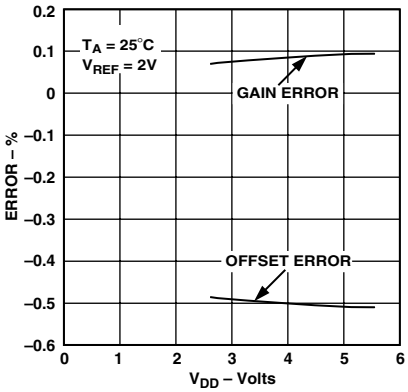

Figure 14. Offset Error and Gain Error vs. V_{DD}

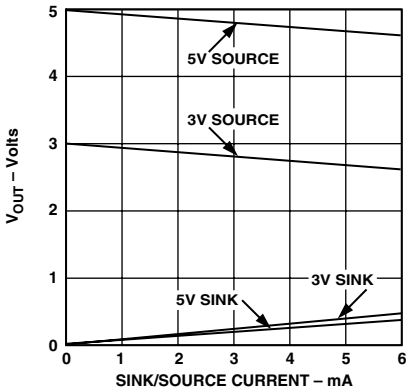

Figure 15. V_{OUT} Source and Sink Current Capability

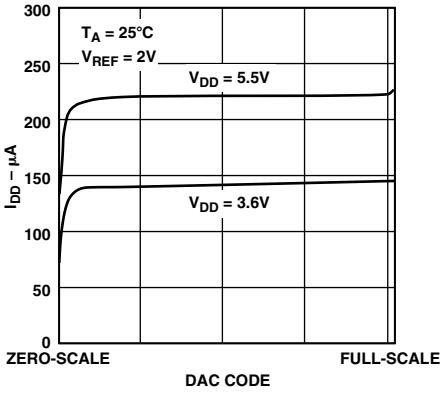

Figure 16. Supply Current vs. DAC Code

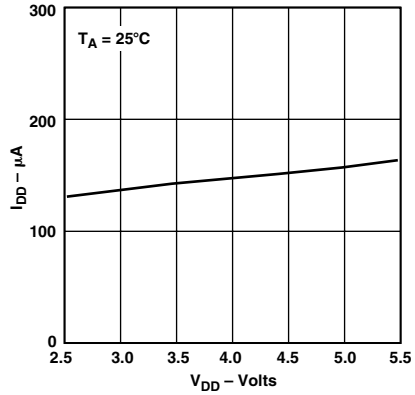

Figure 17. Supply Current vs. Supply Voltage

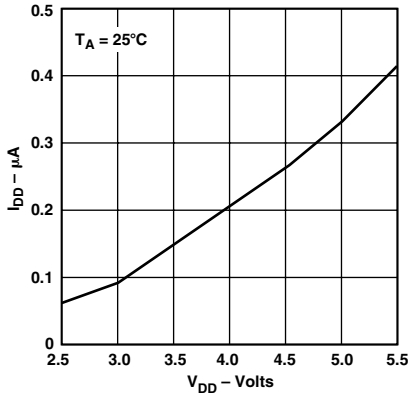

Figure 18. Power-Down Current vs. Supply Voltage

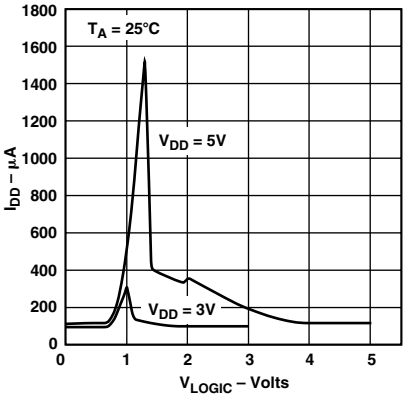

Figure 19. Supply Current vs. Logic Input Voltage

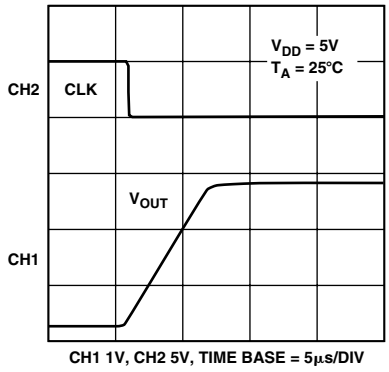

Figure 20. Half-Scale Settling (1/4 to 3/4 Scale Code Change)

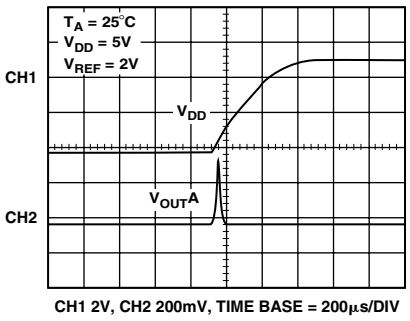

Figure 21. Power-On Reset to 0 V

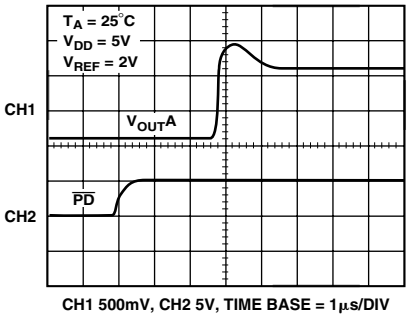

Figure 22. Exiting Power-Down to Midscale

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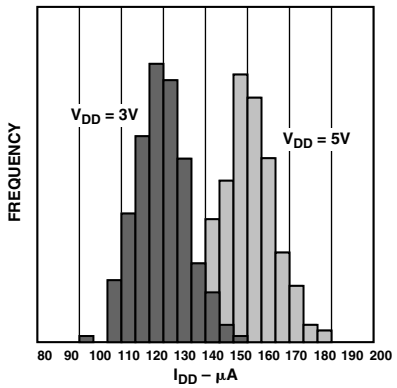

Figure 23. I_{DD} Histogram with V_{DD} = 3 V and V_{DD} = 5 V

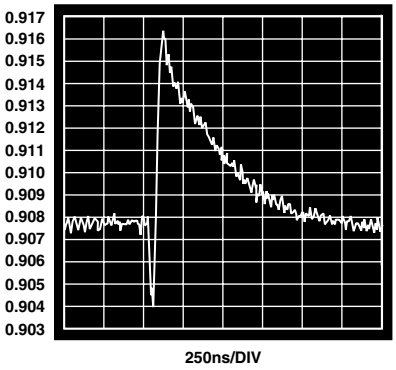

Figure 24. AD5340 Major-Code Transition Glitch Energy

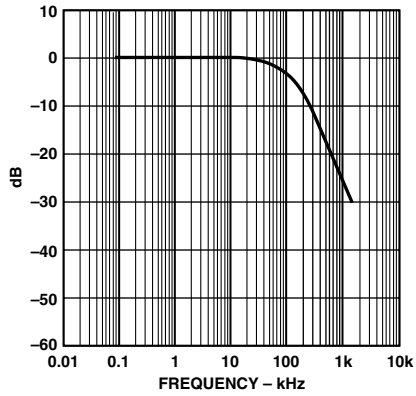

Figure 25. Multiplying Bandwidth (Small-Signal Frequency Response)

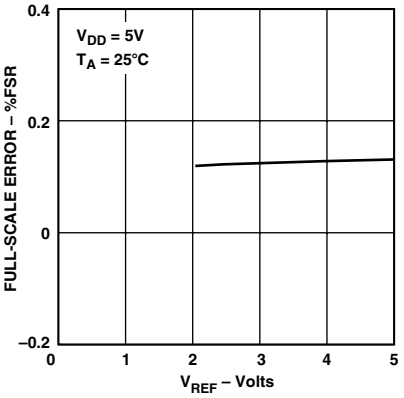

Figure 26. Full-Scale Error vs. V_{REF}

FUNCTIONAL DESCRIPTION

The AD5330/AD5331/AD5340/AD5341 are single resistor-string DACs fabricated on a CMOS process with resolutions of 8, 10, 12, and 12 bits, respectively. They are written to using a parallel interface. They operate from single supplies of 2.5 V to 5.5 V and the output buffer amplifiers offer rail-to-rail output swing. The AD5330, AD5340, and AD5341 have a reference input that may be buffered to draw virtually no current from the reference source. The reference input of the AD5331 is unbuffered. The devices have a power-down feature that reduces current consumption to only 80 nA @ 3 V.

Digital-to-Analog Section

The architecture of one DAC channel consists of a reference buffer and a resistor-string DAC followed by an output buffer amplifier. The voltage at the V_{REF} pin provides the reference voltage for the DAC. Figure 27 shows a block diagram of the DAC architecture. Since the input coding to the DAC is straight binary, the ideal output voltage is given by:

$$V_{OUT} = V_{REF} \times \frac{D}{2^N} \times Gain$$

where:

D = decimal equivalent of the binary code which is loaded to the DAC register:

0–255 for AD5330 (8 Bits)
0–1023 for AD5331 (10 Bits)
0–4095 for AD5340/AD5341 (12 Bits)

N = DAC resolution

Gain = Output Amplifier Gain (1 or 2)

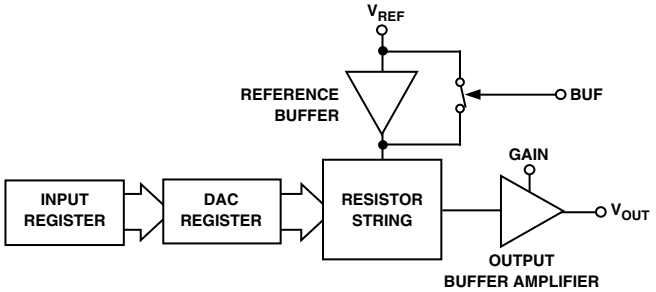

Figure 27. Single DAC Channel Architecture

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Resistor String
The resistor string section is shown in Figure 28. It is simply a string of resistors, each of value R. The digital code loaded to the DAC register determines at what node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

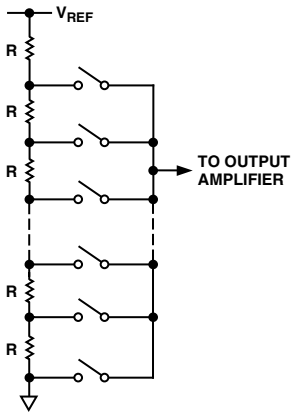

Figure 28. Resistor String

DAC Reference Input
There is a reference input pin for the DAC. The reference input is buffered on the AD5330/AD5340/AD5341 but can be configured as unbuffered also. The reference input of the AD5331 is unbuffered. The buffered/unbuffered option is controlled by the BUF pin.

In buffered mode (BUF = 1), the current drawn from an external reference voltage is virtually zero as the impedance is at least 10 MΩ. The reference input range is 1 V to 5 V with a 5 V supply.

In unbuffered mode (BUF = 0), the user can have a reference voltage as low as 0.25 V and as high as V_{DD} since there is no restriction due to headroom and footroom of the reference amplifier. The impedance is still large at typically 180 kΩ for 0–V_{REF} mode and 90 kΩ for 0–2 V_{REF} mode. If there is an external buffered reference (e.g., REF192) there is no need to use the on-chip buffer.

Output Amplifier
The output buffer amplifier is capable of generating output voltages to within 1 mV of either rail. Its actual range depends on V_{REF}, GAIN, the load on V_{OUT}, and offset error.

If a gain of 1 is selected (GAIN = 0), the output range is 0.001 V to V_{REF}.

If a gain of 2 is selected (GAIN = 1), the output range is 0.001 V to 2 V_{REF}. However, because of clamping, the maximum output is limited to V_{DD} – 0.001 V.

The output amplifier is capable of driving a load of 2 kΩ to GND or V_{DD}, in parallel with 500 pF to GND or V_{DD}. The source and sink capabilities of the output amplifier can be seen in Figure 15.

The slew rate is 0.7 V/μs with a half-scale settling time to ±0.5 LSB (at eight bits) of 6 μs with the output unloaded. See Figure 20.

PARALLEL INTERFACE
The AD5330, AD5331, and AD5340 load their data as a single 8-, 10-, or 12-bit word, while the AD5341 loads data as a low byte of eight bits and a high byte containing four bits.

Double-Buffered Interface
The AD5330/AD5331/AD5340/AD5341 DACs all have double-buffered interfaces consisting of an input register and a DAC register. DAC data, BUF, and GAIN inputs are written to the input register under control of the Chip Select ($\overline{CS}$) and Write ($\overline{WR}$).

Access to the DAC register is controlled by the $\overline{LDAC}$ function. When $\overline{LDAC}$ is high, the DAC register is latched and the input register may change state without affecting the contents of the DAC register. However, when $\overline{LDAC}$ is brought low, the DAC register becomes transparent and the contents of the input register are transferred to it. The gain and buffer control signals are also double-buffered and are only updated when $\overline{LDAC}$ is taken low.

Double-buffering is also useful where the DAC data is loaded in two bytes, as in the AD5341, because it allows the whole data word to be assembled in parallel before updating the DAC register. This prevents spurious outputs that could occur if the DAC register were updated with only the high byte or the low byte.

These parts contain an extra feature whereby the DAC register is not updated unless its input register has been updated since the last time that $\overline{LDAC}$ was brought low. Normally, when $\overline{LDAC}$ is brought low, the DAC register is filled with the contents of the input register. In the case of the AD5330/AD5331/AD5340/AD5341, the part will only update the DAC register if the input register has been changed since the last time the DAC register was updated. This removes unnecessary crosstalk.

Clear Input ($\overline{CLR}$)
$\overline{CLR}$ is an active low, asynchronous clear that resets the input and DAC registers.

Chip Select Input ($\overline{CS}$)
$\overline{CS}$ is an active low input that selects the device.

Write Input ($\overline{WR}$)
$\overline{WR}$ is an active low input that controls writing of data to the device. Data is latched into the input register on the rising edge of $\overline{WR}$.

Load DAC Input ($\overline{LDAC}$)
$\overline{LDAC}$ transfers data from the input register to the DAC register (and hence updates the outputs). Use of the $\overline{LDAC}$ function enables double-buffering of the DAC data, GAIN, and BUF. There are two $\overline{LDAC}$ modes:

Synchronous Mode: In this mode the DAC register is updated after new data is read in on the rising edge of the $\overline{WR}$ input. $\overline{LDAC}$ can be tied permanently low or pulsed as in Figure 1.

Asynchronous Mode: In this mode the outputs are not updated at the same time that the input register is written to. When $\overline{LDAC}$ goes low, the DAC register is updated with the contents of the input register.

High-Byte Enable Input (HBEN)
High-Byte Enable is a control input on the AD5341 only that determines if data is written to the high-byte input register or the low-byte input register.

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The low data byte of the AD5341 consists of data bits 0 to 7 at data inputs DB_0 to DB_7, while the high byte consists of data bits 8 to 11 at data inputs DB_0 to DB_3 as shown in Figure 29. DB_4 to DB_7 are ignored during a high-byte write, but they may be used for data to set up the reference input as buffered/ unbuffered, and buffer amplifier gain. See Figure 33.

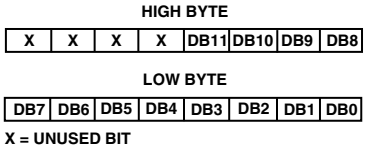

Figure 29. Data Format for AD5341

POWER-ON RESET

The AD5330/AD5331/AD5340/AD5341 are provided with a power-on reset function, so that they power up in a defined state. The power-on state is:

- Normal Operation
- Reference Input Unbuffered
- 0 – V_{REF} Output Range
- Output Voltage Set to 0 V

Both input and DAC registers are filled with zeros and remain so until a valid write sequence is made to the device. This is particularly useful in applications where it is important to know the state of the DAC outputs while the device is powering up.

POWER-DOWN MODE

The AD5330/AD5331/AD5340/AD5341 have low power consumption, dissipating only 0.35 mW with a 3 V supply and 0.7 mW with a 5 V supply. Power consumption can be further reduced when the DAC is not in use by putting it into power-down mode, which is selected by taking pin $\overline{PD}$ low.

When the $\overline{PD}$ pin is high, the DAC works normally with a typical power consumption of 140 µA at 5 V (115 µA at 3 V). In power-down mode, however, the supply current falls to 200 nA at 5 V (80 nA at 3 V) when the DAC is powered-down. Not only does the supply current drop, but the output stage is also internally switched from the output of the amplifier making it open-circuit. This has the advantage that the output is three-state while the part is in power-down mode and provides a defined input condition for whatever is connected to the output of the DAC amplifier. The output stage is illustrated in Figure 30.

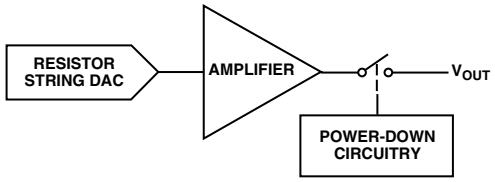

Figure 30. Output Stage During Power-Down

The bias generator, the output amplifier, the resistor string, and all other associated linear circuitry are shut down when the power-down mode is activated. However, the contents of the registers are unaffected when in power-down. The time to exit power-down is typically 2.5 µs for V_{DD} = 5 V and 5 µs when V_{DD} = 3 V. This is the time from a rising edge on the $\overline{PD}$ pin to when the output voltage deviates from its power-down voltage. See Figure 22.

Table I. AD5330/AD5331/AD5340 Truth Table

$\overline{CLR}$	$\overline{LDAC}$	$\overline{CS}$	$\overline{WR}$	Function
1	1	1	X	No Data Transfer
1	1	X	1	No Data Transfer
0	X	X	X	Clear All Registers
1	1	0	0→1	Load Input Register
1	0	0	0→1	Load Input Register and DAC Register
1	0	X	X	Update DAC Register

X = don't care.

Table II. AD5341 Truth Table

$\overline{CLR}$	$\overline{LDAC}$	$\overline{CS}$	$\overline{WR}$	HBEN	Function
1	1	1	X	X	No Data Transfer
1	1	X	1	X	No Data Transfer
0	X	X	X	X	Clear All Registers
1	1	0	0→1	0	Load Low-Byte Input Register
1	1	0	0→1	1	Load High-Byte Input Register
1	0	0	0→1	0	Load Low-Byte Input Register and DAC Register
1	0	0	0→1	1	Load High-Byte Input Register and DAC Register
1	0	X	X	X	Update DAC Register

X = don't care.

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SUGGESTED DATABUS FORMATS

In most applications GAIN and BUF are hard-wired. However, if more flexibility is required, they can be included in a databus. This enables you to software program GAIN, giving the option of doubling the resolution in the lower half of the DAC range. In a bused system, GAIN and BUF may be treated as data inputs since they are written to the device during a write operation and take effect when $\overline{\text{LDAC}}$ is taken low. This means that the reference buffers and the output amplifier gain of multiple DAC devices can be controlled using common GAIN and BUF lines.

In the case of the AD5330 this means that the databus must be wider than eight bits. The AD5331 and AD5340 databuses must be at least 10 and 12 bits wide respectively and are best suited to a 16-bit databus system.

Examples of data formats for putting GAIN and BUF on a 16-bit databus are shown in Figure 31. Note that any unused bits above the actual DAC data may be used for BUF and GAIN. DAC devices can be controlled using common GAIN and BUF lines.

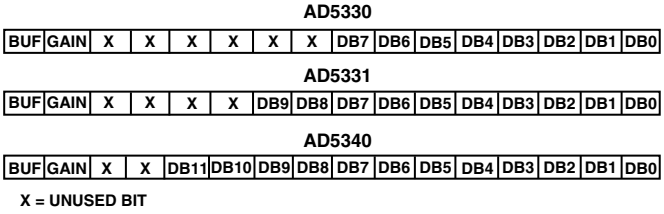

Figure 31. GAIN and BUF Data on a 16-Bit Bus

The AD5341 is a 12-bit device that uses byte load, so only four bits of the high byte are actually used as data. Two of the unused bits can be used for GAIN and BUF data by connecting them to the GAIN and BUF inputs; e.g., Bits 6 and 7, as shown in Figures 32 and 33.

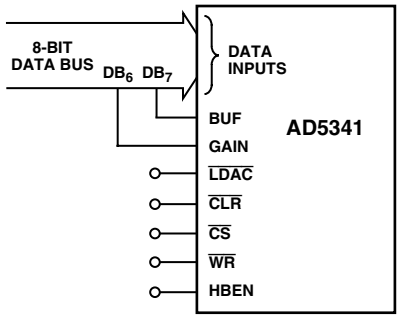

Figure 32. AD5341 Data Format for Byte Load with GAIN and BUF Data on 8-Bit Bus

In this case, the low byte is written first in a write operation with HBEN = 0. Bits 6 and 7 of DAC data will be written into GAIN and BUF registers but will have no effect. The high byte is then written. Only the lower four bits of data are written into the DAC high byte register, so Bits 6 and 7 can be GAIN and BUF data.

$\overline{\text{LDAC}}$ is used to update the DAC, GAIN and BUF values.

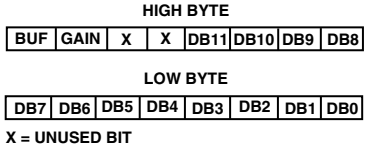

Figure 33. AD5341 with GAIN and BUF Data on 8-Bit Bus

APPLICATIONS INFORMATION

Typical Application Circuits

The AD5330/AD5331/AD5340/AD5341 can be used with a wide range of reference voltages, especially if the reference inputs are configured to be unbuffered, in which case the devices offer full, one-quadrant multiplying capability over a reference range of 0.25 V to V_{DD}. More typically, these devices may be used with a fixed, precision reference voltage. Figure 34 shows a typical setup for the devices when using an external reference connected to the unbuffered reference inputs. If the reference inputs are unbuffered, the reference input range is from 0.25 V to V_{DD}, but if the on-chip reference buffers are used, the reference range is reduced. Suitable references for 5 V operation are the AD780 and REF192. For 2.5 V operation, a suitable external reference would be the AD589, a 1.23 V bandgap reference.

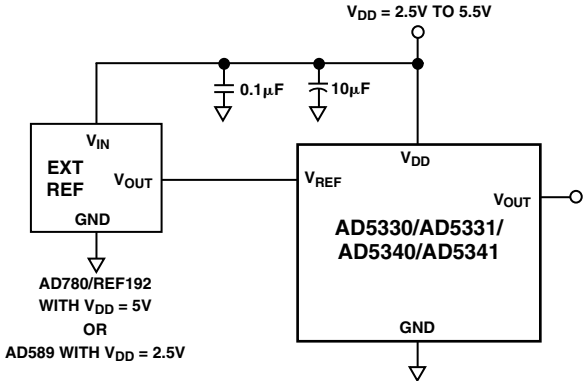

Figure 34. AD5330/AD5331/AD5340/AD5341 Using External Reference

Driving V_{DD} From the Reference Voltage

If an output range of zero to V_{DD} is required, the simplest solution is to connect the reference inputs to V_{DD}. As this supply may not be very accurate, and may be noisy, the devices may be powered from the reference voltage, for example using a 5 V reference such as the ADM663 or ADM666, as shown in Figure 35.

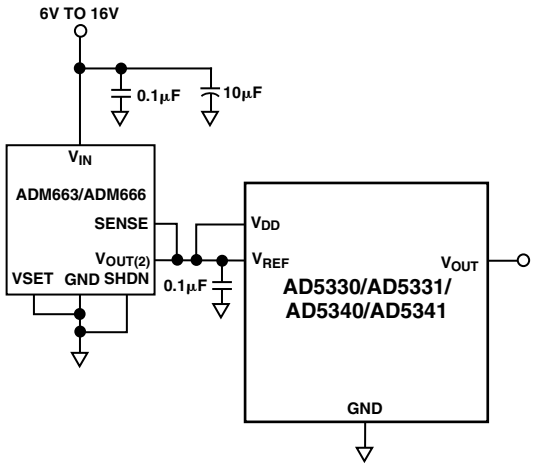

Figure 35. Using an ADM663/ADM666 as Power and Reference to AD5330/AD5331/AD5340/AD5341

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Bipolar Operation Using the AD5330/AD5331/AD5340/AD5341

The AD5330/AD5331/AD5340/AD5341 have been designed for single supply operation, but bipolar operation is achievable using the circuit shown in Figure 36. The circuit shown has been configured to achieve an output voltage range of –5 V < V_O < +5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820 or OP295 as the output amplifier.

The output voltage for any input code can be calculated as follows:

$$V_O = [(1 + R4/R3) \times (R2/(R1 + R2) \times (2 \times V_{REF} \times D/2^N)] - R4 \times V_{REF}/R3$$

where:

D is the decimal equivalent of the code loaded to the DAC, N is DAC resolution and V_{REF} is the reference voltage input.

With:

V_{REF} = 2.5 V
R1 = R3 = 10 kΩ
R2 = R4 = 20 kΩ and V_{DD} = 5 V.
$V_{OUT} = (10 \times D/2^N) - 5$

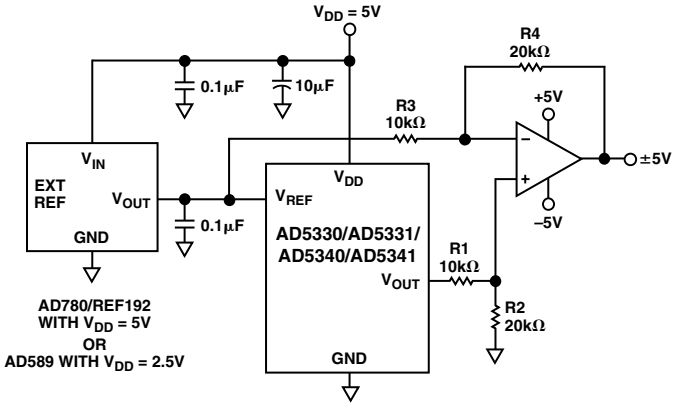

Figure 36. Bipolar Operation using the AD5330/AD5331/ AD5340/AD5341

Decoding Multiple AD5330/AD5331/AD5340/AD5341

The $\overline{CS}$ pin on these devices can be used in applications to decode a number of DACs. In this application, all DACs in the system receive the same data and $\overline{WR}$ pulses, but only the $\overline{CS}$ to one of the DACs will be active at any one time, so data will only be written to the DAC whose $\overline{CS}$ is low. If multiple AD5341s are being used, a common HBEN line will also be required to determine if the data is written to the high-byte or low-byte register of the selected DAC.

The 74HC139 is used as a 2- to 4-line decoder to address any of the DACs in the system. To prevent timing errors, the enable input should be brought to its inactive state while the coded address inputs are changing state. Figure 37 shows a diagram of a typical setup for decoding multiple devices in a system. Once data has been written sequentially to all DACs in a system, all the DACs can be updated simultaneously using a common $\overline{LDAC}$ line. A common $\overline{CLR}$ line can also be used to reset all DAC outputs to zero.

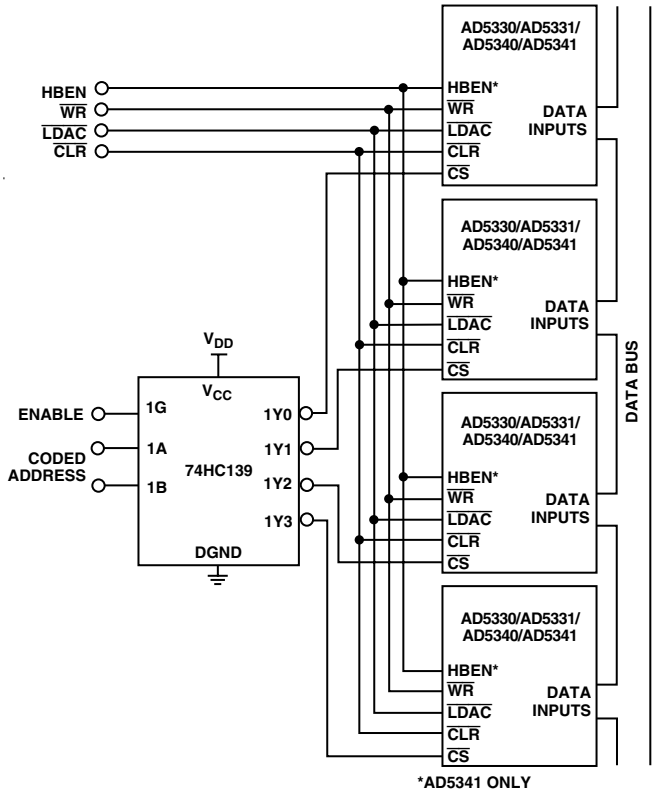

Figure 37. Decoding Multiple DAC Devices

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Programmable Current Source

Figure 38 shows the AD5330/AD5331/AD5340/AD5341 used as the control element of a programmable current source. In this example, the full-scale current is set to 1 mA. The output voltage from the DAC is applied across the current setting resistor of 4.7 kΩ in series with the 470 Ω adjustment potentiometer, which gives an adjustment of about ±5%. Suitable transistors to place in the feedback loop of the amplifier include the BC107 and the 2N3904, which enable the current source to operate from a minimum V_{SOURCE} of 6 V. The operating range is determined by the operating characteristics of the transistor. Suitable amplifiers include the AD820 and the OP295, both having rail-to-rail operation on their outputs. The current for any digital input code and resistor value can be calculated as follows:

$$I = G \times V_{REF} \times \frac{D}{(2^N \times R)}\ mA$$

Where:

G is the gain of the buffer amplifier (1 or 2)
D is the digital equivalent of the digital input code
N is the DAC resolution (8, 10, or 12 bits)
R is the sum of the resistor plus adjustment potentiometer in kΩ

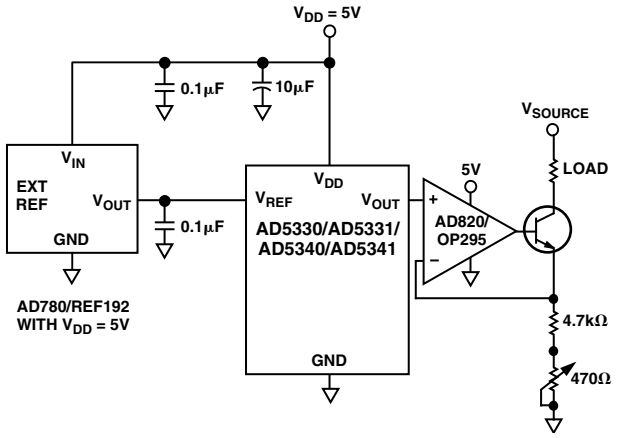

Figure 38. Programmable Current Source

Power Supply Bypassing and Grounding

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5330/AD5331/AD5340/AD5341 is mounted should be designed so that the analog and digital sections are separated, and confined to certain areas of the board. If the device is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as closely as possible to the device. The AD5330/AD5331/AD5340/AD5341 should have ample supply bypassing of 10 µF in parallel with 0.1 µF on the supply located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low Effective Series Resistance (ESR) and Effective Series Inductance (ESI), like the common ceramic types that provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply lines of the device should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane while signal traces are placed on the solder side.

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Table III. Overview of AD53xx Parallel Devices

Part No.	Resolution	DNL	V_{REF} Pins	Settling Time	Additional Pin Functions				Package	Pins
SINGLES					**BUF**	**GAIN**	**HBEN**	**$\overline{CLR}$**		
AD5330	8	±0.25	1	6 µs	✓	✓		✓	TSSOP	20
AD5331	10	±0.5	1	7 µs		✓		✓	TSSOP	20
AD5340	12	±1.0	1	8 µs	✓	✓		✓	TSSOP	24
AD5341	12	±1.0	1	8 µs	✓	✓	✓	✓	TSSOP	20
DUALS										
AD5332	8	±0.25	2	6 µs				✓	TSSOP	20
AD5333	10	±0.5	2	7 µs	✓	✓		✓	TSSOP	24
AD5342	12	±1.0	2	8 µs	✓	✓		✓	TSSOP	28
AD5343	12	±1.0	1	8 µs			✓	✓	TSSOP	20
QUADS										
AD5334	8	±0.25	2	6 µs		✓		✓	TSSOP	24
AD5335	10	±0.5	2	7 µs			✓	✓	TSSOP	24
AD5336	10	±0.5	4	7 µs		✓		✓	TSSOP	28
AD5344	12	±1.0	4	8 µs					TSSOP	28

Table IV. Overview of AD53xx Serial Devices

Part No.	Resolution	No. of DACs	DNL	Interface	Settling Time	Package	Pins
SINGLES							
AD5300	8	1	±0.25	SPI	4 µs	SOT-23, MicroSOIC	6, 8
AD5310	10	1	±0.5	SPI	6 µs	SOT-23, MicroSOIC	6, 8
AD5320	12	1	±1.0	SPI	8 µs	SOT-23, MicroSOIC	6, 8
AD5301	8	1	±0.25	2-Wire	6 µs	SOT-23, MicroSOIC	6, 8
AD5311	10	1	±0.5	2-Wire	7 µs	SOT-23, MicroSOIC	6, 8
AD5321	12	1	±1.0	2-Wire	8 µs	SOT-23, MicroSOIC	6, 8
DUALS							
AD5302	8	2	±0.25	SPI	6 µs	MicroSOIC	8
AD5312	10	2	±0.5	SPI	7 µs	MicroSOIC	8
AD5322	12	2	±1.0	SPI	8 µs	MicroSOIC	8
AD5303	8	2	±0.25	SPI	6 µs	TSSOP	16
AD5313	10	2	±0.5	SPI	7 µs	TSSOP	16
AD5323	12	2	±1.0	SPI	8 µs	TSSOP	16
QUADS							
AD5304	8	4	±0.25	SPI	6 µs	MicroSOIC	10
AD5314	10	4	±0.5	SPI	7 µs	MicroSOIC	10
AD5324	12	4	±1.0	SPI	8 µs	MicroSOIC	10
AD5305	8	4	±0.25	2-Wire	6 µs	MicroSOIC	10
AD5315	10	4	±0.5	2-Wire	7 µs	MicroSOIC	10
AD5325	12	4	±1.0	2-Wire	8 µs	MicroSOIC	10
AD5306	8	4	±0.25	2-Wire	6 µs	TSSOP	16
AD5316	10	4	±0.5	2-Wire	7 µs	TSSOP	16
AD5326	12	4	±1.0	2-Wire	8 µs	TSSOP	16
AD5307	8	4	±0.25	SPI	6 µs	TSSOP	16
AD5317	10	4	±0.5	SPI	7 µs	TSSOP	16
AD5327	12	4	±1.0	SPI	8 µs	TSSOP	16

Visit our web-page at http://www.analog.com/support/standard_linear/selection_guides/AD53xx.html

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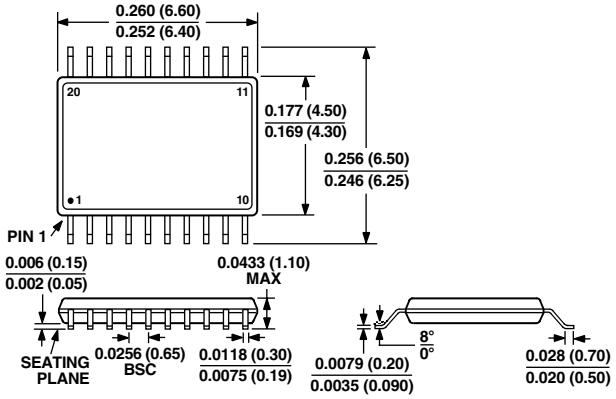
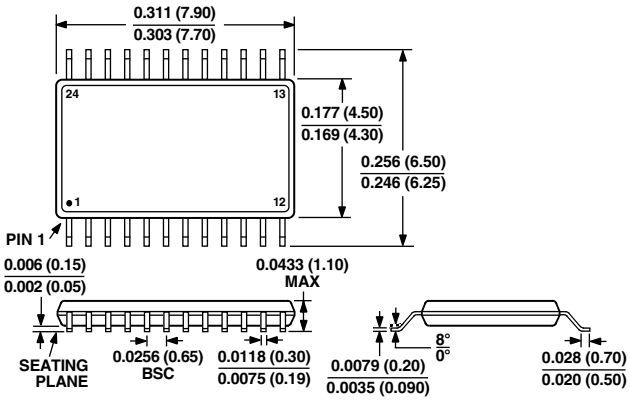
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

20-Lead Thin Shrink Small Outline Package TSSOP (RU-20)



24-Lead Thin Shrink Small Outline Package TSSOP (RU-24)



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