CS1160 Specification

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1 CS1160 DESCRIPTION

The CS1160 is precision, low power dissipation, Analog-to-Digital (A/D) converter with 16-bit resolution and up to 16-bit ENOB. The CS1160 has world wide applications in industrial process control, weigh scales, liquid/gas chemical analysis, blood analysis, smart transmitters and portable instrumentation.

1.1 CS1160 FEATURES

- 16 bits no missing code, 16 bits effective precision Analog-to-Digital converters
- Simultaneous 50Hz and 60Hz rejection (reaching －90dB)
- 0.0060% INL
- PGA gains from 1 to 128
- Single-cycle setting
- Programmable ADC data output rates
- External differential reference of 0.1V to 5V
- On-chip calibration
- Integrated compatible SPI bus interface

1.2 APPLICATIONS

- Industrial process control
- Weigh scales
- liquid/gas chemical analysis
- blood analysis
- Smart transmitters
- Portable instrumentation

1.3 DESCRIPTION

The CS1160 principle block diagram is shown in Figure 1.

The CS1160 is a 16 bits Sigma-Delta analog-to-digital converter chip with high accuracy, low power dissipation. The CS1160 works from 2.7V to 5.5V power supplies with 16 bits ENOB.

The Programmable Gain Amplifier (PGA) provides selectable gains from 1 to 128 with 16 bits ENOB at the gain of 128. The A/D conversion is performed with a second-order Sigma-Delta modulator, and programmable FIR filter that provides a simultaneous 50Hz and 60Hz notch which effectively improve the interference immunity.

The CS1160 provides SPI compatible serial interface bus.

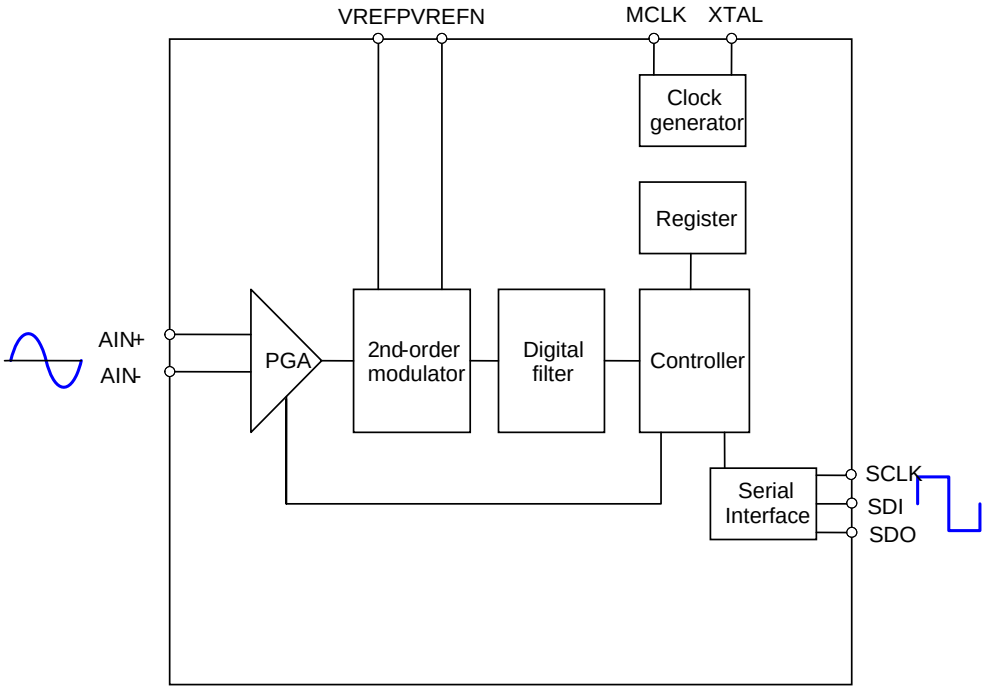


Figure 1 CS1160 Principle Block Diagram

2 CS1160 CHARACTERISTIC DESCRIPTION

2.1 ABSOLUTE MAXIMUM RATINGS

Table 1 shows the limit values of the CS1160.

Table 1 Limit Value

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
AVDD to AGND	AVDD	-0.3	6	V
DVDD to DGND	DVDD	-0.3	6	V
DGND to AGND	DVGND	-0.3	0.3	V
Transient Input Current			100	mA
Continuous Input Current			10	mA
Digital Input Voltage to DGND		-0.3	DVDD+0.3	V
Digital Output Voltage to DGND		-0.3	DVDD+0.3	V
Max. Junction Temperature			150	°C
Operating Temperature		-40	85	°C
Storage Temperature		-60	150	°C
Lead Temperature (Soldering, 10s)			240	°C

2.2 DIGITAL CHARACTERISTICS

Table 2 shows the digital characteristics of the CS1160.

Table 2 Digital Characteristics

PARAMETER	MIN	TYP	MAX	UNITS	CONDITION
VIH	0.8×DVDD		DVDD	V	
VIL	DGND		0.2×DVDD	V	
VOH	DVDD-0.4		DVDD+0.4	V	Ioh=1mA
VOL	DGND		DGND+0.4	V	IoL=1mA
IIH			10	uA	VI=DVDD
IIL	-10			uA	VI=DGND
fosc	1		5	MHz	
tosc	200		1000	ns	
NOTES：The digital interface is CMOS logic.					

2.3 PINS and PACKAGING

The pins of the CS1160 are shown in Figure 2, and particular description refers to Table3.

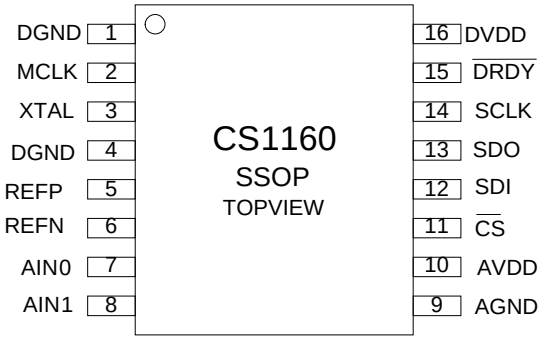


Figure 2 Pin Diagram

Table 3 Pin Description

PIN NUMBER	SYMBOL	DESCRIPTION	REMARK
1	DGND	Digital ground	
2	MCLK	Master clock input, 1～10MHz	
3	XTAL	Crystal oscillator drive pin 2	
4	DGND	Digital ground	
5	REFP	Analog reference voltage input (positive)	
6	REFN	Analog reference voltage input (negative)	
7	AIN0	Analog input 0	
8	AIN1	Analog input 1	
9	AGND	Analog ground	
10	AVDD	Analog power supply voltage, 2.7V~5.25V	
11	$\overline{CS}$	Active low, Chip select	
12	SDI	Serial data input	
13	SDO	Serial data output	
14	SCLK	Serial clock , Schmitt trigger	
15	$\overline{DRDY}$	Active low ,Data ready	
16	DVDD	Digital power supply voltage, 2.7~5.25V	

The CS1160 uses SSOP-16 package, the temperature range of the CS1160 is from -40℃ to +85℃, seeing the Table 4.

Table 4 Package

NAME	PACKAGE	TEMPERATURE RANGE
CS1160	SSOP－16	－40℃～85℃

2.4 ELECTRICAL CHARACTERISTICS

Table 5 Electrical Characteristics (AVDD=5V)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Analog input	Analog input range		AGND-0.1		AVDD+0.1	V
	Full-scale input range (AIN+) - (AIN-)	RAN=0			±VREF/PGA	V
		RAN=1			±VREF/(2×PGA)	V
	Differential input impedance			5/PGA		MΩ
	Bandwidth (-3dB)	f_{DATA} = 3.75Hz		1.65		Hz
		f_{DATA} = 7.50Hz		3.44		Hz
		f_{DATA} = 15.0Hz		3.7		Hz
	PGA	User-selectable gain ranges	1		128	
	Input capacitance			9		pF
	Input leakage current	Modulator OFF, T = 25℃		5		pA
	Burnout current sources			2		2uA
System performance	Resolution	No missing codes		20		Bits
	Integral nonlinearity				±0.0015	% of FS
	Offset error			8		ppm of FS
	Offset error drift			0.02		ppm of FS/℃
	Gain error			0.005		%
	Gain error drift			0.5		ppm/℃
	Common-mode rejection	at DC	100			dB
		f_{CM} = 60Hz, f_{DATA} = 15Hz		130		dB
		f_{CM} = 50Hz, f_{DATA} = 15Hz		120		dB
	Notch rejection	f_{CM} = 60Hz, f_{DATA} = 15Hz		100		dB
		f_{SIG} = 50Hz, f_{DATA} = 15Hz		100		dB
	Power-supply rejection	at DC	80	95		dB
Voltage reference input	VREF≡REFP－REFN	RAN = 0	0.1	2.5	2.6	V
		RAN = 1	0	2.5	AVDD	V
	REFP, REFN Input range	RAN = 0	0		AVDD	V
		RAN = 1	0.1		AVDD	V
	Common-mode rejection	at DC		120		dB
		f_{VREFCM} = 60Hz		120		dB
	Bias current			1.3		uA
Power-supply	Power-supply voltage	AVDD	4.75		5.25	V
	Current of analog part	$\overline{PD}$ = 0, or SLEEP		1		nA
		PGA = 1		120		uA
		PGA = 128		400		uA
	Current of digital part (DVDD = 5V)	Normal mode		80		uA
		SLEEP mode		60		uA
	Power dissipation			1.1	1.9	mW

Table 6 Electrical Characteristics (AVDD=3V)

PARAMETER		CONDITION	MIN	TYP	MAX	UNITS
Analog input	Analog input range		AGND-0.1		AVDD+0.1	V
	Full-scale input range (AIN+) - (AIN-)	RAN=0			±VREF/PGA	V
		RAN=1			±VREF/(2×PGA)	V
	Differential input impedance			5/PGA		MΩ
	Bandwidth (-3dB)	f_{DATA} = 3.75Hz		1.65		Hz
		f_{DATA} = 7.50Hz		3.44		Hz
		f_{DATA} = 15.0Hz		14.6		Hz
	PGA	User-selectable gain ranges	1		128	
	Input capacitance			9		pF
	Input leakage current	Modulator OFF, T = 25℃		5		pA
	Burnout current sources			2		2uA
System performance	Resolution	No missing codes		20		Bits
	Integral nonlinearity				±0.0015	% of FS
	Offset error			15		ppm of FS
	Offset error drift			0.04		ppm of FS/℃
	Gain error			0.01		%
	Gain error drift			1.0		ppm/℃
	Common-mode rejection	at DC	100			dB
		f_{CM} = 60Hz, f_{DATA} = 15Hz		130		dB
		f_{CM} = 50Hz, f_{DATA} = 15Hz		120		dB
	Notch rejection	f_{CM} = 60Hz, f_{DATA} = 15Hz		100		dB
		f_{SIG} = 50Hz, f_{DATA} = 15Hz		100		dB
	Power-supply rejection	at DC	75	90		dB
Voltage reference input	VREF=REFP－REFN	RAN = 0	0.1	1.25	1.30	V
		RAN = 1	0	2.5	2.6	V
	REFP, REFN input range	RAN = 0	0		AVDD	V
		RAN = 1	0.1		AVDD	V
	Common-mode rejection	at DC		120		dB
		f_{VREFCM} = 60Hz		120		dB
	Bias current			0.65		uA
Power-supply	Power-supply voltage	AVDD	2.7		3.3	V
	Current of analog part	$\overline{PD}$ = 0, or SLEEP		1		nA
		PGA = 1		107		uA
		PGA = 128		360		uA
	Current of digital part (DVDD = 3V)	Normal mode		50		uA
		SLEEP mode		40		uA
	Power dissipation			0.6	1.2	mW

2.5 TIMING CHARACTERISTICS

The timing diagram is shown in Figure 3, and particular description refers to Table7.

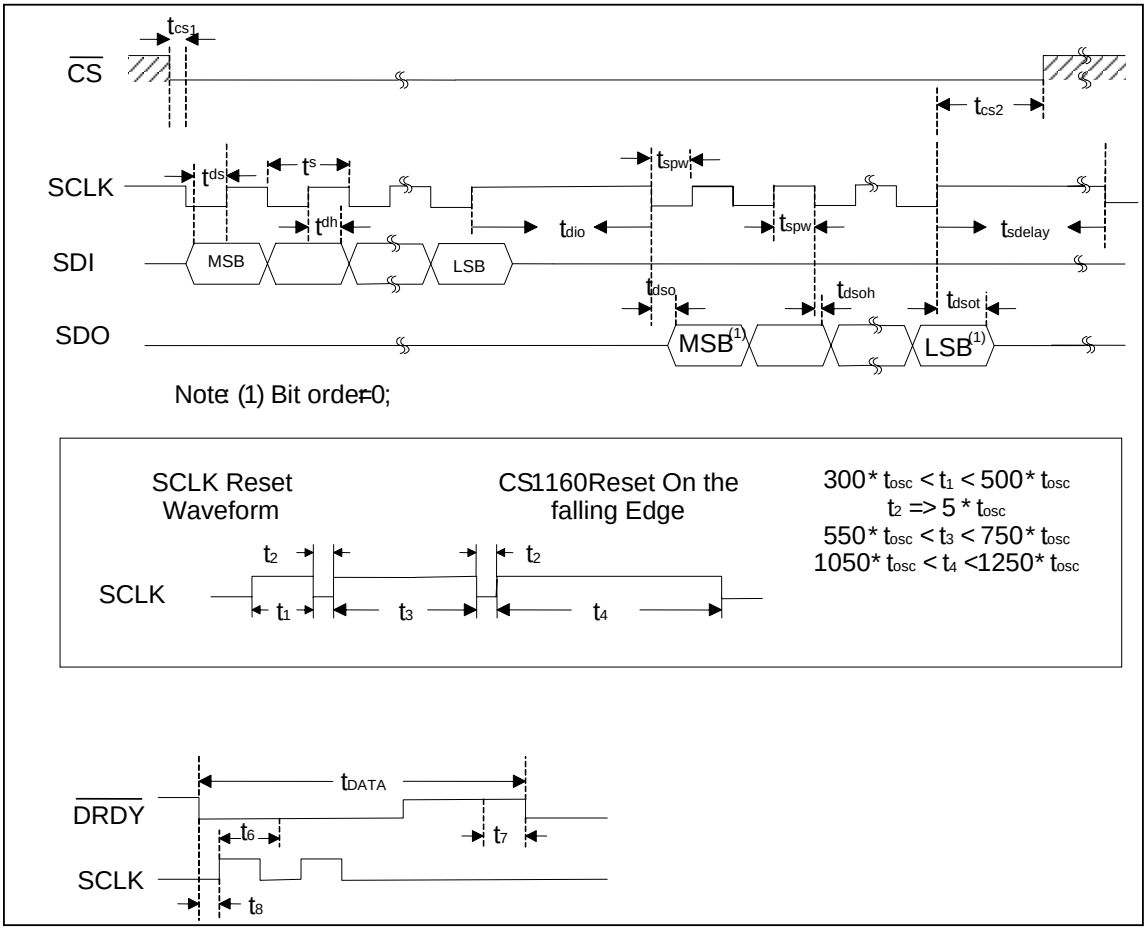


Figure 3 Timing Diagram

Table 7 Timing Table

SPEC	DESCRIPTION		MIN	MAX	UNITS
t_s	SCLK period		4		Tosc Periods
t_{spw}	SCLK Pulse Width, HIGH and LOW		200		ns
t_{cs1}	CS low to first SCLK edge, setup time		0		ns
t_{ds}	SDI data setup time (with SCLK delay)		50		ns
t_{dsh}	Valid SDI data hold time		50		ns
t_{dio}	Delay between last SCLK edge for SDI and first SCLK edge for SDO when sending the following commands: RDATA, RREG, WREG		50		Tosc Periods
t_{dso}	SCLK edge to SDO new output data			50	ns
t_{dsoh}	SDO data hold time		0		
t_{dsot}	Last SCLK edge to SDO goes tri-state		6	10	Tosc Periods
t_{cs2}	CS low time after final SCLK edge		0		ns
t_{sdelay}	Final SCLK edge of one command until first edge SCLK of next command:	RREG, WREG, SYNC, SLEEP, RDATA, RDATAC, STOPC	4		Tosc Periods
		GCALSELF, SELFOCA, OCALSYS, GCALSYS	8		DRDY periods
		CALSELF	15		DRDY Periods
		RESET (also SCLK reset or $\overline{RST}$ pin gives off RESET command)	16		Tosc Periods
t_6	Allowed analog input change for next valid conversion			5000	Tosc Periods
t_7	DOR update, DOR data is invalid		4		Tosc Periods
t_8	First SCLK after DRDY goes low		0		Tosc Periods

3 CS1160 FUNCTION MODULE DESCRIPTION

3.1 ANALOG INPUT BUFFER

The input impedance of the CS1160 is about 5MΩ/PGA with the buffer off, but the input impedance is up to about 5GΩ with the buffer on.

The buffer can be controlled by the BUF pin and the register ACR. When the BUF bit in ACR register and BUF pin is high, the buffer is on.

The buffer will draw additional power dissipation when activated. The power depends on the PGA setting. When PGA=1, the buffer produces approximately 50uA additional current; When the PGA=128, the buffer produces approximately 150uA additional current.

The input range should be AGND+0.3V to AVDD-1.5V with the buffer on.

3.2 PROGRAMMABLE GAIN AMPLIFIER (PGA)

The Programmable Gain Amplifier (PGA) can be set to 1, 2, 4, 8, 16, 32, 64, or 128. Using PGA can improve the ENOB of the A/D converter. For example, when PGA=1, the full scale input is 5V, the converter can resolve down to 38.1uV; when PGA=128, the full scale input is 39mV, the converter can resolve down to 300nV.

3.3 MODULATOR

The Modulator of the CS1160 is a single loop, second order Sigma-Delta system. The sample frequency of the modulator is controlled by the SPEED bit in ACR register (ACR bit 5). The sample frequency is shown in Table8:

Table 8 The Sample Frequency of The Modulator

Frequency (MHz)	SPEED	ADC Sample Frequency (KHz)	Data Output Rate (Hz)			Rejection Frequency (Hz)
			DR = 00	DR = 01	DR = 10	
2.4576	0	19.200	15	7.5	3.75	50/60
	1	9.600	7.5	3.75	1.875	25/30
4.9152	0	38.400	30	15	7.5	100/120
	1	19.200	15	7.5	3.75	50/60

3.4 CALIBRATION

The CS1160 provides both self calibration and system calibration which include offset and gain calibration of the A/D converter. During calibration, the DRDY signal will be held at high, which indicates the result of the AD converter is invalid.

In order to ensure the accuracy of the data of the A/D converter, the calibration should be performed after power-up, a change in temperature, or a change of the PGA.

At the completion of the calibration, the DRDY signal goes low, indicating the calibration is finished. The first output data of the converter after calibration is invalid because of the delay of the inside circuit, and the second output data is valid.

3.4.1 SYSTEM CALIBRATION

System calibration corrects the offset and gain errors of the chip and the system. When performing system calibration, appropriate signal must be applied to the inputs. The commands of system

calibration include OCALSYS and GCALSYS. The command OCALSYS corrects the offset error; the command GCALSYS corrects the gain error. Each calibration is finished in eight TDATA cycles.

The differential input voltage must be zero for offset calibration. The CS1160 computes the offset error for eliminating the system offset error.

The input voltage must be positive full-scale for gain calibration. The CS1160 computes the gain error for eliminating the system gain error.

3.5 EXTERNAL VOLTAGE REFERENCE

The CS1160 requires an external reference voltage which connects to REFP and REFN pins. The value can't exceed the supply voltage. The specific voltage value is shown in Table9:

Table 9 The Relation Between External Reference Voltage and RAN

RAN (ACR.2)	Power Voltage (V)	Reference Voltage (V)	Remark
0	5	<=2.5	
1	5	<=5	
0	3.0	<=1.25	
1	3.0	<=2.5	

3.6 CLOCK UNIT

The clock source for the CS1160 can be provided from external clock, a crystal, or oscillator. If the clock source is external clock, the clock is only connected to MCLK pin, and the XTAL pin is unused. If the source is a crystal, the clock circuit is shown in Figure5: (two capacitances of 10~20pF connect to the MCLK and XTAL pins)

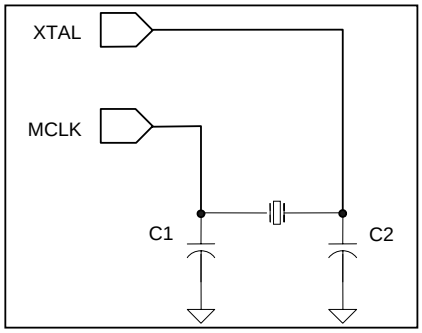


Figure 4 Schematic of Using External Crystal

3.7 DIGITAL FILTER (FIR)

The CS1160 has a programmable FIR filter which can be set to different data output rates. When the clock is 2.4576MHz, the data output rate can be set to 15Hz, 7.5Hz, or 3.75Hz. Under these conditions, the FIR filter rejects both 50Hz and 60Hz interference.

Using other clock frequency can get other data output rates, and the notch frequencies change simultaneously. For example, when the clock frequency is 3.6864MHZ, the register is under the default setting, and the data output rate is:

(3.6864MHz/2.4576MHz) ×15Hz = 22.5Hz

Notch frequency:

(3.6864MHz/2.4576MHz) ×(50Hz and 60Hz) = (75Hz and 90Hz)

3.8 SERIAL PERIPHERAL INTERFACE (SPI)

The CS1160 can communicate with external controller through the SPI bus. The CS1160 only operates in slave mode. The serial interface is a standard four-wire SPI interface, including CS, SCLK, SDI and SDO.

3.8.1 CHIP SELECT (CS)

Before communicating with the CS1160, the external controller must send the chip select (CS) signal to the chip. During communication, the CS signal must be maintained at low. When the CS signal is high, the entire SPI is reset. CS can be hard-wired low, the SPI bus can work in the three-wire mode which fits for communicating with external controller.

3.8.2 SERIAL CLOCK (SCLK)

The serial clock features a Schmitt-triggered input, which is used for sampling the SDI and SDO signals. The SCLK must be very clean to prevent the sample error. If the SCLK doesn't appear in three DRDY cycles, the SPI bus is reset on next SCLK and starts a new communication cycle. A special waveform can reset the entire chip. See the RESET chapter for more information.

3.8.3 DATA INPUT (SDI) and DATA OUTPUT (SDO)

The data input pin (SDI) and the data output pin (SDO) receive and send data. The SDO is high impendence when unused, allowing SDI and SDO to be connected together and driven by a bidirectional bus.

3.8.4 DATA READY (DRDY)

The DRDY signal is used for indicating the status of data registers. When the new data in the data output register (DOR) is ready, the DRDY signal goes low. After a read operation, the DRDY signal goes high. When the DOR register is ready to update, the DRDY goes high, which indicates the data in DOR can't be read.

The status of DRDY also can be got from the seventh bit of ACR register.

3.9 POWER-UP RESET and CHIP RESET

The power-on reset circuit is designed to reset the CS1160 automatically after power-up.
The CS1160 can be reset through two methods when the CS1160 is working: sending RESET command, or sending specific waveform on the SCLK (the SCLK RESET waveform, as shown in the Timing Diagram of the CS1160).

4 CS1160 REGISTER DESCRIPTION

The CS1160 configures the working mode through a series of control registers, which are used for controlling data format, data rate, calibration, etc.

4.1 RIGISTER LIST

Registers list is shown in Table 10:

Table 10 Registers List

Address	Register	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00H	SETUP	ID3	ID2	ID1	ID0	Reserved	PGA2	PGA1	PGA0
01H	MUX	0	0	0	0	0	0	0	1
02H	ACR	$\overline{\text{DRDY}}$	U/$\overline{\text{B}}$	SPEED	Reserved	BITOR	RAN	DR1	DR0
03H	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
04H	Reserved								
05H	Reserved								
06H	Reserved								
07H	OCC0	OCC07	OCC06	OCC05	OCC04	OCC03	OCC02	OCC01	OCC00
08H	OCC1	OCC15	OCC14	OCC13	OCC12	OCC11	OCC10	OCC09	OCC08
09H	OCC2	OCC23	OCC22	OCC21	OCC20	OCC19	OCC18	OCC17	OCC16
0AH	GCC0	GCC07	GCC06	GCC05	GCC04	GCC03	GCC02	GCC01	GCC00
0BH	GCC1	GCC15	GCC14	GCC13	GCC12	GCC11	GCC10	GCC09	GCC08
0CH	GCC2	GCC23	GCC22	GCC21	GCC20	GCC19	GCC18	GCC17	GCC16
0DH	DOR1	DOR15	DOR14	DOR13	DOR12	DOR11	DOR10	DOR09	DOR08
0EH	DOR0	DOR07	DOR06	DOR05	DOR04	DOR03	DOR02	DOR01	DOR00
0FH	Reserved	Nullity	Nullity	Nullity	Nullity	Nullity	Nullity	Nullity	Nullity

4.2 DETAILED REGISTER DEFINITIONS

SETUP Register (Address = 00H, Reset Value = xxxx0000) PGA Control

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID3	ID2	ID1	ID0	Reserved	PGA2	PGA1	PGA0

SETUP. 7—4 ： Code of the chip, factory programmed bits
SETUP. 3 ： Reserved
SETUP. 2—0 ： PGA2/PGA1/PGA0, Programmable Gain Amplifier Gain Selection
000 = 1 (Default)
001 = 2
010 = 4
011 = 8
100 = 16
101 = 32
110 = 64
111 = 128

MUX Register (Address = 01H, Reset Value = 00000001)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	1

When the value of MUX register is 00H, the input of ADC is shorted inside, and the output of the ADC is the NOISE of ADC. The register must be 01H in the normal use.

Analog Control Register (ACR) (Address = 02H, Reset Value = x0H) Analog Control

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$\overline{DRDY}$	U/$\overline{B}$	SPEED	Reserved	BITOR	RAN	DR1	DR0

ETUP.7 : $\overline{DRDY}$ (Data Ready), Read Only, Bit 7 duplicates the state of the $\overline{DRDY}$ signal.

SETUP.6 : U/$\overline{B}$, Data Format
0= Bipolar (Default);
+FSR Output 0x7FFFFFH, ZERO = 0x00000H, −FSR = 0x800000H;
1 = Unipolar;
+FSR Output 0xFFFFFFH, ZERO = 0x00000H, −FSR = 0x000000H;

SETUP.5 : SPEED, Modulator Clock Speed Control
0 = fosc/128 (Default)
1 = fosc/256;

SETUP.4 : BUF (Buffer Enable)
0 = BUF Disabled (Default);
1 = BUF Enabled;

SETUP.3 : BITOR, Set Bit Order For Output Data
0 = Most Significant Bit Transmitted First (Default);
1 = Least Significant Bit Transmitted First;

SETUP.2 : RAN, Range Selection
0 = Full-Scale Input Range Equal to +/−V_{REF} (default);
1 = Full-Scale Input Range Equal to +/−V_{REF} / 2;

SETUP.1-0 : DR1/DR0, (Data Rate)
00 = 15Hz (Default);
01 = 7.5Hz;
10 = 3.75Hz;
11 = Reserved

Offset Calibration Coefficient Register 0 (OCC0) (Address = 07H, Reset Value = 00H)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OCC07	OCC06	OCC05	OCC04	OCC03	OCC02	OCC01	OCC00

Offset calibration coefficient is composed of OCC0, OCC1 and OCC2. OCC23-00(totally 24 bits, OCC23 is MSB, OCC00 is LSB) is used for calibrating the offset error.

Offset Calibration Coefficient Register 1 (OCC1) (Address = 08H, Reset Value = 00H)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OCC15	OCC14	OCC13	OCC12	OCC11	OCC10	OCC09	OCC08

Offset calibration coefficient is composed of OCC0, OCC1 and OCC2. OCC23-00(totally 24 bits, OCC23 is MSB, OCC00 is LSB) is used for calibrating the offset error.

Offset Calibration Coefficient Register 2 (OCC2) (Address = 09H, Reset Value = 00H)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OCC23	OCC22	OCC21	OCC20	OCC19	OCC18	OCC17	OCC16

Offset calibration coefficient is composed of OCC0, OCC1 and OCC2. OCC23-00(totally 24 bits, OCC23 is MSB, OCC00 is LSB) is used for calibrating the offset error.

Gain Calibration Coefficient Register 0 (GCC0) (Address = 0AH, Reset Value = 59H)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GCC07	GCC06	GCC05	GCC04	GCC03	GCC02	GCC01	GCC00
Gain calibration coefficient is composed of GCC0, GCC1 and GCC2. GCC23-00(totally 24 bits, GCC23 is MSB, GCC00 is LSB) is used for calibrating the gain error.							

Gain Calibration Coefficient Register 1 (GCC1) (Address = 0BH, Reset Value = 55H)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GCC15	GCC14	GCC13	GCC12	GCC11	GCC10	GCC09	GCC08
Gain calibration coefficient is composed of GCC0, GCC1 and GCC2. GCC23-00(totally 24 bits, GCC23 is MSB, GCC00 is LSB) is used for calibrating the gain error.							

Gain Calibration Coefficient Register 2 (GCC2) (Address = 0CH, Reset Value = 55H)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GCC23	GCC22	GCC21	GCC20	GCC19	GCC18	GCC17	GCC16
Gain calibration coefficient is composed of GCC0, GCC1 and GCC2. GCC23-00(totally 24 bits, GCC23 is MSB, GCC00 is LSB) is used for calibrating the gain error.							

Data Output Register 1 (DOR1) (Address = 0DH, Reset Value = 00H) ADC Data

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DOR15	DOR14	DOR13	DOR12	DOR11	DOR10	DOR09	DOR08
ADC data is composed of DOR0 and DOR1. DOR15-00(totally 16 bits, DOR15 is MSB, DOR00 is LSB)							

Data Output Register 0 (DOR0) (Address = 0FH, Reset Value = 00H) ADC Data

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DOR07	DOR06	DOR05	DOR04	DOR03	DOR02	DOR01	DOR00
ADC data is composed of DOR0 and DOR1. DOR15-00(totally 16 bits, DOR15 is MSB, DOR00 is LSB)							

5 CS1160 COMMAND DESCRIPTION

The CS1160 has a series of commands, which control the working mode, working speed, calibration, etc. Some of the commands are single (such as RESET); some need operands (such as WREG, etc).

Operands:
n = Amount (0-127)
r = Register (0-15)
x = Arbitrary value

5.1 CS1160 COMMAND LIST

Commands aggregate of the CS1160 is shown in Table 11.

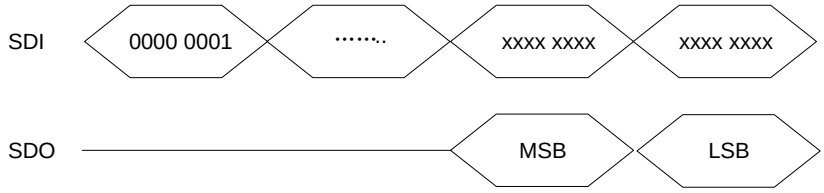
Table 11 Commands Table

COMMANDS	DESCRIPTION	OPERATE CODE	OPERANDS
RDATA	Read data from DOR register	0000 0001 (01_H)	--
RREG	Read value from "rrrr" register	0001 r r r r ($1X_H$)	xxxx_nnnn
WREG	Write value to "rrrr" register	0101 r r r r ($5X_H$)	xxxx_nnnn
OCALSYS	System offset calibration	1111 0011 ($F3_H$)	
GCALSYS	System gain calibration	1111 0100 ($F4_H$)	
WAKEUP	Wake up system from sleep mode	1111 1011 (FB_H)	
SYNC	Sync DRDY	1111 1100 (FC_H)	
SLEEP	Put in sleep mode	1111 1101 (FD_H)	
RESET	Reset to power-up value	1111 1110 (FE_H)	
NOTE: The received data format is always MSB first; the BITOR bit in ACR register sets the data out format.			

5.2 DETAILED COMMANDS DESCRIPTION

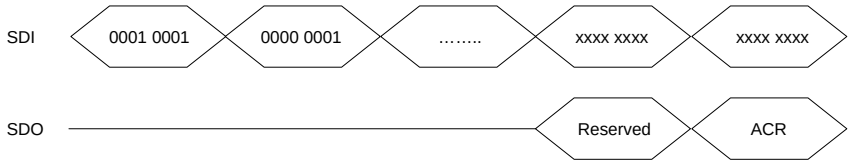
RDATA—Read Data from Data Output Register (DOR)

Description: Read the most recent conversion single data from the data output register (DOR). This is a 24-bit value, the last 8bis is nullity.
Operands: none
Byte: 1
Encoding: 0000 0001
Data transmit sequence:



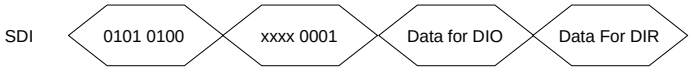
RREG—Read from Register

Description: Output the data from up to 16 registers, the starting register address is decided by operand in command. The number of registers read will be one plus the second byte. If the count exceeds the remaining registers, the addresses will wrap back to the beginning.
Operands: r, n
Byte: 2
Encoding: 0001 rrrr xxxx nnnn
Data transmit sequence:
Read 2 registers, starting with the register 01H (Reserved)



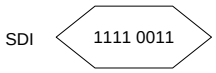
WREG—Write to Register

Description: Write multi-data to registers. The starting register address is decided by operand in command. The number of registers that will be written is one plus the value of the second byte.
Operands: r, n
Byte: 2
Encoding: 0101 rrrr xxxx nnnn
Data transmit sequence:
Write data to two registers, starting with the register 04H (DIO)



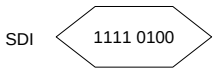
OCALSYS—System Offset Calibration

Description: Perform system offset calibration. For a system offset calibration, the input should be set to 0V, and the CS1160 computes the OCC value that will compensate for offset errors. The OCC value is updated after this operation. 0V signal must be applied to the analog inputs, and the OCC register is updated automatically.
Operands: none
Byte: 1
Encoding: 1111 0011
Data transmit sequence:



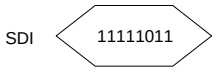
GCALSYS—System Gain Calibration

Description: Perform system gain calibration. For a system gain calibration, the input should be set to the full-scale voltage and the CS1160 computes the GCC value that will compensate for gain errors. GCC register value is updated after this operation. Full-scale voltage must be applied to the analog inputs, and the GCC register is updated automatically.
Operands: none
Byte: 1
Encoding: 1111 0100
Data transmit sequence:



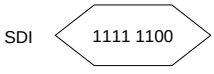
WAKEUP—Wake Up from The Sleep Mode

Description: Wake up the CS1160 from the sleep mode
Operands: none
Byte: 1
Encoding: 1111 1011
Data transmit sequence:



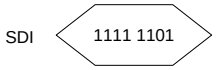
SYNC—Synchronize DRDY

Description: Synchronize the data of the CS1160
Operands: none
Byte: 1
Encoding: 1111 1100
Data transmit sequence:



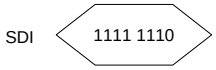
SLEEP—Sleep Mode

Description: Put the CS1160 into sleep mode. Use WAKEUP command to wake up from sleep mode.
Operands: none
Byte: 1
Encoding: 1111 1101
Data transmit sequence:



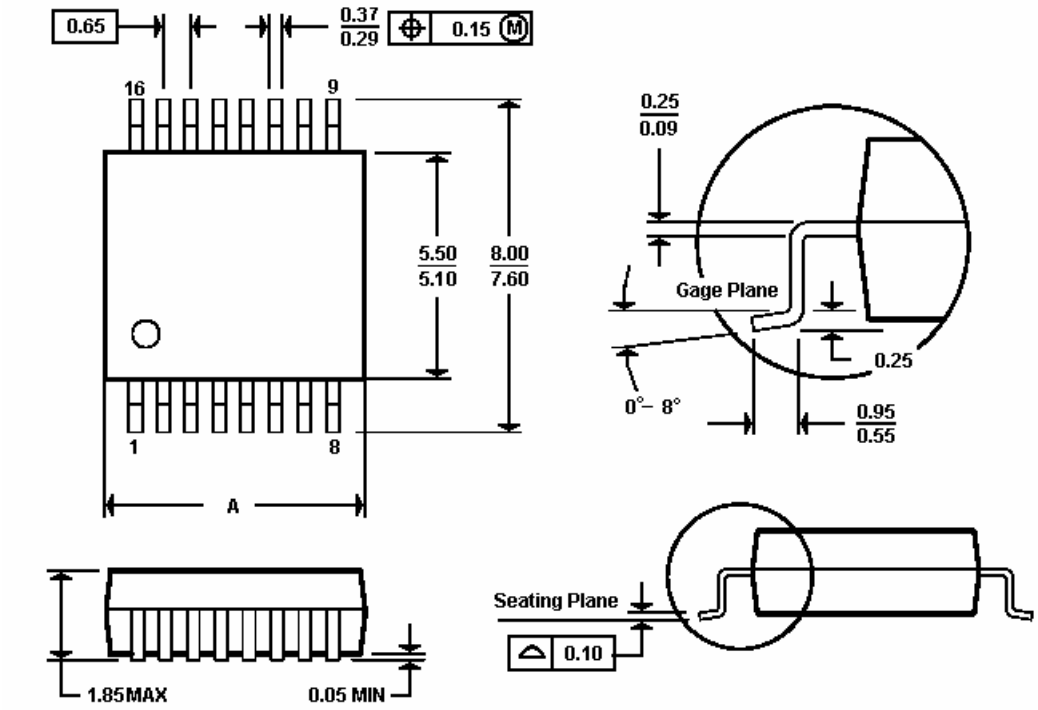
RESET—Reset to Power-up Value

Description: Restore the registers to their power-up values.
Operands: none
Byte: 1
Encoding: 1111 1110
Data transmit sequence:



6 CS1160 PACKAGE

The CS1160 uses SSOP16 packaging, shown in the following figure.



NOTES :

A. All linear dimensions are in millimeters
B. This drawing is subject to change without notice
C. Body demensions do not include mold flash or protrusion nont to exceed 0.15
D. Falls within JEDEC MO-150

A MAX	6.40
A MIN	6.00