CS4340

24-Bit, 96 kHz Stereo D/A Converter for Audio

Features

- 101 dB Dynamic Range
- -91 dB THD+N
- +3.0 V or +5.0 V Power Supply
- Low Clock Jitter Sensitivity
- Filtered Line-level Outputs
- On-chip Digital De-emphasis for 32, 44.1 and 48 kHz
- 33 mW with 3V Supply
- Popguard® Technology for Control of Clicks and Pops
- Lead-free Packaging Available

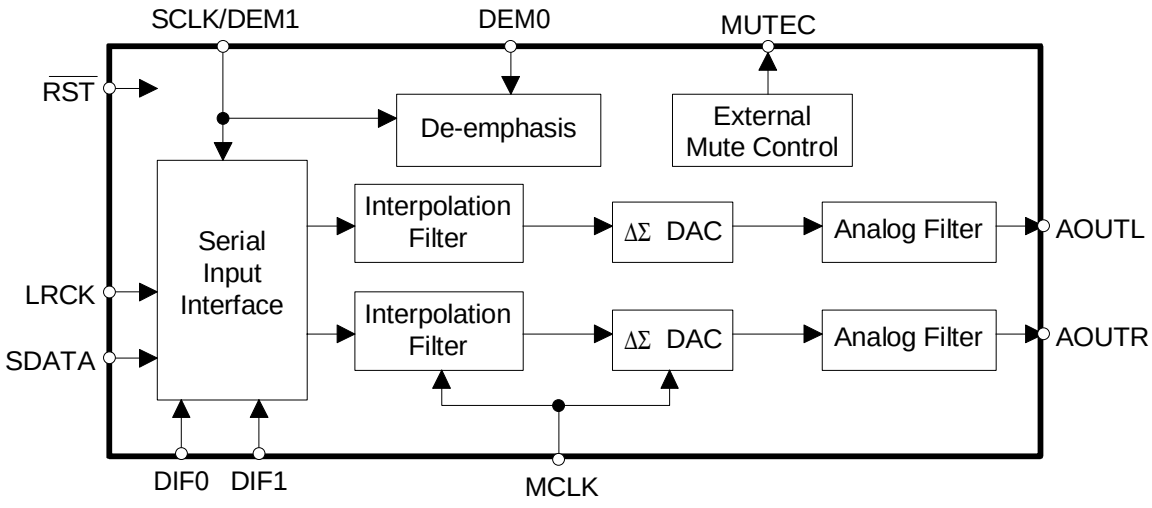
Description

The CS4340 is a complete stereo digital-to-analog system including digital interpolation, fourth-order delta-sigma digital-to-analog conversion, digital de-emphasis and switched capacitor analog filtering. The advantages of this architecture include: ideal differential linearity, no distortion mechanisms due to resistor matching errors, no linearity drift over time and temperature and a high tolerance to clock jitter.

The CS4340 accepts data at audio sample rates from 4 kHz to 100 kHz, consumes very little power, and operates over a wide power supply range. The features of the CS4340 are ideal for DVD players, CD players, set-top box and automotive systems.

ORDERING INFORMATION

CS4340-DSZ	16-pin SOIC, Lead Free,	-40 to 85 °C
CS4340-KS	16-pin SOIC	-10 to 70 °C
CS4340-KSZ	16-pin SOIC, Lead Free,	-10 to 70 °C
CS4340-CZZ	16-pin TSSOP, Lead Free,	-10 to 70 °C
CDB4340	Evaluation Board	



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Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find one nearest you go to **www.cirrus.com**

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1. CHARACTERISTICS AND SPECIFICATIONS

(Min/Max performance characteristics and specifications are guaranteed over the Specified Operating Conditions. Typical performance characteristics are derived from measurements taken at T_A = 25°C.)

SPECIFIED OPERATING CONDITIONS (All voltages with respect to AGND = 0 V.)

Parameters		Symbol	Min	Nom	Max	Units
DC Power Supply						
	Nominal 3.3V	VA	2.7	3.3	3.6	V
	Nominal 5.0V	VA	4.75	5.0	5.5	V
Specified Operating Temperature	-KS/KSZ/CZZ	T_A	-10	-	+70	°C
(Power Applied)	-DSZ	T_A	-40		+85	°C

ABSOLUTE MAXIMUM RATINGS (AGND = 0 V; all voltages with respect to AGND. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.)

Parameters		Symbol	Min	Max	Units
DC Power Supply		VA	-0.3	6.0	V
Input Current	(Note 1)	I_{in}	-	±10	mA
Digital Input Voltage		V_{IND}	-0.3	VA+0.4	V
Ambient Operating Temperature (power applied)		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

Notes: 1. Any pin except supplies.

ANALOG CHARACTERISTICS (CS4340-KS/KSZ/CZZ)

(Test conditions (unless otherwise specified): Input test signal is a 997 Hz sine wave at 0 dBFS; measurement bandwidth is 10 Hz to 20 kHz; test load R_L = 10 kΩ, C_L = 10 pF (see Figure 1).)

Parameter		VA = 5.0 V			VA = 3.0 V			Unit
		Min	Typ	Max	Min	Typ	Max	
Single-Speed Mode	**Fs = 48 kHz**							
Dynamic Range	(Note 2)							
18 to 24-Bit	unweighted	93	98	-	89	94	-	dB
	A-Weighted	96	101	-	92	97	-	dB
16-Bit	unweighted	-	92	-	-	92	-	dB
	A-Weighted	-	95	-	-	95	-	dB
Total Harmonic Distortion + Noise	(Note 2)							
18 to 24-Bit	0 dB	-	-91	-86	-	-94	-89	dB
	-20 dB	-	-78	-	-	-74	-	dB
	-60 dB	-	-38	-	-	-34	-	dB
16-Bit	0 dB	-	-90	-	-	-91	-	dB
	-20 dB	-	-72	-	-	-72	-	dB
	-60 dB	-	-32	-	-	-32	-	dB
Double-Speed Mode	**Fs = 96 kHz**							
Dynamic Range	(Note 2)							
18 to 24-Bit	unweighted	93	98	-	89	94	-	dB
	A-Weighted	96	101	-	92	97	-	dB
16-Bit	unweighted	-	92	-	-	92	-	dB
	A-Weighted	-	95	-	-	95	-	dB
Total Harmonic Distortion + Noise	(Note 2)							
18 to 24-Bit	0 dB	-	-91	-86	-	-94	-89	dB
	-20 dB	-	-78	-	-	-74	-	dB
	-60 dB	-	-38	-	-	-34	-	dB
16-Bit	0 dB	-	-90	-	-	-91	-	dB
	-20 dB	-	-72	-	-	-72	-	dB
	-60 dB	-	-32	-	-	-32	-	dB

ANALOG CHARACTERISTICS (CS4340-KS/KSZ/CZZ) (Continued)

Parameters	Symbol	Min	Typ	Max	Units
Dynamic Performance for All Modes					
Interchannel Isolation (1 kHz)		-	102	-	dB
DC Accuracy					
Interchannel Gain Mismatch		-	0.1	-	dB
Gain Drift		-	±100	-	ppm/°C
Analog Output Characteristics and Specifications					
Full Scale Output Voltage		0.6•VA	0.7•VA	0.8•VA	Vpp
Output Impedance		-	100	-	Ω
Minimum AC-Load Resistance (Note 3)	R_L	-	3	-	kΩ
Maximum Load Capacitance (Note 3)	C_L	-	100	-	pF

Notes: 2. One-half LSB of triangular PDF dither is added to data.

3. Refer to Figure 2.

.

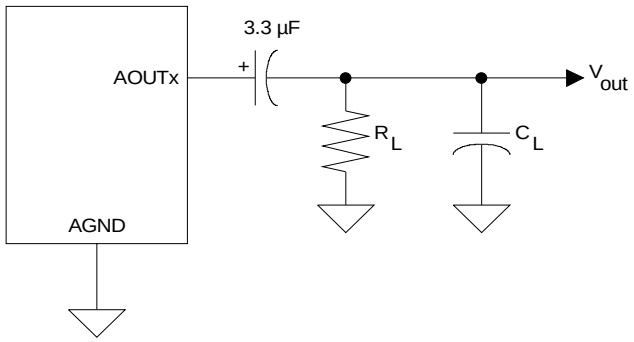


Figure 1. Output Test Load

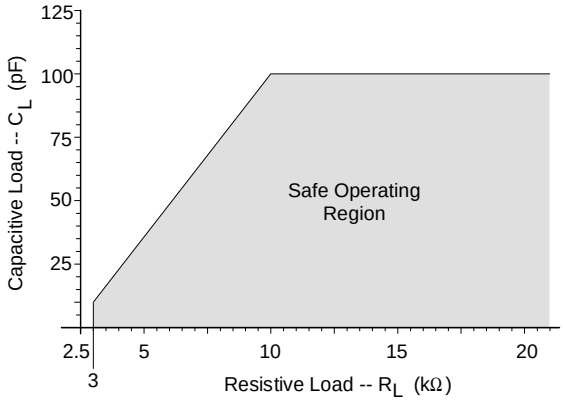


Figure 2. Maximum Loading

ANALOG CHARACTERISTICS (CS4340-DSZ) (Test conditions (unless otherwise specified): Input test signal is a 997 Hz sine wave at 0 dBFS; measurement bandwidth is 10 Hz to 20 kHz; test load R_L = 10 kΩ, C_L = 10 pF (see Figure 1).)

Parameter		VA = 5.0 V Min	VA = 5.0 V Typ	VA = 5.0 V Max	VA = 3.0 V Min	VA = 3.0 V Typ	VA = 3.0 V Max	Unit
Single-Speed Mode	**Fs = 48 kHz**							
Dynamic Range	(Note 2)							
18 to 24-Bit	unweighted	93	98	-	89	94	-	dB
	A-Weighted	96	101	-	92	97	-	dB
16-Bit	unweighted	-	92	-	-	92	-	dB
	A-Weighted	-	95	-	-	95	-	dB
Total Harmonic Distortion + Noise	(Note 2)							
18 to 24-Bit	0 dB	-	-91	-86	-	-94	-87	dB
	-20 dB	-	-78	-	-	-74	-	dB
	-60 dB	-	-38	-	-	-34	-	dB
16-Bit	0 dB	-	-90	-	-	-91	-	dB
	-20 dB	-	-72	-	-	-72	-	dB
	-60 dB	-	-32	-	-	-32	-	dB
Double-Speed Mode	**Fs = 96 kHz**							
Dynamic Range	(Note 2)							
18 to 24-Bit	unweighted	93	98	-	89	94	-	dB
	A-Weighted	96	101	-	92	97	-	dB
16-Bit	unweighted	-	92	-	-	92	-	dB
	A-Weighted	-	95	-	-	95	-	dB
Total Harmonic Distortion + Noise	(Note 2)							
18 to 24-Bit	0 dB	-	-91	-86	-	-94	-87	dB
	-20 dB	-	-78	-	-	-74	-	dB
	-60 dB	-	-38	-	-	-34	-	dB
16-Bit	0 dB	-	-90	-	-	-91	-	dB
	-20 dB	-	-72	-	-	-72	-	dB
	-60 dB	-	-32	-	-	-32	-	dB

ANALOG CHARACTERISTICS (CS4340-DSZ) (Continued)

Parameters	Symbol	Min	Typ	Max	Units
Dynamic Performance for All Modes					
Interchannel Isolation (1 kHz)		-	102	-	dB
DC Accuracy					
Interchannel Gain Mismatch		-	0.1	-	dB
Gain Drift		-	±100	-	ppm/°C
Analog Output Characteristics and Specifications					
Full Scale Output Voltage		0.6•VA	0.7•VA	0.8•VA	Vpp
Output Impedance		-	100	-	Ω
Minimum AC-Load Resistance (Note 3)	R_L	-	3	-	kΩ
Maximum Load Capacitance (Note 3)	C_L	-	100	-	pF

COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE (The filter characteristics and the X-axis of the response plots have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs.)

Parameter		Min	Typ	Max	Unit
Single-Speed Mode - (4 kHz to 50 kHz sample rates)					
Passband					
	to -0.05 dB corner	0	-	0.4535	Fs
	to -3 dB corner	0	-	0.4998	Fs
Frequency Response 10 Hz to 20 kHz		-0.02	-	+0.08	dB
StopBand		0.5465	-	-	Fs
StopBand Attenuation (Note 4)		50	-	-	dB
Group Delay		-	9/Fs	-	s
Passband Group Delay Deviation	0 - 20 kHz	-	±0.36/Fs	-	s
De-emphasis Error (Relative to 1 kHz) (Note 5)	Fs = 44.1 kHz	-	-	+0.05/-0.14	dB
Double-Speed Mode - (50 kHz to 100 kHz sample rates)					
Passband					
	to -0.1 dB corner	0	-	0.4621	Fs
	to -3 dB corner	0	-	0.4982	Fs
Frequency Response 10 Hz to 20 kHz		-0.06	-	+0.2	dB
StopBand		0.577	-	-	Fs
StopBand Attenuation (Note 4)		55	-	-	dB
Group Delay		-	4/Fs	-	s
Passband Group Delay Deviation	0 - 40 kHz	-	±1.39/Fs	-	s
	0 - 20 kHz	-	±0.23/Fs	-	s

Notes: 4. For Single-Speed Mode, the measurement bandwidth is 0.5465 Fs to 3 Fs.
For Double-Speed Mode, the measurement bandwidth is 0.577 Fs to 1.4 Fs.

5. De-emphasis is only available in Single-Speed Mode.

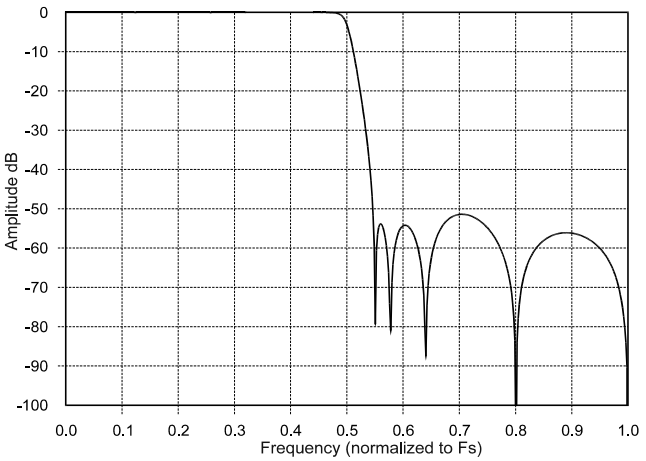


Figure 3. Single-Speed Stopband Rejection

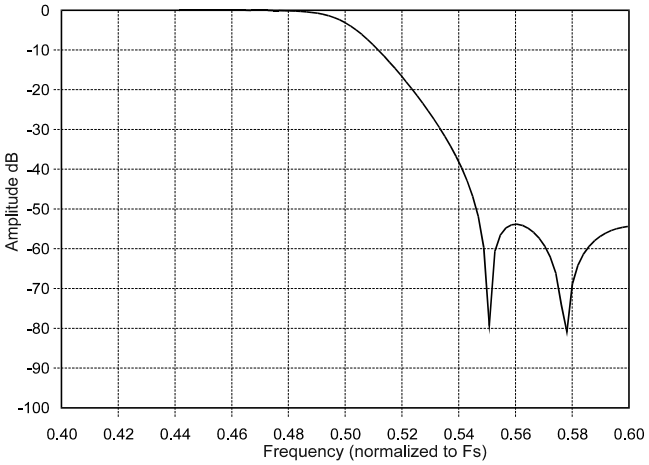


Figure 4. Single-Speed Transition Band

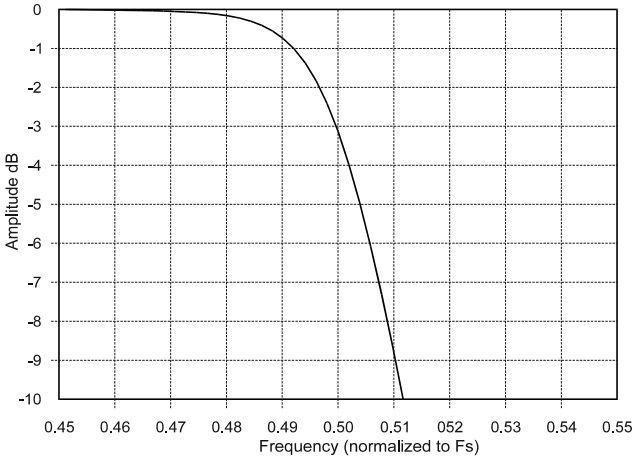


Figure 5. Single-Speed Transition Band (Detail)

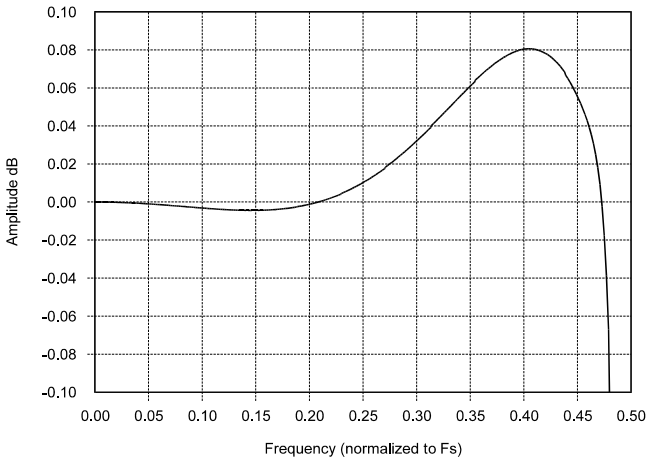


Figure 6. Single-Speed Passband Ripple

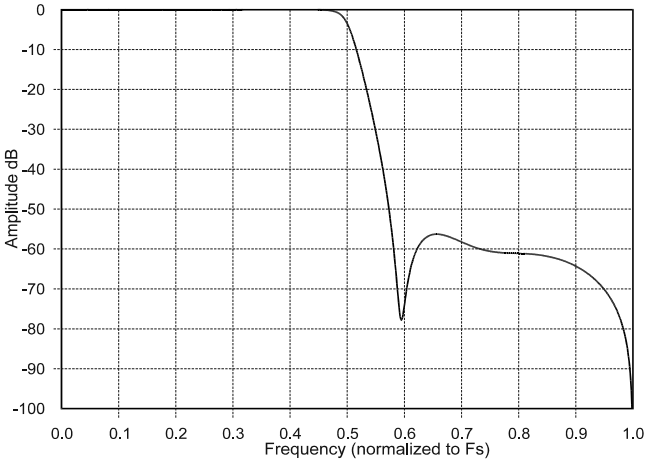


Figure 7. Double-Speed Stopband Rejection

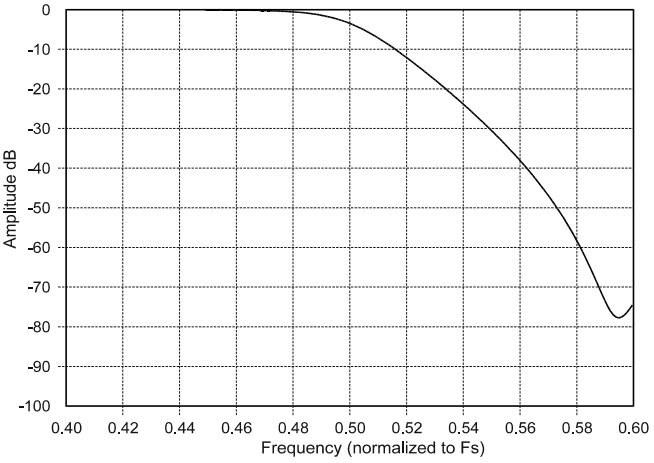


Figure 8. Double-Speed Transition Band

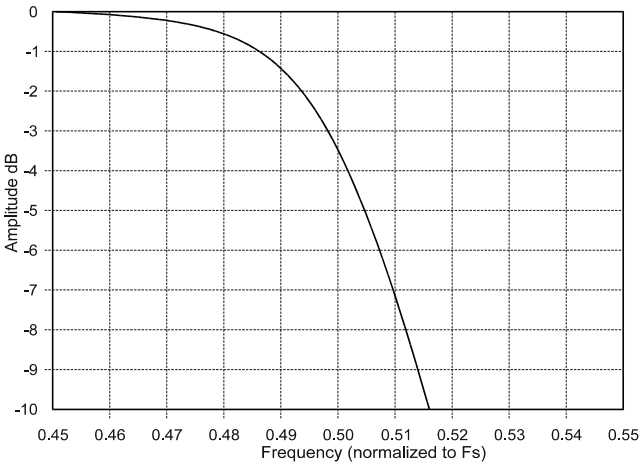


Figure 9. Double-Speed Transition Band (Detail)

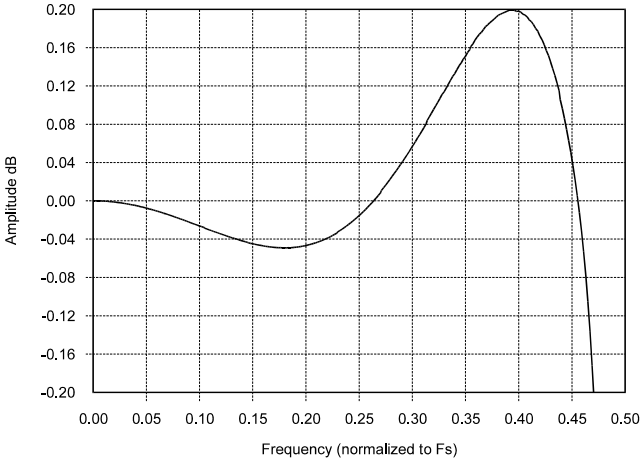


Figure 10. Double-Speed Passband Ripple

SWITCHING SPECIFICATIONS - SERIAL AUDIO INTERFACE

Parameters		Symbol	Min	Max	Units
MCLK Frequency			1.024	25.6	MHz
MCLK Duty Cycle			45	55	%
Input Sample Rate	Single-Speed Mode Double-Speed Mode	Fs Fs	4 50	50 100	kHz kHz
LRCK Duty Cycle			40	60	%
SCLK Pulse Width Low		t_{sclkl}	20	-	ns
SCLK Pulse Width High		t_{sclkh}	20	-	ns
SCLK Frequency	Single-Speed Mode Double-Speed Mode		- -	128xFs 64xFs	Hz Hz
SCLK rising to LRCK edge delay		t_{slrd}	20	-	ns
SCLK rising to LRCK edge setup time		t_{slrs}	20	-	ns
SDIN valid to SCLK rising setup time		t_{sdlrs}	20	-	ns
SCLK rising to SDIN hold time		t_{sdh}	20	-	ns

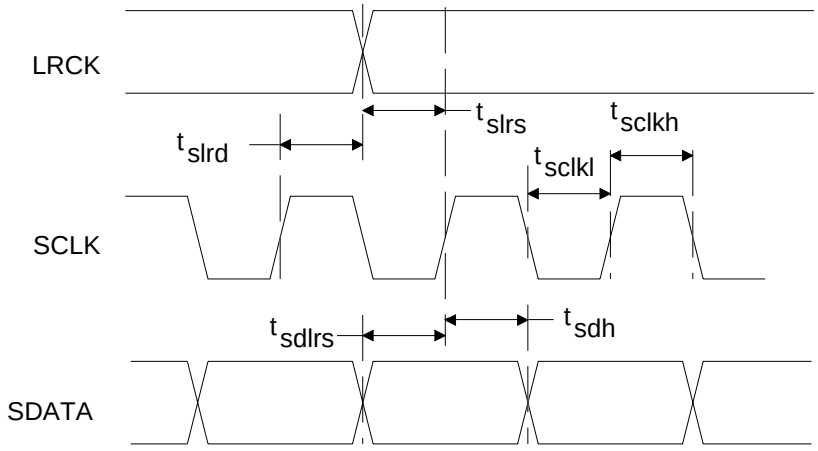


Figure 11. Serial Input Timing (External SCLK)

SWITCHING CHARACTERISTICS - INTERNAL SERIAL CLOCK

Parameters	Symbol	Min	Typ	Max	Units
MCLK Frequency		1.024	-	25.6	MHz
MCLK Duty Cycle		45	-	55	%
Input Sample Rate Single-Speed Mode Double-Speed Mode	Fs Fs	4 50	- -	50 100	kHz kHz
LRCK Duty Cycle			(Note 6)		%
SCLK Period (Note 7)	t_{sclkw}	$\frac{1}{SCLK}$	-	-	s
SCLK rising to LRCK edge	t_{sclkr}	-	$\frac{t_{sclkw}}{2}$	-	s
SDATA valid to SCLK rising setup time	t_{sdlrs}	$\frac{1}{(512)Fs} + 10$	-	-	ns
SCLK rising to SDATA hold time MCLK / LRCK = 512, 256 or 128	t_{sdh}	$\frac{1}{(512)Fs} + 15$	-	-	ns
SCLK rising to SDATA hold time MCLK / LRCK = 384 or 192	t_{sdh}	$\frac{1}{(384)Fs} + 15$	-	-	ns

Notes: 6. The Duty Cycle must be 50% +/– 1/2 MCLK Period.

7. See section 4.2.1 for derived internal frequencies.

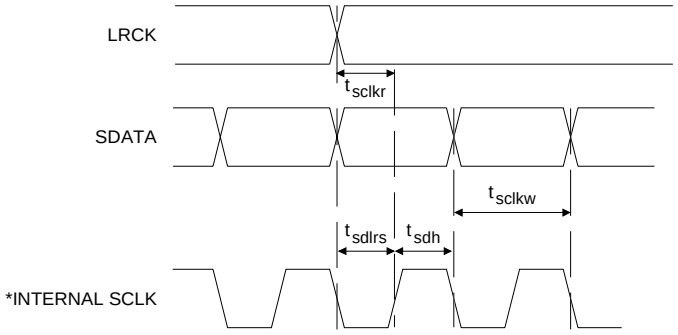


Figure 12. Internal Serial Mode Input Timing

*The SCLK pulses shown are internal to the CS4340.

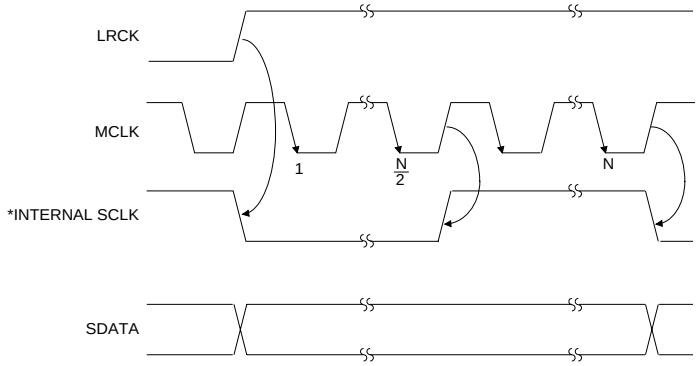


Figure 13. Internal Serial Clock Generation

* The SCLK pulses shown are internal to the CS4340. N equals MCLK divided by SCLK

DC ELECTRICAL CHARACTERISTICS (AGND = 0 V; all voltages with respect to AGND.)

Parameters		Symbol	Min	Typ	Max	Units
Normal Operation (Note 8)						
Power Supply Current	VA = 5.0 V	I_A	-	15	18	mA
	VA = 3.0 V	I_A	-	11	14	mA
Power Dissipation	VA = 5.0 V		-	75	90	mW
	VA = 3.0 V		-	33	42	mW
Power-down Mode (Note 9)						
Power Supply Current	VA = 5.0 V	I_A	-	60	-	µA
	VA = 3.0 V		-	30	-	µA
Power Dissipation	VA = 5.0 V		-	0.3	-	mW
	VA = 3.0 V		-	0.09	-	mW
All Modes of Operation						
Power Supply Rejection Ratio (Note 10)	1 kHz	PSRR	-	60	-	dB
	60 Hz		-	40	-	dB
V_Q Nominal Voltage			-	0.45•VA	-	V
Output Impedance			-	250	-	kΩ
Maximum allowable DC current source/sink			-	0.01	-	mA
Filt+ Nominal Voltage			-	VA	-	V
Output Impedance			-	250	-	kΩ
Maximum allowable DC current source/sink			-	0.01	-	mA
MUTEC Low-Level Output Voltage			-	0	-	V
MUTEC High-Level Output Voltage			-	VA	-	V
Maximum MUTEC Drive Current			-	3	-	mA

Notes: 8. Normal operation is defined as $\overline{RST}$ = HI with a 997 Hz, 0 dBFS input sampled at the highest Fs for each speed mode, and open outputs, unless otherwise specified.

9. Power Down Mode is defined as $\overline{RST}$ = LO with all clocks and data lines held static.

10. Valid with the recommended capacitor values on FILT+ and VQ as shown in Figure 14. Increasing the capacitance will also increase the PSRR.

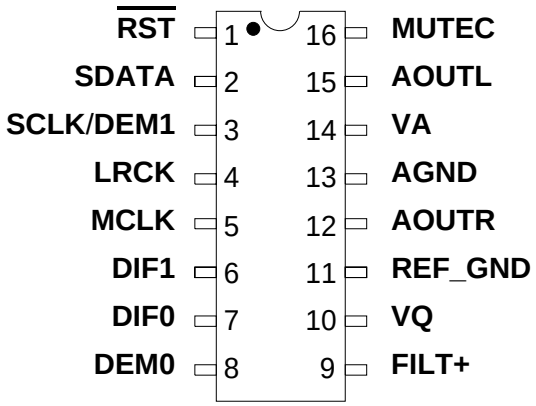
DIGITAL INPUT CHARACTERISTICS (AGND = 0 V; all voltages with respect to AGND.)

Parameters	Symbol	Min	Typ	Max	Units
Input Leakage Current	I_{in}	-	-	±10	µA
Input Capacitance		-	8	-	pF

DIGITAL INTERFACE SPECIFICATIONS (AGND = 0 V; all voltages with respect to AGND.)

Parameters	Symbol	Min	Max	Units
3.3 V Logic *(3.0 V to 3.6 V DC Supply)*				
High-Level Input Voltage	V_{IH}	2.0	-	V
Low-Level Input Voltage	V_{IL}	-	0.8	V
5.0 V Logic *(4.75 V to 5.25 V DC Supply)*				
High-Level Input Voltage	V_{IH}	2.0	-	V
Low-Level Input Voltage	V_{IL}	-	0.8	V

2. PIN DESCRIPTION



Pin Name	#	Pin Description
RST	1	**Reset** (*Input*) - Powers down device.
SDATA	2	**Serial Audio Data** (*Input*) - Input for two's complement serial audio data.
SCLK	3	**Serial Clock** (*Input*) -Serial clock for the serial audio interface.
DEM1 **DEM0**	3 8	**De-emphasis Control** (*Input*) - Selects the standard 15 µs/50 µs digital de-emphasis filter response for 44.1 kHz sample rate.
LRCK	4	**Left Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
MCLK	5	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
DIF1 **DIF0**	6 7	**Digital Interface Format** (I*nput*) - Defines the required relationship between the Left Right Clock, Serial Clock and Serial Audio Data.
FILT+	9	**Positive Voltage Reference** (*Output*) **-** Positive voltage reference for the internal sampling circuits.
VQ	10	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent reference voltage.
REF_GND	11	**Reference Ground** (*Input*) - Ground reference for the internal sampling circuits.
AOUTR **AOUTL**	12 15	**Analog Outputs** (*Output*) - The full scale analog output level is specified in the *Analog Characteristics* table.
AGND	13	**Analog Ground** (*Input*)
VA	14	**Power** (*Input*) **-** Positive power for the analog, digital and serial audio interface sections.
MUTEC	16	**Mute Control** (*Output*) - Control signal for an optional mute circuit.

3. TYPICAL CONNECTION DIAGRAM

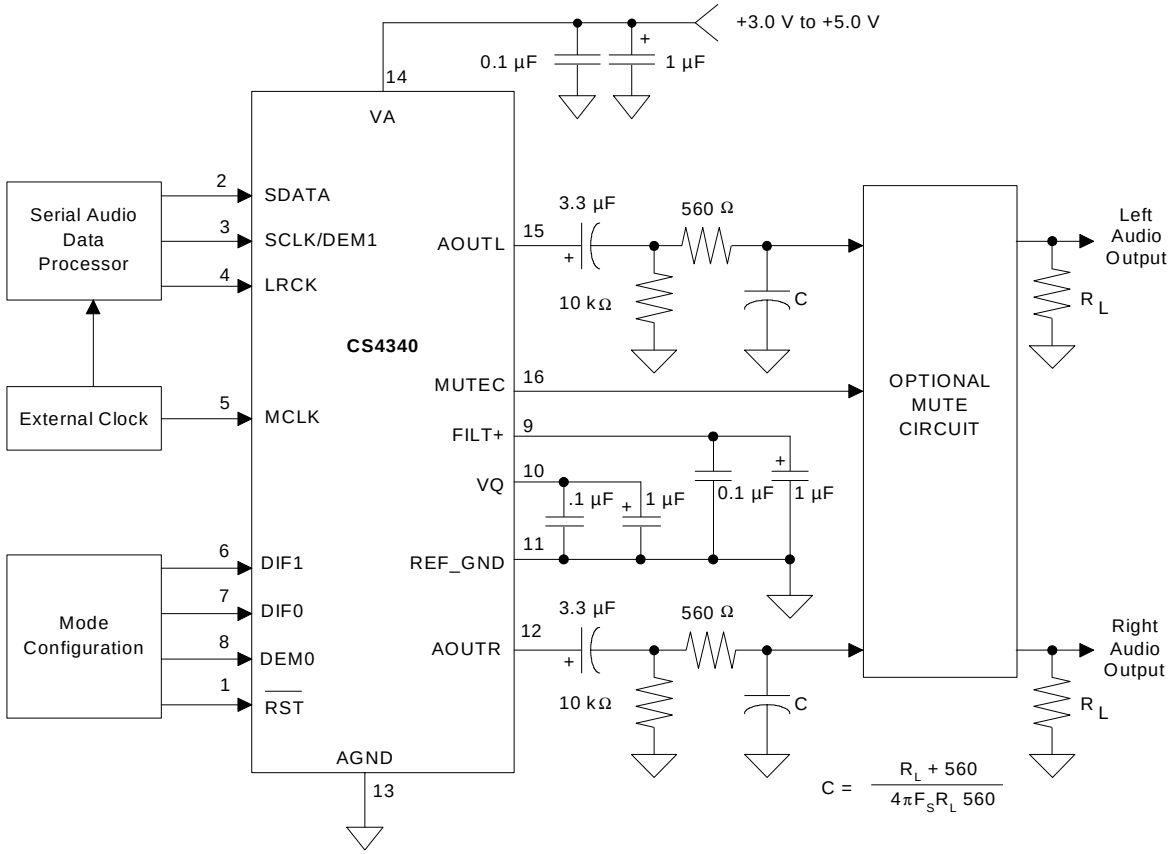


Figure 14. Typical Connection Diagram

4. APPLICATIONS

4.1 Sample Rate Range/Operational Mode

The device operates in one of two operational modes determined by the Master Clock to Left/Right Clock ratio (see section 4.2). Sample rates outside the specified range for each mode are not supported.

Input Sample Rate (Fs)	MODE
4 kHz - 50 kHz	Single-Speed Mode
50 kHz - 100 kHz	Double-Speed Mode

Table 1. CS4340 Speed Modes

4.2 System Clocking

The device requires external generation of the master (MCLK) and left/right (LRCK) clocks. The device also requires external generation of the serial clock (SCLK) if the internal serial clock is not used. The LRCK, defined also as the input sample rate Fs, must be synchronously derived from MCLK according to specified ratios. The specified ratios of MCLK to LRCK, along with several standard audio sample rates and the required MCLK frequency, are illustrated in Tables 2 and 3.

Sample Rate (kHz)	MCLK (MHz)		
	256x	384x	512x
32	8.1920	12.2880	16.3840
44.1	11.2896	16.9344	22.5792
48	12.2880	18.4320	24.5760

Table 2. Single-Speed Mode Standard Frequencies

Sample Rate (kHz)	MCLK (MHz)	
	128x	192x
64	8.1920	12.2880
88.2	11.2896	16.9344
96	12.2880	18.4320

Table 3. Double-Speed Mode Standard Frequencies

4.2.1 Internal Serial Clock Mode

The device will enter the Internal Serial Clock Mode if no low to high transitions are detected on the SCLK pin for 2 consecutive periods of LRCK. In this mode, the SCLK is internally derived and synchronous with MCLK and LRCK. The SCLK/LRCK ratio is either 32, 48, or 64 depending upon the MCLK/LRCK ratio and the Digital Interface Format selection (see Table 4).

The internal serial clock is utilized when additional de-emphasis control is required. Operation in the Internal Serial Clock mode is identical to operation with an external SCLK synchronized with LRCK; however, External SCLK mode is recommended for system clocking applications.

Input MCLK/LRCK Ratio	Digital Interface Format Selection				Internal SCLK/LRCK Ratio
	I^2S up to 24 Bits	*Left Justified 24 Bits*	*Right Justified 24 Bits*	*Right Justified 16 Bits*	
512, 256, 128	X	-	-	X	32
384, 192	X	X	X	X	48
512, 256, 128	-	X	X	-	64

Table 4. Internal SCLK/LRCK Ratio

4.2.2 External Serial Clock Mode

The device will enter the External Serial Clock Mode whenever 16 low to high transitions are detected on the SCLK pin during any phase of the LRCK period. The device will revert to Internal Serial Clock Mode if no low to high transitions are detected on the SCLK pin for 2 consecutive periods of LRCK.

4.3 Digital Interface Format

The device will accept audio samples in several digital interface formats as illustrated in Table 5. The desired format is selected via the DIF1 and DIF0 pins. For an illustration of the required relationship between LRCK, SCLK and SDIN, see Figures 15 through 18.

DIF1	DIF0	DESCRIPTION	FORMAT	FIGURE
0	0	I^2S, up to 24-bit data	0	15
0	1	Left Justified, up to 24-bit data	1	16
1	0	Right Justified, 24-bit Data	2	17
1	1	Right Justified, 16-bit Data	3	18

Table 5. Digital Interface Format - DIF1 and DIF0

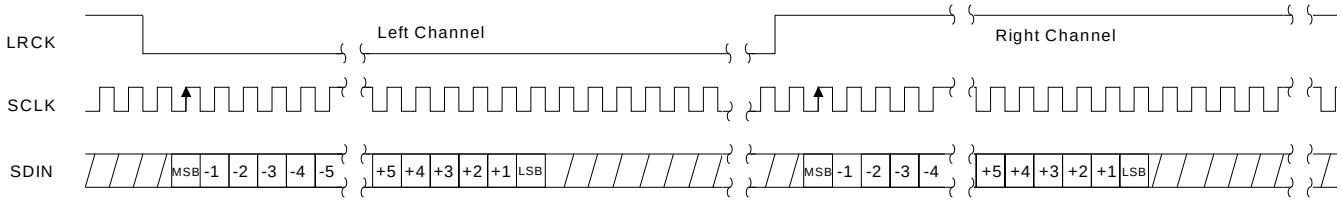


Figure 15. CS4340 Format 0 - I^2S up to 24-Bit Data

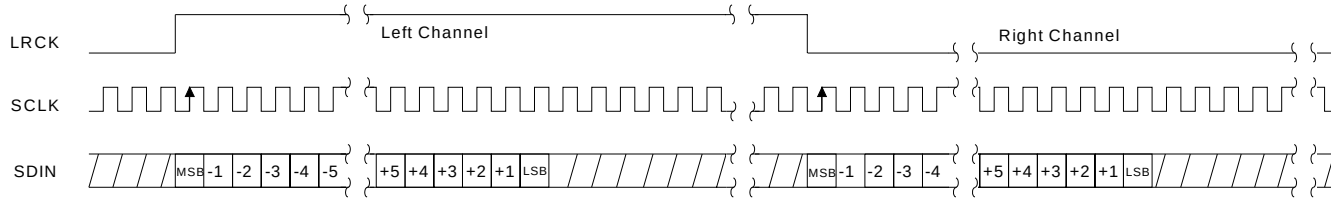


Figure 16. CS4340 Format 1 - Left Justified up to 24-Bit Data

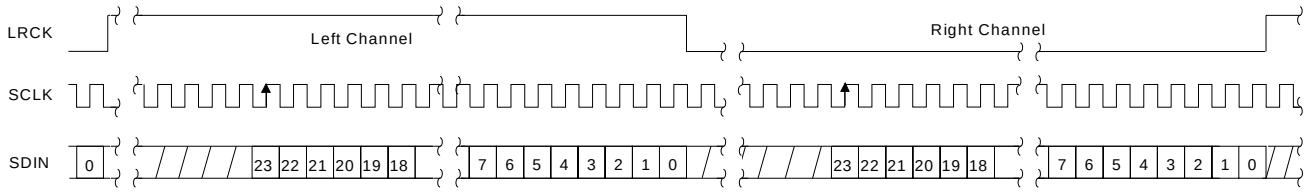


Figure 17. CS4340 Format 2 - Right Justified, 24-Bit Data

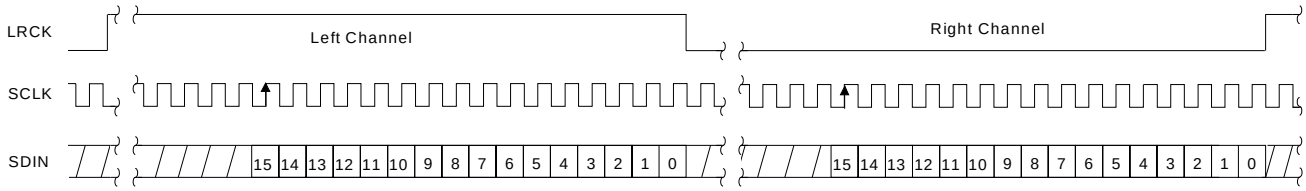


Figure 18. CS4340 Format 3 - Right Justified, 16-Bit Data

4.4 De-Emphasis

The device includes on-chip digital de-emphasis. Figure 19 shows the de-emphasis curve for Fs equal to 44.1 kHz. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, Fs.

Pin 8 is available for de-emphasis control and selects the 44.1 kHz de-emphasis filter. If the Internal Serial Clock is used, pin 3 is also available for additional de-emphasis control and, in combination with pin 8, selects either the 32, 44.1, or 48 kHz de-emphasis filter. Please see Table 6 for the desired de-emphasis control.

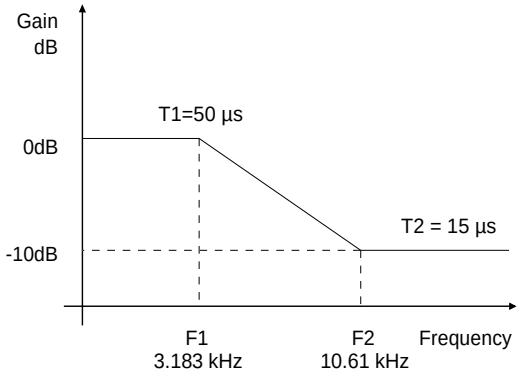


Figure 19. De-Emphasis Curve

Internal SCLK		
DEM1	**DEM0**	**Description**
0	0	Disabled
0	1	44.1 kHz
1	0	48 kHz
1	1	32 kHz

External SCLK	
DEM0	**Description**
0	Disabled
1	44.1 kHz

Table 6. De-Emphasis Control

4.5 Power-up Sequence

Reliable power-up can be accomplished by keeping the device in reset until the power supply and configuration pins are stable, and the clocks are locked to the appropriate frequencies discussed in section 4.2. It is also recommended that reset be enabled if the analog supply drops below the minimum specified operating voltage to prevent power glitch related issues.

4.6 Popguard® Transient Control

The CS4340 uses Popguard® technology to minimize the effects of output transients during power-up and power-down. This technology, when used with external DC-blocking capacitors in series with the audio outputs, minimizes the audio transients commonly produced by single-ended single-supply converters. It is activated inside the DAC when $\overline{\text{RST}}$ is enabled/disabled and requires no other external control, aside from choosing the appropriate DC-blocking capacitors.

4.6.1 Power-up

When the device is initially powered-up, the audio outputs, AOUTL and AOUTR, are clamped to AGND. Following a delay of approximately 1000 sample periods, each output begins to ramp toward the quiescent voltage. Approximately 10,000 LRCK cycles later, the outputs reach V_Q and audio output begins. This gradual voltage ramping allows time for the external DC-blocking capacitors to charge to the quiescent voltage, minimizing the power-up transient.

4.6.2 Power-down

To prevent transients at power-down, the device must first enter its power-down state by enabling $\overline{\text{RST}}$. When this occurs, audio output ceases and the internal output buffers are disconnected from AOUTL and AOUTR. In their place, a soft-start current sink is substituted which allows the DC-blocking capacitors to slowly discharge. Once this charge is dissipated, the power to the device may be turned off and the system is ready for the next power-on.

4.6.3 Discharge Time

To prevent an audio transient at the next power-on, it is necessary to ensure that the DC-blocking capacitors have fully discharged before turning on the power or exiting the power-down state. If not, a transient will occur when the audio outputs are initially clamped to AGND. The time that the device must remain in the power-down state is related to the value of the DC-blocking capacitance. For example, with a 3.3 µF capacitor, the minimum power-down time will be approximately 0.4 seconds.

4.7 Mute Control

The Mute Control pin goes high during power-up initialization, reset, or if the MCLK to LRCK ratio is incorrect. The pin will also go high following the reception of 8192 consecutive audio samples of static 0 or -1 on both the left and right channels. A single sample of non-zero data on either channel will cause the Mute Control pin to go low. This pin is intended to be used as a control for an external mute circuit to prevent the clicks and pops that can occur in any single-ended single supply system.

Use of the Mute Control function is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops. Also, use of the Mute Control function can enable the system designer to achieve idle channel noise/signal-to-noise ratios which are only limited by the external mute circuit. See the CDB4340 data sheet for a suggested mute circuit.

4.8 Grounding and Power Supply Arrangements

As with any high resolution converter, the CS4340 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 14 shows the recommended power arrangements, with VA connected to a clean supply. If the ground planes are split between digital ground and analog ground, REF_GND & AGND should be connected to the analog ground plane.

Decoupling capacitors should be as close to the DAC as possible, with the low value ceramic capacitor being the closest. To further minimize impedance, these capacitors should be located on the same layer as the DAC.

All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the modulators. The FILT+ and VQ decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from FILT+ and REF_GND (as well as VQ and REF_GND), and should also be located on the same layer as the DAC. The CDB4340 evaluation board demonstrates the optimum layout and power supply arrangements.

5. PARAMETER DEFINITIONS

Total Harmonic Distortion + Noise (THD+N)

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Dynamic Range

The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full scale analog output for a full scale digital input.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

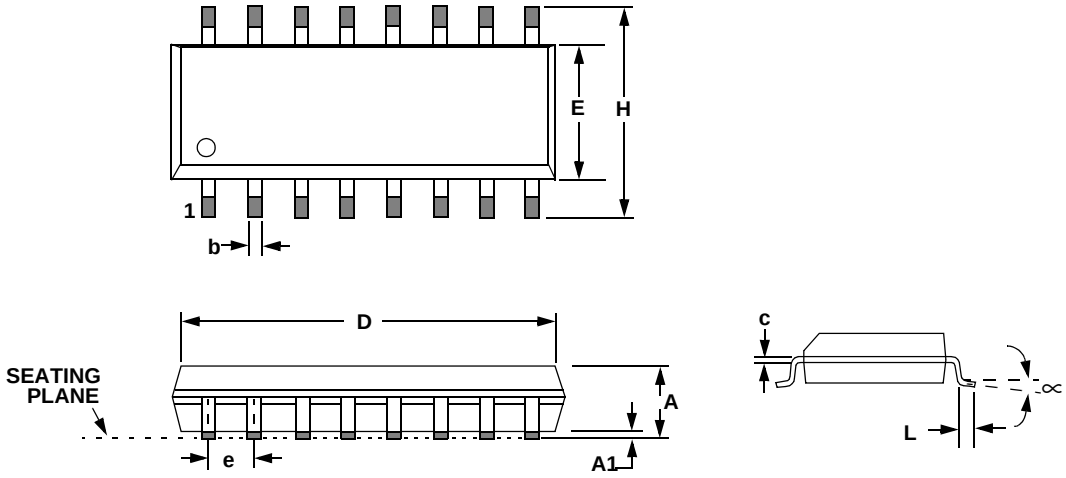
6. REFERENCES

1) CDB4340 Evaluation Board Datasheet

7. PACKAGE DIMENSIONS

7.1 SOIC

16L SOIC (150 MIL BODY) PACKAGE DRAWING



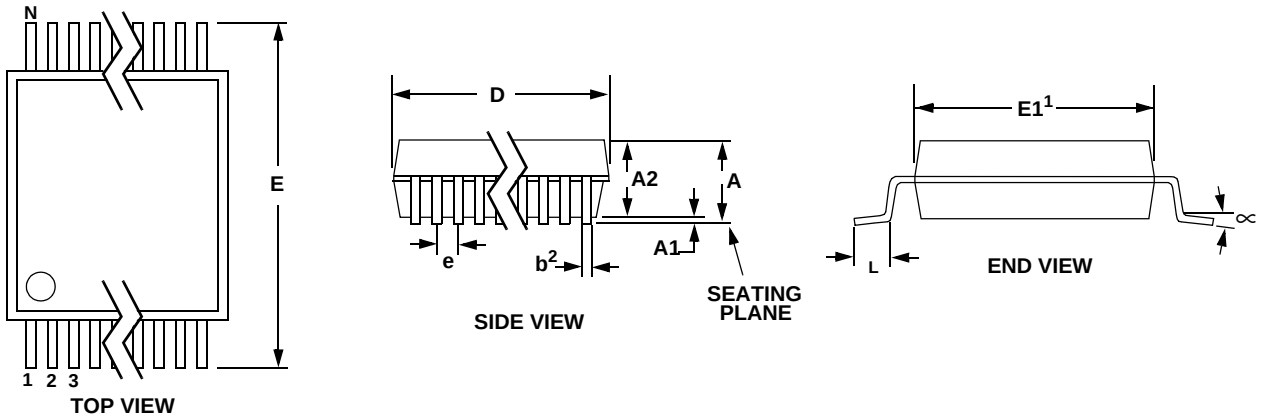
	INCHES			MILLIMETERS		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	0.053	0.064	0.069	1.35	1.63	1.75
A1	0.004	0.006	0.010	0.10	0.15	0.25
b	0.013	0.016	0.020	0.33	0.41	0.51
C	0.0075	0.008	0.010	0.19	0.20	0.25
D	0.386	0.390	0.394	9.80	9.91	10.00
E	0.150	0.154	0.157	3.80	3.90	4.00
e	0.040	0.050	0.060	1.02	1.27	1.52
H	0.228	0.236	0.244	5.80	6.0	6.20
L	0.016	0.025	0.050	0.40	0.64	1.27
∝	0°	4°	8°	0°	4°	8°

JEDEC #: MS-012

Controling Dimension is Millimeters

7.2 TSSOP

16L TSSOP (4.4 mm BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.043	--	--	1.10	
A1	0.002	0.004	0.006	0.05	--	0.15	
A2	0.03346	0.0354	0.037	0.85	0.90	0.95	
b	0.00748	0.0096	0.012	0.19	0.245	0.30	2,3
D	0.193	0.1969	0.201	4.90	5.00	5.10	1
E	0.248	0.2519	0.256	6.30	6.40	6.50	
E1	0.169	0.1732	0.177	4.30	4.40	4.50	1
e	--	0.026 BSC	--	--	0.065 BSC	--	
L	0.020	0.024	0.028	0.50	0.60	0.70	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-153

Controlling Dimension is Millimeters

Notes:
1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

8. PACKAGE THERMAL RESISTANCE

Package		Symbol	Min	Typ	Max	Units
SOIC	(for multi-layer boards)	θ_{JA}	-	74	-	°C/Watt
TSSOP	(for multi-layer boards)	θ_{JA}	-	89	-	°C/Watt