



# STH200N55F3-2

N-channel 55 V, 1.8 mΩ, 160 A, H<sup>2</sup>PAK  
STripFET™ III Power MOSFET

Preliminary data

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub> (1)
STH200N55F3-2	55 V	< 2.6 mΩ	160 A

1. Current limited by package

- Ultra low on-resistance
- 100% avalanche tested

## Application

- Switching applications

## Description

This STripFET™ III Power MOSFET technology is among the latest improvements, which have been especially tailored to minimize on-state resistance providing superior switching performance.

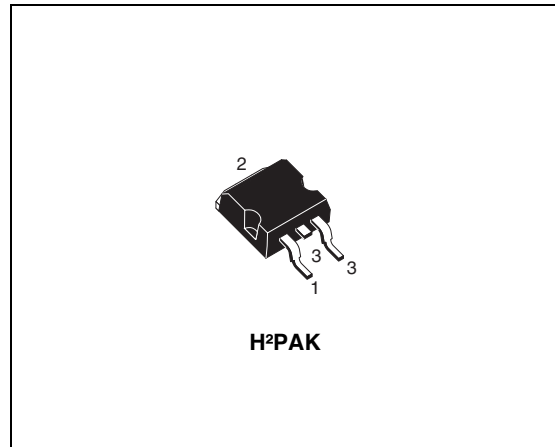


Figure 1. Internal schematic diagram

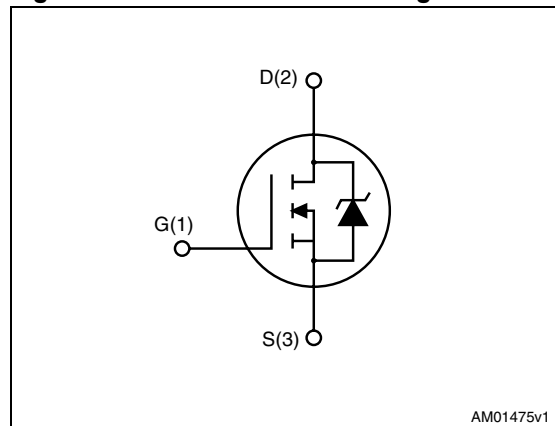


Table 1. Device summary

Order code	Marking	Package	Packaging
STH200N55F3-2	200N55F3	H <sup>2</sup> PAK	Tape and reel

## Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	55	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	160	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	160	A
$I_{DM}^{(2)}$	Drain current (pulsed)	640	A
$P_{TOT}^{(3)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	300	W
	Derating factor	2.0	W/ $^\circ\text{C}$
$E_{AS}^{(4)}$	Single pulse avalanche energy	1.0	J
$T_{stg}$	Storage temperature	-55 to 175	$^\circ\text{C}$
$T_J$	Operating junction temperature		

1. Current limited by package
2. Pulse width limited by safe operating area
3. This value is rated according to Rthj-c
4. Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $I_D = 60\text{ A}$ ,  $V_{DD} = 35\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max	0.5	$^\circ\text{C}/\text{W}$
Rthj-pcb <sup>(1)</sup>	Thermal resistance junction-pcb max	35	$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch<sup>2</sup> FR-4 2 oz Cu

## 2 Electrical characteristics

( $T_{\text{case}} = 25\text{ °C}$  unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$ , $V_{\text{GS}} = 0$	55			V
$I_{\text{DSS}}$	Zero gate voltage drain current ( $V_{\text{GS}} = 0$ )	$V_{\text{DS}} = \text{Max rating}$ , $V_{\text{DS}} = \text{Max rating}$ , $T_c = 125\text{ °C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{\text{GSS}}$	Gate body leakage current ( $V_{\text{DS}} = 0$ )	$V_{\text{DS}} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$ , $I_D = 250\ \mu\text{A}$	2		4	V
$R_{\text{DS(on)}}$	Static drain-source on resistance	$V_{\text{GS}} = 10\text{ V}$ , $I_D = 60\text{ A}$		1.8	2.6	$\text{m}\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{\text{ISS}}$	Input capacitance			6800		pF
$C_{\text{OSS}}$	Output capacitance	$V_{\text{DS}} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{\text{GS}} = 0$	-	1450	-	pF
$C_{\text{RSS}}$	Reverse transfer capacitance					
$Q_g$	Total gate charge	$V_{\text{DD}} = 44\text{ V}$ , $I_D = 120\text{ A}$ ,		100		nC
$Q_{\text{gs}}$	Gate-source charge	$V_{\text{GS}} = 10\text{ V}$		30		nC
$Q_{\text{gd}}$	Gate-drain charge	<a href="#">Figure 3</a>		26		nC

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time Rise time	$V_{DD} = 27.5\text{ V}$ , $I_D = 60\text{ A}$ $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ , <i>Figure 2</i>	-	25 150	-	ns ns
$t_{d(off)}$ $t_f$	Turn-off delay time Fall time	$V_{DD} = 27.5\text{ V}$ , $I_D = 60\text{ A}$ $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ , <i>Figure 2</i>	-	110 50	-	ns ns

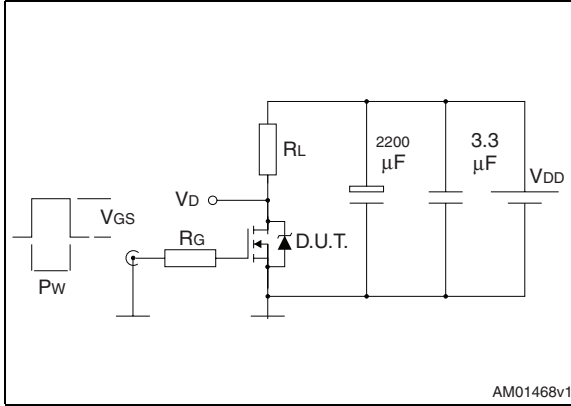
**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		160	A
$I_{SD}^{(1)}$	Source-drain current (pulsed)		-		640	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 160\text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 120\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	-	60		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 35\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$	-	110		nC
$I_{RRM}$	Reverse recovery current	<i>Figure 7</i>	-	3.5		A

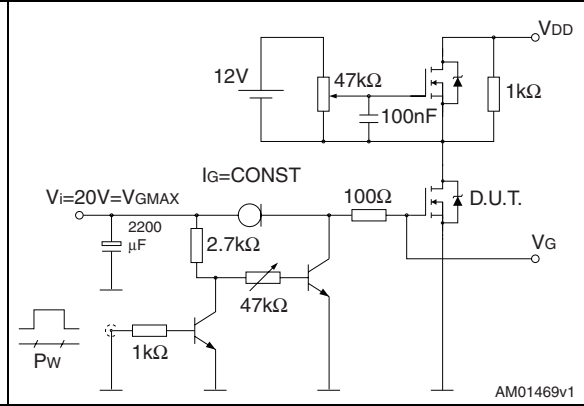
1. Pulse width limited by safe operating area
2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

### 3 Test circuits

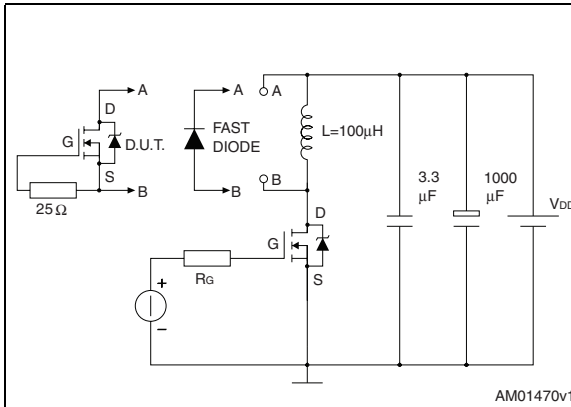
**Figure 2. Switching times test circuit for resistive load**



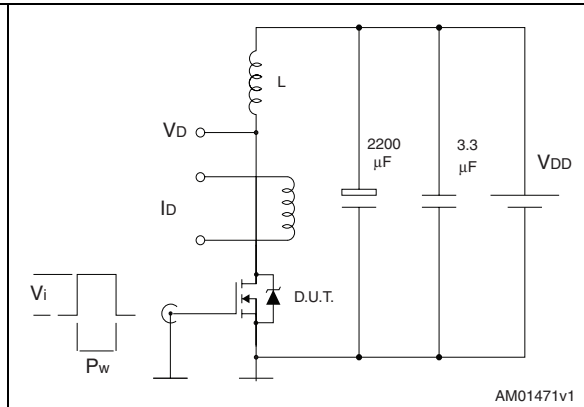
**Figure 3. Gate charge test circuit**



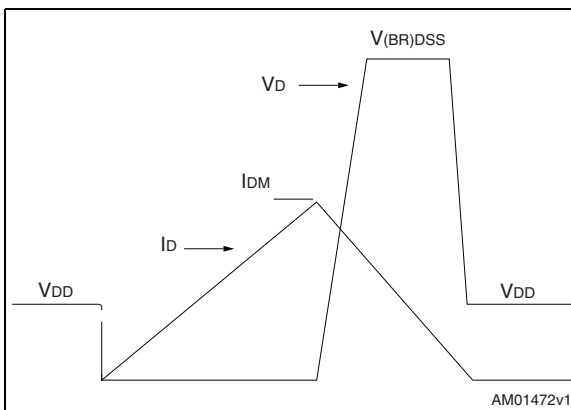
**Figure 4. Test circuit for inductive load switching and diode recovery times**



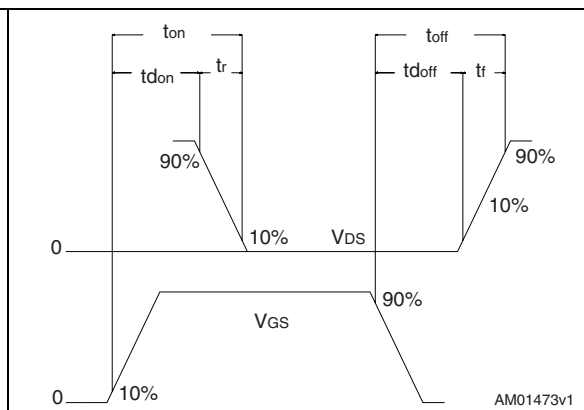
**Figure 5. Unclamped inductive load test circuit**



**Figure 6. Unclamped inductive waveform**



**Figure 7. Switching time waveform**



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 8. H<sup>2</sup>PAK 2 leads mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.80
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.171		7.971
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	7.45		7.85
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°



Figure 8. H<sup>2</sup>PAK 2 leads drawing

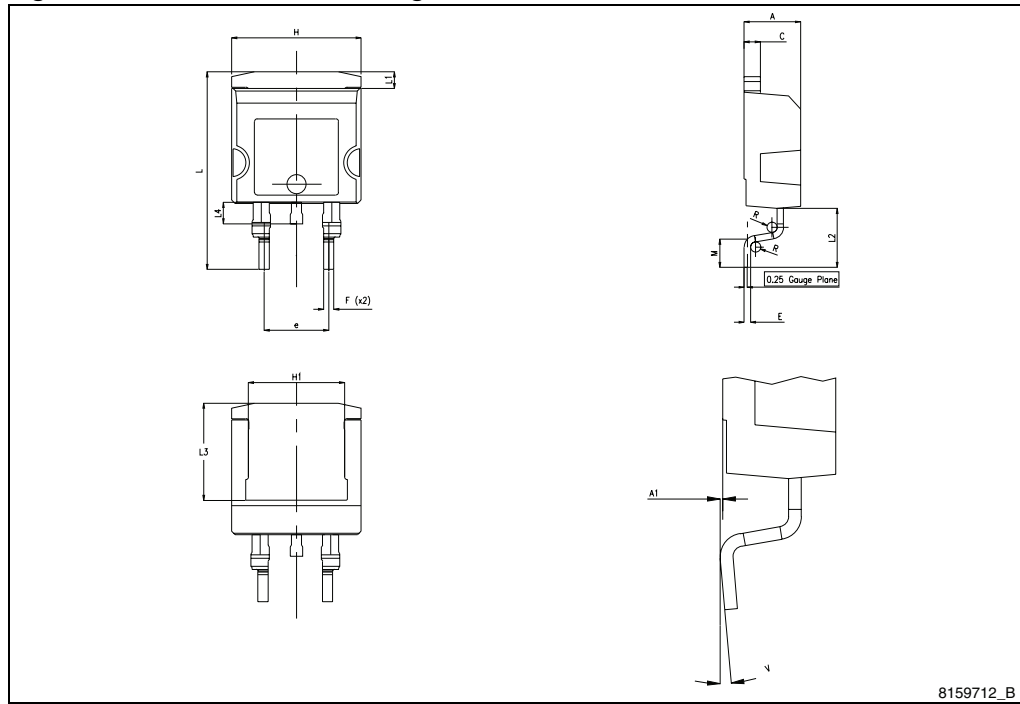
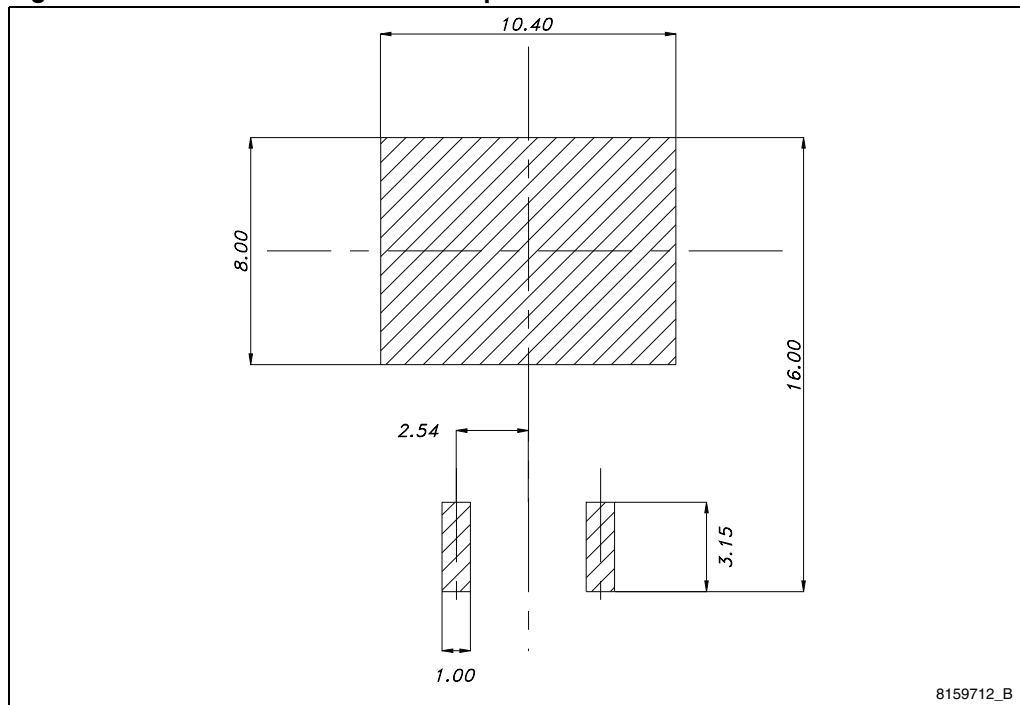


Figure 9. H<sup>2</sup>PAK 2 recommended footprint



## 5 Revision history

Table 9. Document revision history

Date	Revision	Changes
30-Jul-2009	1	First release.

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