# **Product Preview**

# N-Channel Power MOSFET 600 V, 0.75 $\Omega$

#### **Features**

- Low ON Resistance
- Low Gate Charge
- Zener Diode-protected Gate
- 100% Avalanche Tested
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

#### ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25°C unless otherwise noted)

Rating	Symbol	Тур	Unit	
Drain-to-Source Voltage	$V_{DSS}$	600	V	
Continuous Drain Current, $R_{\theta JC}$	I <sub>D</sub>	10 (Note 2)	Α	
Continuous Drain Current $T_A = 100$ °C, $R_{\theta JC}$	I <sub>D</sub>	5.7 (Note 2)	Α	
Pulsed Drain Current, V <sub>GS</sub> @ 10 V	I <sub>DM</sub>	36 (Note 2)	Α	
Power Dissipation, $R_{\theta JC}$ (Note 1)	$P_{D}$	36	W	
Gate-to-Source Voltage	$V_{GS}$	±30	V	
Single Pulse Avalanche Energy, L = 6.0 mH, I <sub>D</sub> = 10 A	E <sub>AS</sub>	300	mJ	
ESD (HBM) (JESD22-A114)	V <sub>esd</sub>	3900	V	
RMS Isolation Voltage (t = 0.3 sec., R.H. $\leq$ 30%, T <sub>A</sub> = 25°C) (Figure 14)	V <sub>ISO</sub>	4500	V	
Peak Diode Recovery	dv/dt	4.5 (Note 3)	V/ns	
Continuous Source Current (Body Diode)	IS	10	Α	
Maximum Temperature for Soldering Leads	TL	260	°C	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- 1. Surface mounted on FR4 board using 1 in sq. pad size, 1 oz cu
- 2. Limited by maximum junction temperature
- 3.  $I_S \le 10 \text{ A}$ ,  $di/dt \le 200 \text{ A/}\mu\text{s}$ ,  $V_{DD} = 80\% \text{ BV}_{DSS}$

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.



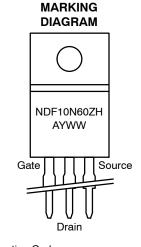
## ON Semiconductor®

#### http://onsemi.com

V <sub>DSS</sub>	R <sub>DS(ON)</sub> (MAX) @ 5 A
600 V	0.75 Ω



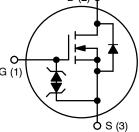
TO-220FP CASE 221AH STYLE 1



A = Location Code Y = Year WW = Work Week

H = Halogen Free Package

# N-Channel D (2) O



#### **ORDERING INFORMATION**

Device	Package	Shipping
NDF10N60ZH	TO-220FP	50 Units / Rail (In Development)

## THERMAL RESISTANCE

Parameter	Symbol	Тур	Unit
Junction-to-Case (Drain)	$R_{ heta JC}$	3.4	°C/W
Junction-to-Ambient Steady State (Note 4)	$R_{ heta JA}$	50	

# **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Test Conditions		Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS					-	•	
Drain-to-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA		BV <sub>DSS</sub>	600			V
Breakdown Voltage Temperature Coefficient	Reference to 25°C, I <sub>D</sub> = 1 mA		$\Delta BV_{DSS}/ \ \Delta T_{J}$		0.6		V/°C
Drain-to-Source Leakage Current	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V	25°C	I <sub>DSS</sub>			1	μΑ
		125°C				50	
Gate-to-Source Forward Leakage	V <sub>GS</sub> = ±20 V		I <sub>GSS</sub>			±10	μΑ
ON CHARACTERISTICS (Note 5)							
Static Drain-to-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5.0 A		R <sub>DS(on)</sub>		0.65	0.75	Ω
Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 100 μA		V <sub>GS(th)</sub>	3.0		4.5	V
Forward Transconductance	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 A		9 <sub>FS</sub>		7.9		S
OYNAMIC CHARACTERISTICS							
Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		C <sub>iss</sub>		1425		pF
Output Capacitance			C <sub>oss</sub>		150		
Reverse Transfer Capacitance			C <sub>rss</sub>		35		
Total Gate Charge			$Q_g$		47		nC
Gate-to-Source Charge	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 10 A,		Q <sub>gs</sub>		9.0		1
Gate-to-Drain ("Miller") Charge	V <sub>GS</sub> = 10 V		$Q_{gd}$		26		
Plateau Voltage			$V_{GP}$		6.3		V
Gate Resistance	1		$R_{g}$		1.5		Ω
RESISTIVE SWITCHING CHARACTER	ISTICS				-	-	-
Turn-On Delay Time			t <sub>d(on)</sub>		15		ns
Rise Time	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 10 /	Α,	t <sub>r</sub>		31		
Turn-Off Delay Time	$V_{GS}$ = 10 V, $R_{G}$ = 5 $\Omega$		t <sub>d(off)</sub>		40		
Fall Time			t <sub>f</sub>		23		
OURCE-DRAIN DIODE CHARACTER	RISTICS (T <sub>C</sub> = 25°C unless oth	erwise not	ed)				·
Diode Forward Voltage	I <sub>S</sub> = 10 A, V <sub>GS</sub> = 0 V		$V_{SD}$			1.6	V
Reverse Recovery Time	V <sub>GS</sub> = 0 V, V <sub>DD</sub> = 30 V I <sub>S</sub> = 10 A, di/dt = 100 A/μs		t <sub>rr</sub>		395		ns
Reverse Recovery Charge			Q <sub>rr</sub>		3.0		μС

Insertion mounted
 Pulse Width ≤ 380 μs, Duty Cycle ≤ 2%.

#### TYPICAL CHARACTERISTICS

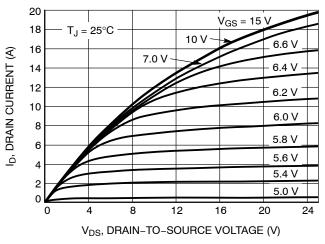


Figure 1. On-Region Characteristics

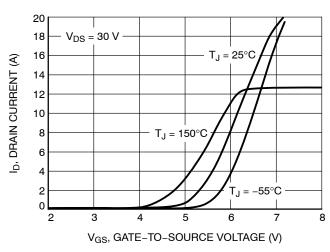


Figure 2. Transfer Characteristics

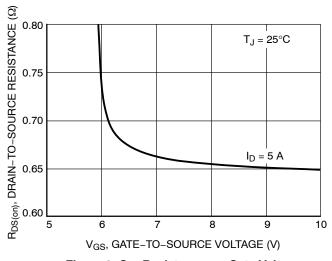


Figure 3. On-Resistance vs. Gate Voltage

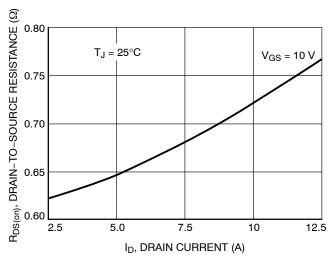


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

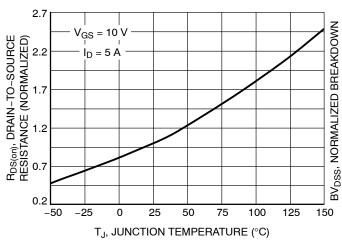


Figure 5. On–Resistance Variation with Temperature

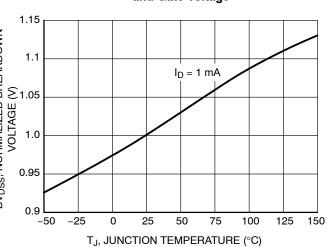


Figure 6. BVDSS Variation with Temperature

#### **TYPICAL CHARACTERISTICS**

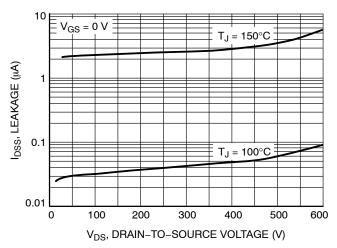


Figure 7. Drain-to-Source Leakage Current vs. Voltage

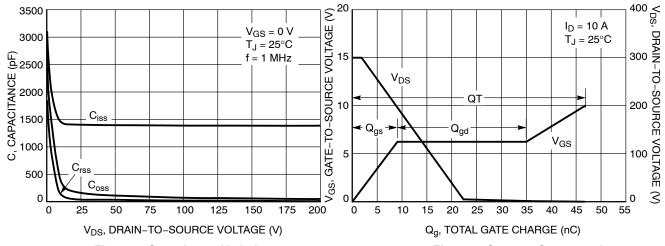


Figure 8. Capacitance Variation

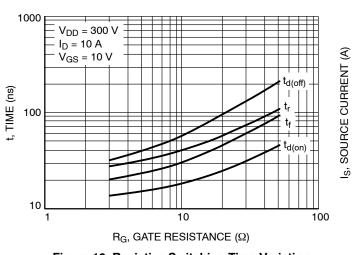


Figure 10. Resistive Switching Time Variation vs. Gate Resistance

Figure 9. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

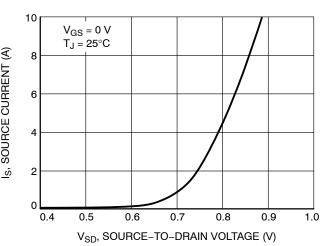


Figure 11. Diode Source Current vs. Forward Voltage

#### **TYPICAL CHARACTERISTICS**

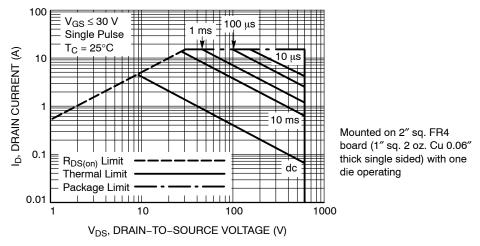


Figure 12. Maximum Rated Forward Biased Safe Operating Area

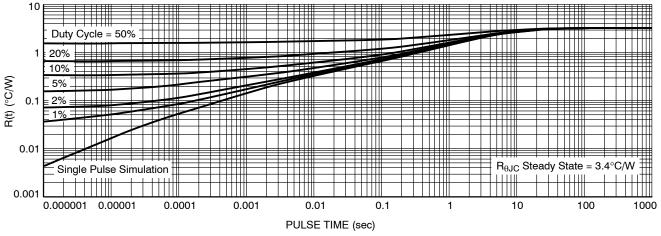


Figure 13. Thermal Impedance (Junction-to-Case)

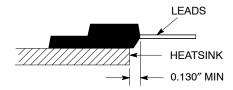


Figure 14. Mounting Position for Isolation Test

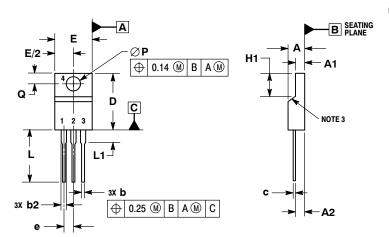
Measurement made between leads and heatsink with all leads shorted together.

\*For additional mounting information, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

#### PACKAGE DIMENSIONS

#### TO-220 FULLPACK, 3-LEAD

CASE 221AH-01 **ISSUE O** 



- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. CONTROLLING DIMENSION: MILLIMETERS.
  3. CONTOUR UNCONTROLLED IN THIS AREA.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH AND GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.13 PER SIDE. THESE DIMENSIONS ARE TO BE MEASURED AT OUTERMOST EXTREME OF THE PLASTIC BODY.

  5. DIMENSION b2 DOES NOT INCLUDE DAMBAR
- PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 2.00

	MILLIMETERS			
DIM	MIN	MAX		
Α	4.30	4.70		
A1	2.50	2.90		
A2	2.50	2.70		
b	0.54	0.84		
b2	1.10	1.40		
С	0.49	0.79		
D	14.22	15.88		
E	9.65	10.67		
е	2.54 BSC			
H1	5.97	6.48		
L	12.70	14.73		
L1		2.80		
P	3.00	3.40		
Q	2.80	3.20		

ON Semiconductor and 📖 are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### **PUBLICATION ORDERING INFORMATION**

#### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada

Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free

Europe, Middle East and Africa Technical Support: Phone: 421 33 790 2910 Japan Customer Focus Center

Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

NDF10N60ZH/D