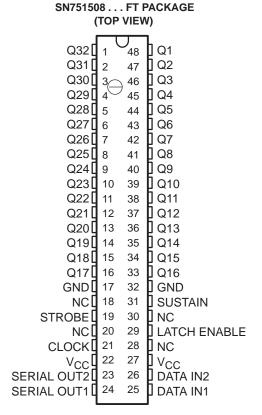
- Each Device Drives 32 Lines
- –120-V PNP Open-Collector Parallel Outputs
- High-Speed Serially Shifted Data Inputs
- CMOS-Compatible Inputs
- Strobe and Sustain Inputs Provided
- Serial Data Output for Cascade Operation

description

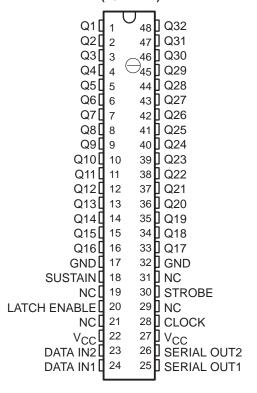
The SN751508 and SN751518 are monolithic integrated circuits designed to drive the data lines of a dc plasma panel display. The SN751518 pin sequence is reversed from the SN751508 for ease in printed-circuit-board layout.

Each device consists of two 16-bit shift registers. 32 latches, 32 OR gates, and 32 pnp opencollector output AND gates. Typically, a 32-bit data string is split into two 16-bit data strings externally and then entered in parallel into the shift registers on the high-to-low transition of the clock signal. A high LATCH ENABLE transfers the data from the shift registers to the inputs of 32 OR gates through the latches. Data present in the latch during the high-to-low transition of LATCH ENABLE is stored. When STROBE is high, the latch is masked and a high is placed on the data input of the output AND gates. When STROBE is low and SUSTAIN is high, data from the latches is reflected at the outputs. When low, SUSTAIN forces all outputs to their off state. Drivers can be cascaded via the serial data outputs of the static shift registers. These outputs are not affected by LATCH ENABLE, STROBE, or SUSTAIN.

The SN751508 and the SN751518 are characterized from 0°C to 70°C.



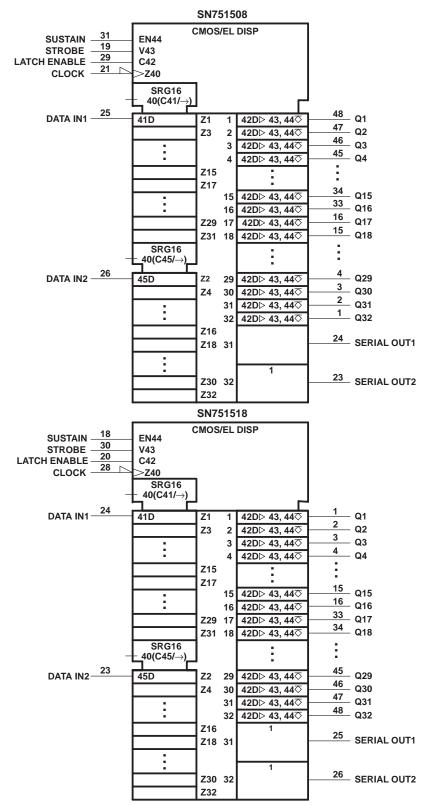
SN751518...FT PACKAGE (TOP VIEW)



NC - No internal connection

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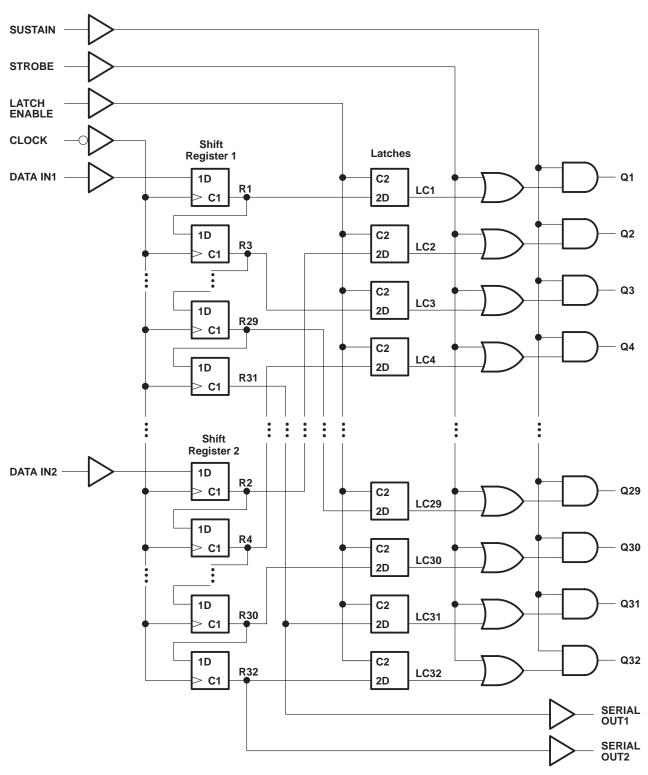
logic symbols†



[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



logic diagram (positive logic)





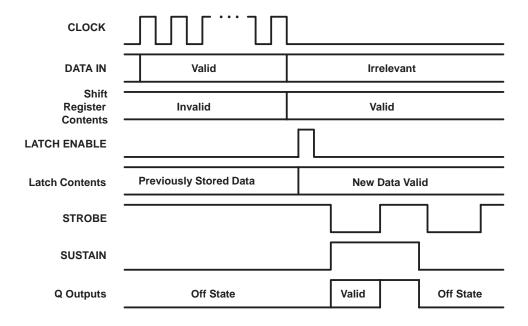
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FUNCTION TABLE

		CONTRO	L INPUTS			LATCHES			OUTPUTS	
FUNCTION	CLOCK	LATCH	STROBE	SUSTAIN	SHIFT REGISTERS R1 THRU R32	LC1 THRU	SER	IAL	Q1 THRU Q32	
	CLOCK	ENABLE	SIRUBE	SUSTAIN	KT TIIKO K32	LC32	S01	S02	QT INKU Q32	
Load	↓ No ↓	X X	X X	X X	Load and shift [†] No change	Determined by LATCH ENABLE‡	R31	R32	Determined by SUSTAIN and STROBE	
Latch Enable	X X	L H	X X	X X	As determined above	Stored data New data	R31	R32	Determined by SUSTAIN and STROBE	
Strobe	X X	X X	L H	H H	As determined above	Determined by LATCH ENABLE‡	R31	R32	LC1 thru LC32 All on (high)	
Sustain	х	Х	Х	L	As determined above	Determined by LATCH ENABLE‡	R31	R32	All off	

H = high level, L = low level, X = irrelevant, \downarrow = high-to-low transition

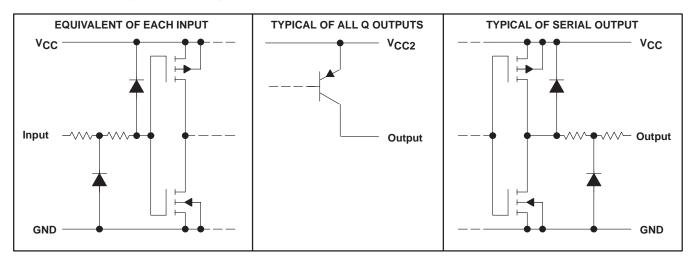
typical operating sequence



[†] Each even-numbered shift register stage takes on the state of the next-lower even-numbered stage, and likewise each odd-numbered shift register stage takes on the state of the next-lower odd-numbered stage; i.e., R32 takes on the state of R30, R30 takes on the state of R28, ... R4 takes on the state of R2, R2 takes on the state of DATA IN2, R31 takes on the state of R29, R29 takes on the state of R27, ... R3 takes on the state of R1, and R1 takes on the state on DATA IN1.

[‡] New data enters the latches while LATCH ENABLE is high. This data is stored while LATCH ENABLE is low.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V _{CC} (see Note 1)
On-state Q output voltage range, V _O
Input voltage range, V_1 -0.4 V to V_{CC} + 0.4 V
Serial output voltage range
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) 1025 mW
Operating free-air temperature range, T _A 0°C to 70°C
Storage temperature range65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds

NOTES: 1. Voltages values are with respect to GND.

2. For operation above 25°C free-air temperature, derate linearly to 656 mW at 70°C at the rate of 8.2 mW/°C.



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recommended operating conditions

		MIN	NOM	MAX	UNIT	
Supply voltage, V _{CC}		4.5	5	5.5	V	
Output voltage, VO				-75	V	
High-level input voltage, V_{IH} $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 5.5 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ Low-level input voltage, V_{IL}	V _{CC} = 4.5 V	3.6			V	
	V _{CC} = 5.5 V	4.4			V	
Laure laure l'amort au décourse V	V _{CC} = 4.5 V			0.9	V	
Low-level input voltage, VIL	/ _{CC} = 5.5 V			1	·	
Output current, IO (TA = 25°C)				-1.2	mA	
Clock frequency, f _{clock}			5	MHz		
	CLOCK	75			ns	
	DATA IN	160				
Pulse duration, t _W (see Figure 1)	LATCH ENABLE	90	90			
	STROBE					
	SUSTAIN	2	2		μs	
	DATA IN before CLOCK↓	20				
	CLOCK low before LATCH ENABLE↑ LATCH ENABLE low before CLOCK↓					
Setup time, t _{SU} (see Figure 1)					ns	
	LATCH ENABLE high before STROBE↓					
	LATCH ENABLE high before SUSTAIN↑	0				
Hold time, DATA IN after CLOCK↓, th (see Figure 1)					μs	
Operating free-air temperature, TA		0		70	°C	

electrical characteristics over operating free-air temperature range, V_{CC} = 5 V (unless otherwise noted)

PARAMETER			TEST CON	DITIONS	MIN	TYP [†]	MAX	UNIT
		Q outputs	$I_{OH} = -0.5 \text{ mA}$		4	4.5		
			\\ - - - - - - - - -	$I_{OH} = -100 \mu A$	4.3	4.6		1 1
Vон	High-level output voltage	SERIAL OUT 1, 2	V _{CC} = 5.5 V	$I_{OH} = -20 \mu A$	4.4			V
		SERIAL OUT 1, 2	V00 - 4 5 V	$I_{OH} = -100 \mu A$	3.4	3.6		
			V _{CC} = 4.5 V	$I_{OH} = -20 \mu A$	3.6			
	V_{OL} Low-level output voltage SERIAL OUT 1, 2 $V_{CC} = 5.5 \text{ V}$ $V_{CC} = 4.5 \text{ V}$	I _{OL} = 100 μA		0.9	1.2			
		CEDIAL OUT 4.2	vCC = 5.5 v	I _{OL} = 20 μA			1.1	V
VOL		· I	V 4 E V	I _{OL} = 100 μA		0.9	1.1	
			VCC = 4.5 V	I _{OL} = 20 μA			0.9	
loh	High-level Q output current		T _A = 25°C,	VO = 3 V	-1.2			mA
lOL	Low-level Q output current		T _A = 25°C,	$V_0 = -75 \text{ V}$			-500	μΑ
lн	High-level input current		T _A = 25°C,	$\Lambda^{I} = \Lambda^{CC}$			1	μΑ
IլL	Low-level input current		T _A = 25°C,	V _I = 0			-1	μΑ
laa	La Cumply ourrent		All Q outputs high,	utputs high, V _{CC} = 5.5 V		17	25	A
ICC	Supply current		All Q outputs low				3	mA
Ci	Input capacitance						15	pF

[†] All typical values are at $T_A = 25$ °C.



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switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tpd	Propagation delay time, CLOCK to SERIAL OUT			100	150	ns
tDLH	Delay time, low-to-high-level Q output from SUSTAIN or STROBE			0.3‡	1	μs
tDHL	Delay time, high-to-low-level Q output from SUSTAIN or STROBE	R _L = 91 kΩ,		1‡	2.5	μs
^t TLH	Transition time, low-to-high-level Q output	See Figures 1 and 2		2	5	μs
^t THL	Transition time, high-to-low-level Q output			11	18	μs

[‡] Typical values for delay times are measured from SUSTAIN.

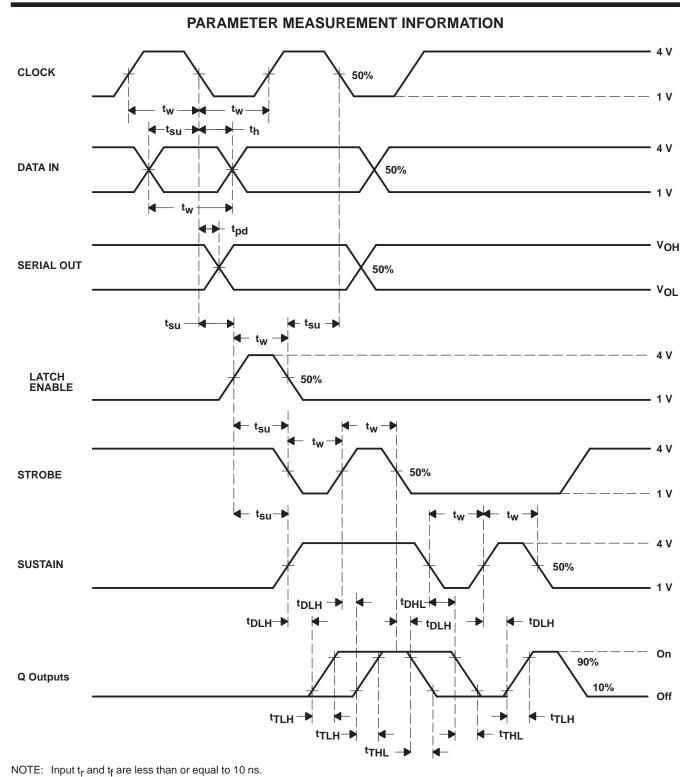
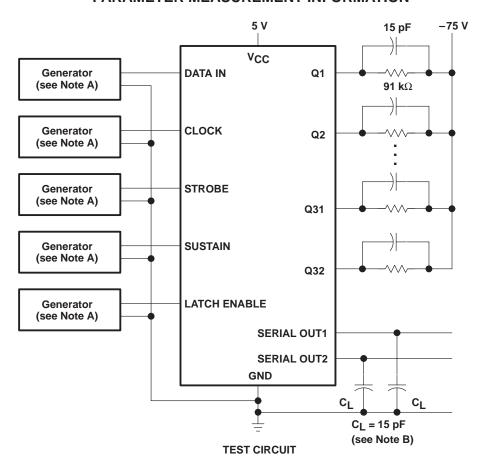


Figure 1. Input Timing and Switching Time Voltage Waveforms



PARAMETER MEASUREMENT INFORMATION

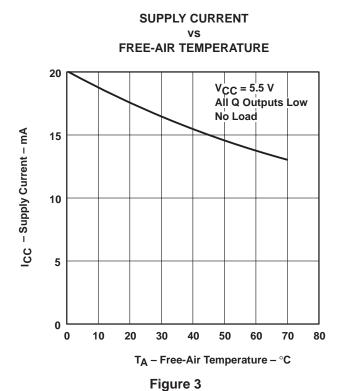


NOTES: A. Input pulses are supplied by generators having the following characteristics: t_W = 100 ns, PRR \leq 5 MHz, $t_\Gamma \leq$ 10 ns, $t_f \leq$ 10 ns, Z_O = 50 Ω .

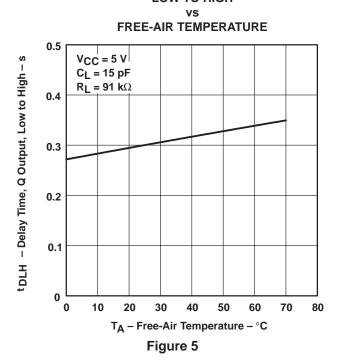
B. C_L includes probe and jig capacitance.

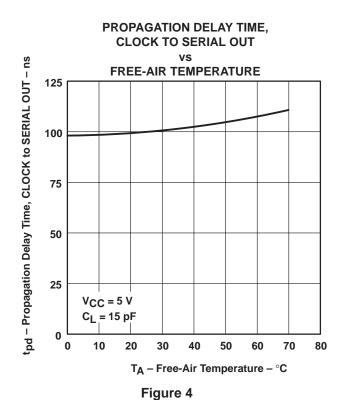
Figure 2. Test Circuit

TYPICAL CHARACTERISTICS



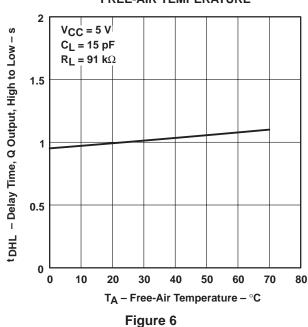






DELAY TIME, SUSTAIN INPUT TO Q OUTPUT HIGH TO LOW





TYPICAL CHARACTERISTICS

TRANSITION TIME, Q OUTPUT, **LOW TO HIGH** FREE-AIR TEMPERATURE tTLH – Transition Time, Q Output, Low to High – $\mu\,\text{s}$ 5 $V_{CC} = 5 V$ 4.5 C_L = 15 pF $R_L = 91 \text{ k}\Omega$ 4 3.5 3 2.5 2 1.5 1 0.5 0 0 10 20 30 40 50 60 70 80 T_A – Free-Air Temperature – $^{\circ}C$

Figure 7

TRANSITION TIME, Q OUTPUT, **HIGH TO LOW** FREE-AIR TEMPERATURE

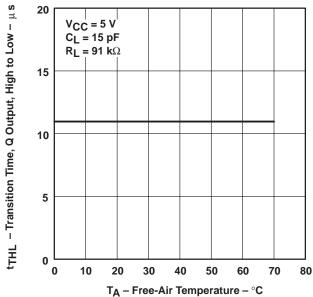


Figure 8

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	dataconverter.ti.com dsp.ti.com interface.ti.com logic.ti.com power.ti.com microcontroller.ti.com	amplifier.ti.com dataconverter.ti.com dsp.ti.com dsp.ti.com interface.ti.com logic.ti.com power.ti.com microcontroller.ti.com www.ti.com/lpw Audio Audio Audio Audio Automotive Broadband Digital Control Military Optical Networking Security Telephony Video & Imaging





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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN751508FT	OBSOLETE	DFP	FT	48	TBD	Call TI	Call TI
SN751518FT	OBSOLETE	DFP	FT	48	TBD	Call TI	Call TI
SN751518FT	OBSOLETE	DFP	FT	48	TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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