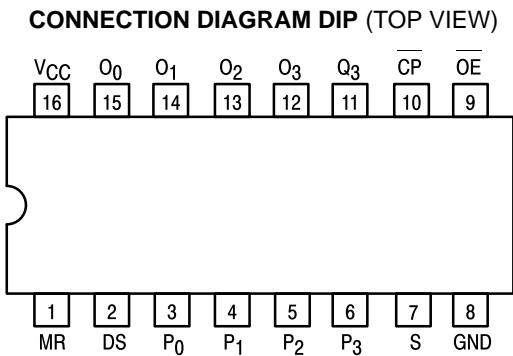




# 4-BIT SHIFT REGISTER WITH 3-STATE OUTPUTS

The SN74LS395 is a 4-Bit Register with 3-state outputs and can operate in either a synchronous parallel load or a serial shift-right mode, as determined by the Select input. An asynchronous active LOW Master Reset (MR) input overrides the synchronous operations and clears the register. An active HIGH Output Enable (OE) input controls the 3-state output buffers, but does not interfere with the other operations. The fourth stage also has a conventional output for linking purposes in multi-stage serial operations.

- Shift Left or Parallel 4-Bit Register
- 3-State Outputs
- Input Clamp Diodes Limit High-Speed Termination Effects



### PIN NAMES

$P_0-P_3$	Parallel Inputs
$D_S$	Serial Data Input
$S$	Mode Select Input
$\overline{CP}$	Clock (Active LOW) Input
$\overline{MR}$	Master Reset (Active LOW) Input
$OE$	Output Enable (Active HIGH) Input
$O_0-O_3$	3-State Register Outputs
$Q_3$	Register Output

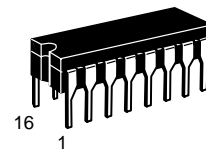
### NOTES:

a) 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.

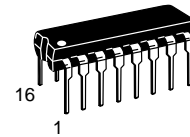
LOADING (Note a)	
HIGH	LOW
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
65 U.L.	15 U.L.
10 U.L.	5 U.L.

## SN74LS395

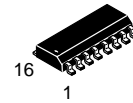
### 4-BIT SHIFT REGISTER WITH 3-STATE OUTPUTS LOW POWER SCHOTTKY



**J SUFFIX**  
CERAMIC  
CASE 620-09



**N SUFFIX**  
PLASTIC  
CASE 648-08

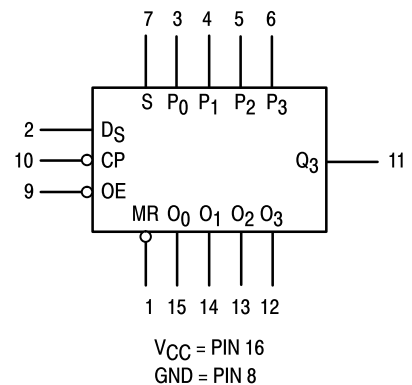


**D SUFFIX**  
SOIC  
CASE 751B-03

### ORDERING INFORMATION

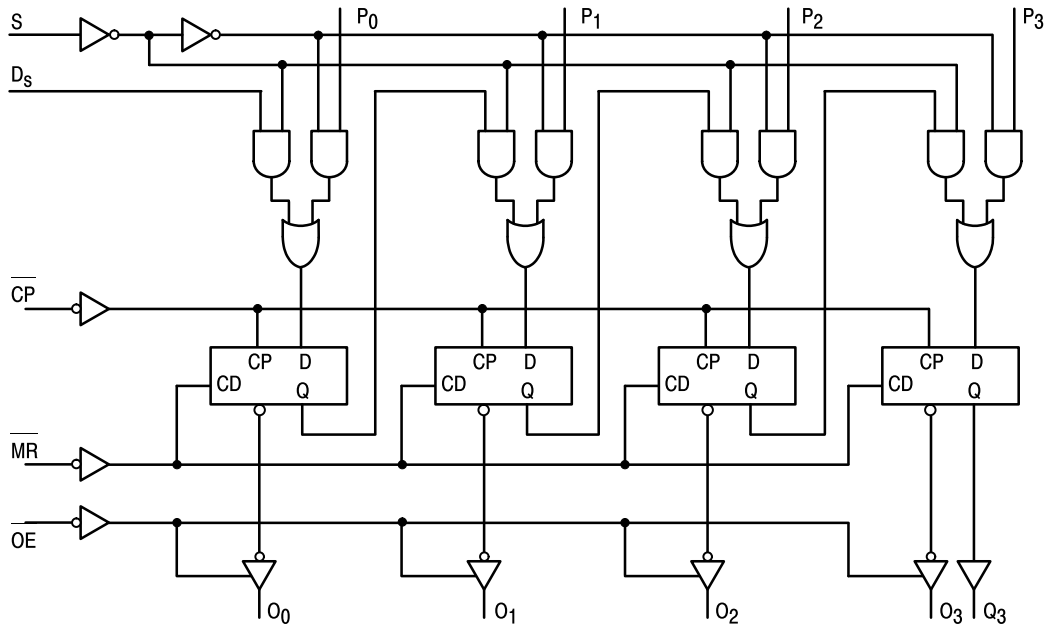
SN74LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

### LOGIC SYMBOL



# SN74LS395

## LOGIC DIAGRAM



## FUNCTION DESCRIPTION

The SN74LS395 contains four D-type edge-triggered flip-flops and auxiliary gating to select a D input either from a Parallel ( $P_n$ ) input or from the preceding stage. When the Select input is HIGH, the  $P_n$  inputs are enabled. A LOW signal on the S input enables the serial inputs for shift-right operations, as indicated in the Truth Table.

State changes are initiated by HIGH-to-LOW transitions on the Clock Pulse (CP) input. Signals on the  $P_n$ ,  $D_s$  and S inputs can change when the Clock is in either state, provided that the recommended set-up and hold times are observed. When the

S input is LOW, a CP HIGH-LOW transition transfers data in  $Q_0$  to  $Q_1$ ,  $Q_1$  to  $Q_2$ , and  $Q_2$  to  $Q_3$ . A left-shift is accomplished by connecting the outputs back to the  $P_n$  inputs, but offset one place to the left, i.e.,  $O_3$  to  $P_2$ ,  $O_2$  to  $P_1$  and  $O_1$  to  $P_0$ , with  $P_3$  acting as the linking input from another package.

When the OE input is HIGH, the output buffers are disabled and the  $Q_0$ – $Q_3$  outputs are in a high impedance condition. The shifting, parallel loading or resetting operations can still be accomplished, however.

## MODE SELECT — TRUTH TABLE

Operating Mode	Inputs @ $t_n$					Outputs @ $t_{n+1}$			
	MR	CP	S	$D_s$	$P_n$	$O_0$	$O_1$	$O_2$	$O_3$
Asynchronous Reset	L	X	X	X	X	L	L	L	L
Shift, SET First Stage	H		L	H	X	H	$O_{0n}$	$O_{1n}$	$O_{2n}$
Shift, RESET First Stage	H		L	L	X	L	$O_{0n}$	$O_{1n}$	$O_{2n}$
Parallel Load	H		H	X	$P_n$	$P_0$	$P_1$	$P_2$	$P_3$

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

$t_n, t_{n+1}$  = time before and after CP HIGH-to-LOW transition

NOTE:—

When OE is HIGH, outputs  $O_0$ – $O_3$  are in the high impedance state; however, this does not affect other operations or the  $Q_3$  output.

## GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CC}$	Supply Voltage	4.75	5.0	5.25	V
$T_A$	Operating Ambient Temperature Range	0	25	70	°C
$I_{OH}$	Output Current — High			–0.4	mA
$I_{OL}$	Output Current — Low			8.0	mA

FAST AND LS TTL DATA

5-552

# SN74LS395

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.7	3.5		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table
V <sub>OL</sub>	Output LOW Voltage		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA
			0.35	0.5	V	I <sub>OL</sub> = 8.0 mA
I <sub>OZH</sub>	Output Off Current HIGH			20	μA	V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.4 V
I <sub>OZL</sub>	Output Off Current LOW			-20	μA	V <sub>CC</sub> = MAX, V <sub>O</sub> = 0.4 V
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
				-0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current Total, Output HIGH			31	mA	V <sub>CC</sub> = MAX, OE = GND, CP = GND
	Total, Output LOW			34	mA	V <sub>CC</sub> = MAX, OE = 4.5 V, CP momentary 3.0 V then GND

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f <sub>MAX</sub>	Maximum Input Clock Frequency	30	45		MHz	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF
t <sub>PHL</sub>	Propagation Delay, Clear to Output		22	35	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay, Low to High Propagation Delay, High to Low		15 25	30 30	ns	
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time		15 17	25 25	ns	
t <sub>PLZ</sub> t <sub>PHZ</sub>	Output Disable Time		12 11	20 17	ns	C <sub>L</sub> = 5.0 pF

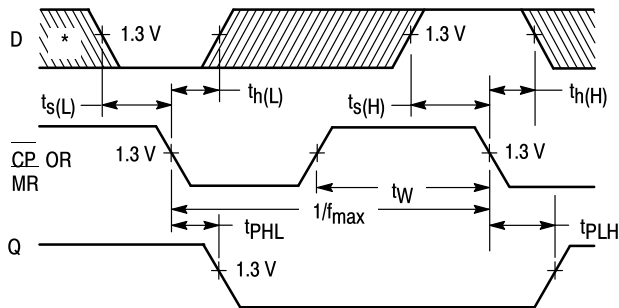
## AC SETUP REQUIREMENTS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>W</sub>	Clock Pulse Width	16			ns	V <sub>CC</sub> = 5.0 V
t <sub>s</sub>	Setup Time, Mode Select	40			ns	
t <sub>s</sub>	Setup Time, All Others	20			ns	
t <sub>h</sub>	Data Hold Time	10			ns	

# SN74LS395

## AC WAVEFORMS

The shaded areas indicate when the input is permitted to change for predictable output performance.



\*The Data Input is  $D_S$  for  $S = \text{LOW}$  and  $P_n$  for  $S = \text{HIGH}$ .

Figure 1

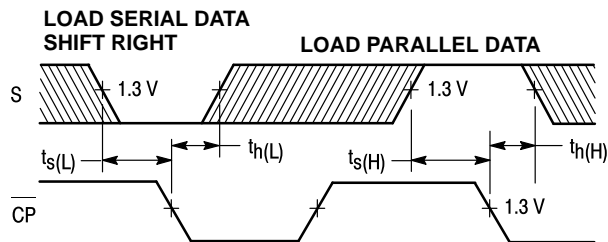


Figure 2

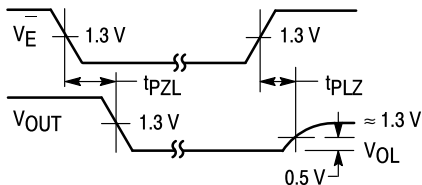


Figure 3

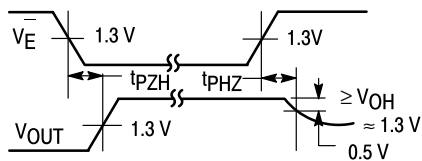
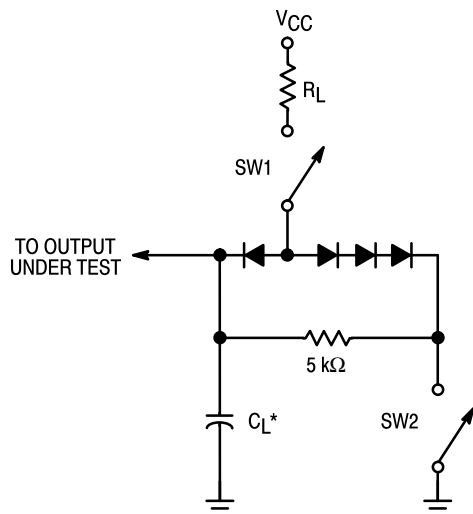


Figure 4

## AC LOAD CIRCUIT



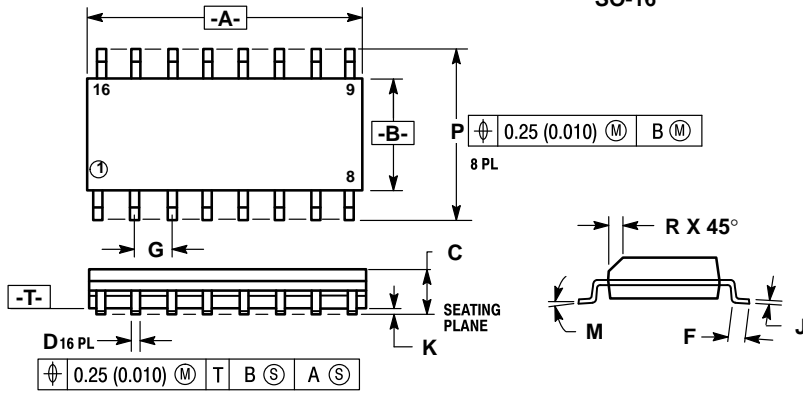
\* Includes Jig and Probe Capacitance.

Figure 5

### SWITCH POSITIONS

SYMBOL	SW1	SW2
$t_{PZH}$	Open	Closed
$t_{PZL}$	Closed	Open
$t_{PLZ}$	Closed	Closed
$t_{PHZ}$	Closed	Closed

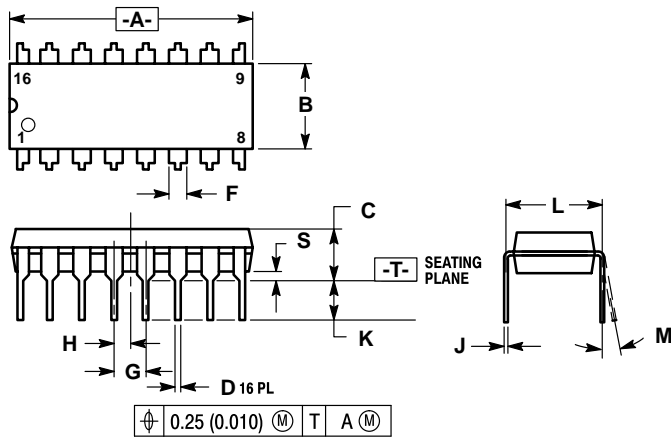
**Case 751B-03 D Suffix  
16-Pin Plastic  
SO-16**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. 751B-01 IS OBSOLETE, NEW STANDARD 751B-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

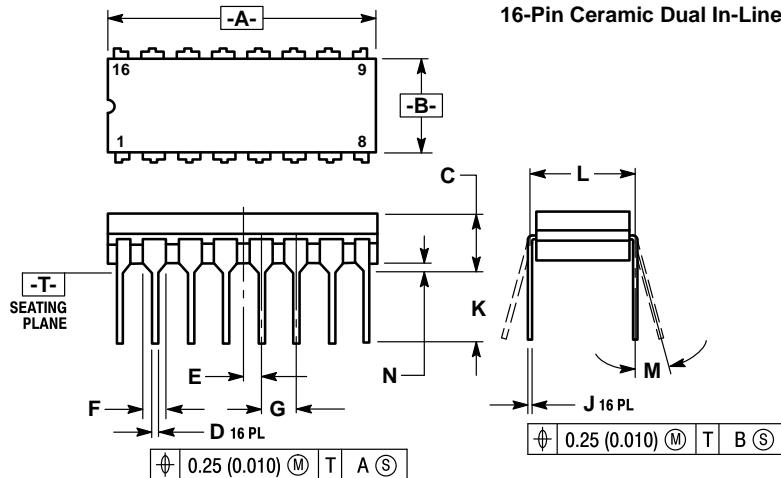
**Case 648-08 N Suffix  
16-Pin Plastic**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
  4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
  5. ROUNDED CORNERS OPTIONAL.
  6. 648-01 THRU -07 OBSOLETE, NEW STANDARD 648-08.


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

**Case 620-09 J Suffix  
16-Pin Ceramic Dual In-Line**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
  5. 620-01 THRU -08 OBSOLETE, NEW STANDARD 620-09.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.55	0.750	0.770
B	6.10	7.36	0.240	0.290
C	—	4.19	—	0.165
D	0.39	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
J	0.23	0.27	0.009	0.011
K	—	5.08	—	0.200
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.39	0.88	0.015	0.035

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