

CCD area image sensor



S10810

Front-illuminated FFT-CCDs for X-ray imaging

The S10810 is an FFT-CCD image sensor suitable for intra-oral X-ray imaging in dental diagnosis. The S10810 has 1.5 mega (1500 × 1000) pixels, each of which is 20 × 20 μm in size. The FOP (fiber optic plate) used as an input window is as thin as 1.5 mm, making high resolution as well as highly resistant to X-ray irradiation. The scintillator coated on the FOP is optimized to have high X-ray sensitivity and high resolution (20 Lp/mm).

The S10810 is an easy-to-use X-ray imaging module, with added functions such as a cable assembly and X-ray trigger circuit. The S10810 is pin-compatible with the S8981-02C and also S10811 (1700 × 1200 pixels).

Features

- X-ray monitoring photodiode incorporated
- Compact size
- High dynamic range: 12-bit
- Long-term stability
For use under 100000 shots
(60 kVp, 30 mR X-ray irradiation)
- Resolution: 20 Lp/mm
- 1500 (H) × 1000 (V) pixel format
- Pixel size: 20 × 20 μm
- Coupled with FOS for X-ray imaging
- 100 % fill factor
- Low dark signal
- Low readout noise
- MPP operation
- AC/DC X-ray source adapted

Applications

- Intra-oral X-ray imaging in dental diagnosis
- General X-ray imaging
- Non-destructive inspection

General ratings

Parameter	Specification
CCD structure	Full frame transfer
Fill factor	100 %
Cooling	Non-cooled
Number of pixels	1508 (H) × 1002 (V)
Number of active pixels	1500 (H) × 1000 (V)
Pixel size	20 (H) × 20 (V) μm
Active area	30 (H) × 20 (V) mm
Vertical clock phase	2 phases
Horizontal clock phase	2 phases
Output circuit	Emitter follower without load resistance
Dimensions	41.0 (H) × 26.4 (V) mm
Reliability	100000 shots at 60 kVp, 30 mR
Window	Scintillator on 1.5 mm FOP

▣ Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Storage temperature	Tstg	-20	-	+70	°C
Operating temperature	Topr	0	-	+40	°C
OD voltage	VOD	-0.5	-	+20	V
RD voltage	VRD	-0.5	-	+18	V
SG voltage	VSG	-15	-	+15	V
OG voltage	VOG	-15	-	+15	V
RG voltage	VRG	-15	-	+15	V
TG voltage	VTG	-15	-	+15	V
Vertical clock voltage	VP1V, VP2V	-15	-	+15	V
Horizontal clock voltage	VP1H, VP2H	-15	-	+15	V
Vcc voltage	Vcc	0	-	+7	V

▣ Operating conditions (MPP mode, Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Output transistor drain voltage	VOD	12	15	-	V	
Reset drain voltage	VRD	12	13	14	V	
Output gate voltage	VOG	-0.5	2	5	V	
Substrate voltage	Vss	-	0	-	V	
Vertical shift register clock voltage	High	VP1VH, VP2VH	0	3	6	V
	Low	VP1VL, VP2VL	-9	-8	-7	V
Horizontal shift register clock voltage	High	VP1HH, VP2HH	0	3	6	V
	Low	VP1HL, VP2HL	-9	-8	-7	V
Summing gate voltage	High	VSGH	0	3	6	V
	Low	VSGL	-9	-8	-7	V
Reset gate voltage	High	VRGH	0	3	6	V
	Low	VRGL	-9	-8	-7	V
Transfer gate voltage	High	VTGH	0	3	6	V
	Low	VTGL	-9	-8	-7	V
+5 V power supply voltage	Vcc	4.75	5	5.25	V	

▣ Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Signal output frequency	fc	-	1	-	MHz
Vertical shift register capacitance	CP1V, CP2V	-	60000	-	pF
Horizontal shift register capacitance	CP1H, CP2H	-	550	-	pF
Summing gate capacitance	Csg	-	220	-	pF
Reset gate capacitance	CRG	-	220	-	pF
Transfer gate capacitance	CTG	-	450	-	pF
Charge transfer efficiency *1	CTE	0.99995	0.99998	-	-
DC output level *2	Vout	5	8	11	V
Output impedance *2	Zo	-	500	-	Ω
Power dissipation *2 *3	P	-	75	-	mW
+5 V power supply current	Icc	-	2	-	mA

*1: Measured at half of the full well capacity. CTE is defined per pixel.

*2: VOD=15 V

*3: Power dissipation of the on-chip amplifier

Electrical and optical characteristics (Ta=25 °C, VOD=15 V, unless otherwise noted)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Full well capacity	Vertical	Fw	100	200	-	ke ⁻
	Horizontal		-	300	-	
	Summing		-	600	-	
CCD node sensitivity *4		Sv	1.0	1.4	-	μV/e ⁻
Dark current (MPP mode) *5		DS	-	250	2500	e ⁻ /pixel/s
Readout noise *6		Nr	-	60	-	e ⁻ rms
Dynamic range *7		DR	-	3333	-	-
X-ray response non-uniformity *8 *9		XRNU	-	±10	±30	%
Blemish *10	Point defects *11	White spots	-	-	20	-
		Black spots	-	-	20	
	Cluster defects *12		-	-	3	
	Column defects *13		-	-	1	
X-ray resolution *8		ΔR	15	20	-	Lp/mm

*4: VOD=15 V, RL (load resistance of emitter follower)=1 kΩ

*5: Dark signal doubles for every 5 to 7 °C.

*6: -40 °C, operating frequency is 1 MHz.

*7: Dynamic range = Full well capacity / Readout noise

*8: X-ray irradiation of 60 kVp, measured at half of the full well capacity

*9: XRNU (%) = Noise / Signal × 100

Noise: Fixed pattern noise (peak to peak)

In the range that excludes 5 pixels from edges to the center at every position

*10: Refer to "Characteristics and use of FFT-CCD area image sensor" of technical information.

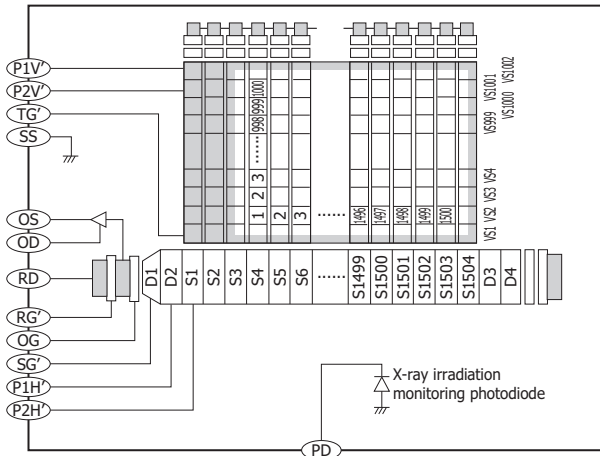
*11: White spots > 10 times of Max. Dark signal (2500 e⁻/pixel/s)

Black spots > 50 % reduction in response relative to adjacent pixels, measured at half of the full well capacity

*12: Continuous 2 to 9 point defects

*13: Continuous > 10 point defects

Device structure



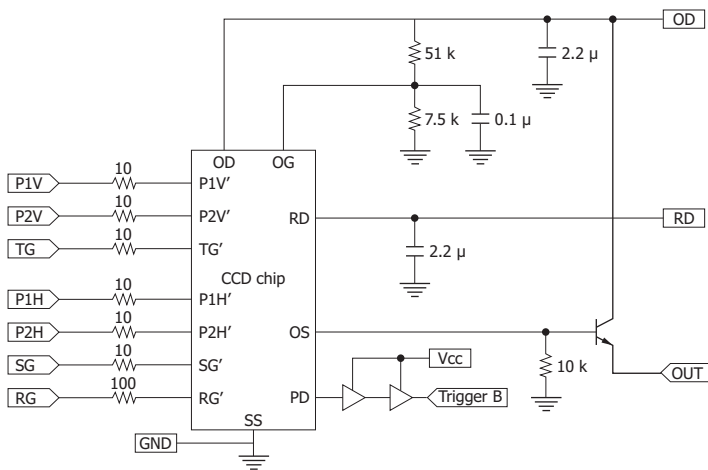
KMPDC0163EA

Pixel format

Left ← Horizontal direction → Right						
Blank	Optical black	Isolation	Effective	Isolation	Optical black	Blank
2	2	1	1500	1	0	2

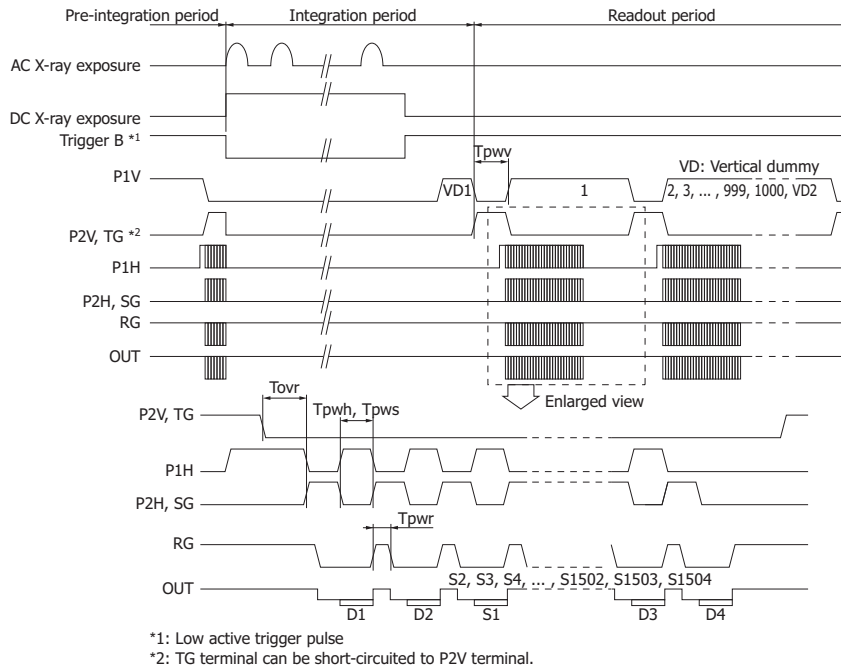
Top ← Vertical direction → Bottom		
Isolation	Effective	Isolation
1	1000	1

On-board circuit



KMPDC0314EA

Timing chart



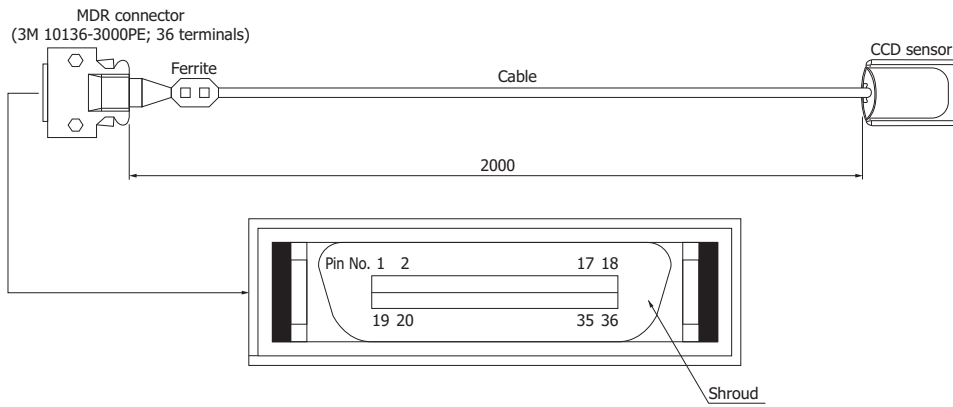
KMPDC0315EA

Parameter		Symbol	Min.	Typ.	Max.	Unit
P1V, P2V, TG	Pulse width *14	tpwv	30	60	-	μs
	Rise and fall times	tprv, tpfv	200	-	-	ns
P1H, P2H	Pulse width	tpwh	100	500	-	ns
	Rise and fall times *14	tprh, tpfh	5	-	-	ns
	Duty ratio	-	-	50	-	%
SG	Pulse width	tpws	100	500	-	ns
	Rise and fall times	tprs, tpfs	3	-	-	ns
	Duty ratio	-	-	50	-	%
RG	Pulse width	tpwr	10	50	-	ns
	Rise and fall times	tpr, tprf	3	-	-	ns
TG-P1H	Overlap time	tovr	18	36	-	μs

*14: The clock pulses should be overlapped at 50 % of maximum amplitude.

Dimensional outlines (unit: mm)

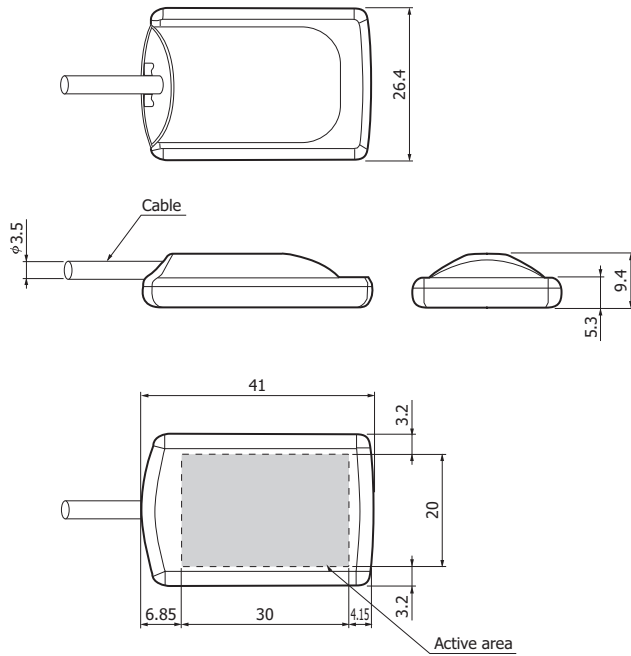
Entire view



KMPDA024EA

* The shield of cable and the shroud of MDR connector are short-circuited.
Take due care of EMC and ESD when connected to 0 V reference and the ground.

CCD sensor



KMPDA0245EA

Pin connections

Pin No.	Symbol	Description	Remark
1	GND	Ground	
2	Vcc	+5 V power supply	
3	SG	Summing gate	Same timing as P2H
4	Trigger B	Trigger B output	
5	RG	Reset gate	
6	NC		
7	Reserve		Should be opened
8	NC		
9	RD	Reset drain	
10	NC		
11	OD	Output transistor drain	
12	NC		
13	OUT	Sensor output	
14	NC		
15	GND	Ground	
16	NC		
17	P1V	CCD vertical register clock-1	
18	Reserve		Should be opened
19	Reserve		Should be opened
20	P2H	CCD horizontal register clock-2	
21	NC		
22	P1H	CCD horizontal register clock-1	
23	NC		
24	GND	Ground	
25	NC		
26	RD	Reset drain	
27	NC		
28	OD	Output transistor drain	
29	NC		
30	GND	Ground	
31	NC		
32	OUT	Sensor output	
33	NC		
34	P2V	CCD vertical register clock-2	
35	NC		
36	TG	Transfer gate	Same timing as P2V

Precautions for use (electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

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