Document Title

256M: 8M x 32 Mobile DDR SDRAM

Revision History

Revision No.	Date	History
0.0	Dec. 11, 2007	Initial Draft

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256M : 8M x 32bit Mobile DDR SDRAM

FEATURES

- 1.8V power supply, 1.8V I/O power
- LVCMOS compatible with multiplexed address.
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe(DQS)
- Four banks operation.
- MRS cycle with address key programs.
  - CAS latency (2, & 3).
  - Burst length (2, 4, 8, & 16).
  - Burst type (Sequential & Interleave).
- Differential clock inputs(CK and CKB).
- EMRS cycle with address key programs.
  - PASR(Partial Array Self Refresh).
  - DS (Driver Strength)
- Internal auto TCSR
  (Temperature Compensated Self Refresh)
- Deep power-down(DPD) mode.
- DM for write masking only.
- Auto refresh and self refresh modes.
- 64㎳ refresh period (4K cycle).
- Operating temperature range (-25℃ ~ 85℃).

GENERAL DESCRIPTION

This EMD56324P is 268,435,456 bits synchronous double data rate Dynamic RAM. Each 67,108,854 bits bank is organized as 4,096 rows by 512columns by 32 bits, fabricated with EMLSI's high performance CMOS technology.

This device uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2n-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O balls.

Range of operating frequencies, programmable burst lengths and programmable latencies allow the same device to be useful for a variety of high bandwidth and high performance memory system applications.

Table 1: ORDERING INFORMATION

Part No.	Max Freq.	Interface	Package	Remark
EMD56324P-60(DDR332)	166㎒(CL3), 83㎒(CL2)	LVCMOS	Wafer Biz.	
EMD56324P-75(DDR266)	133㎒(CL3), 83㎒(CL2)			

NOTE :

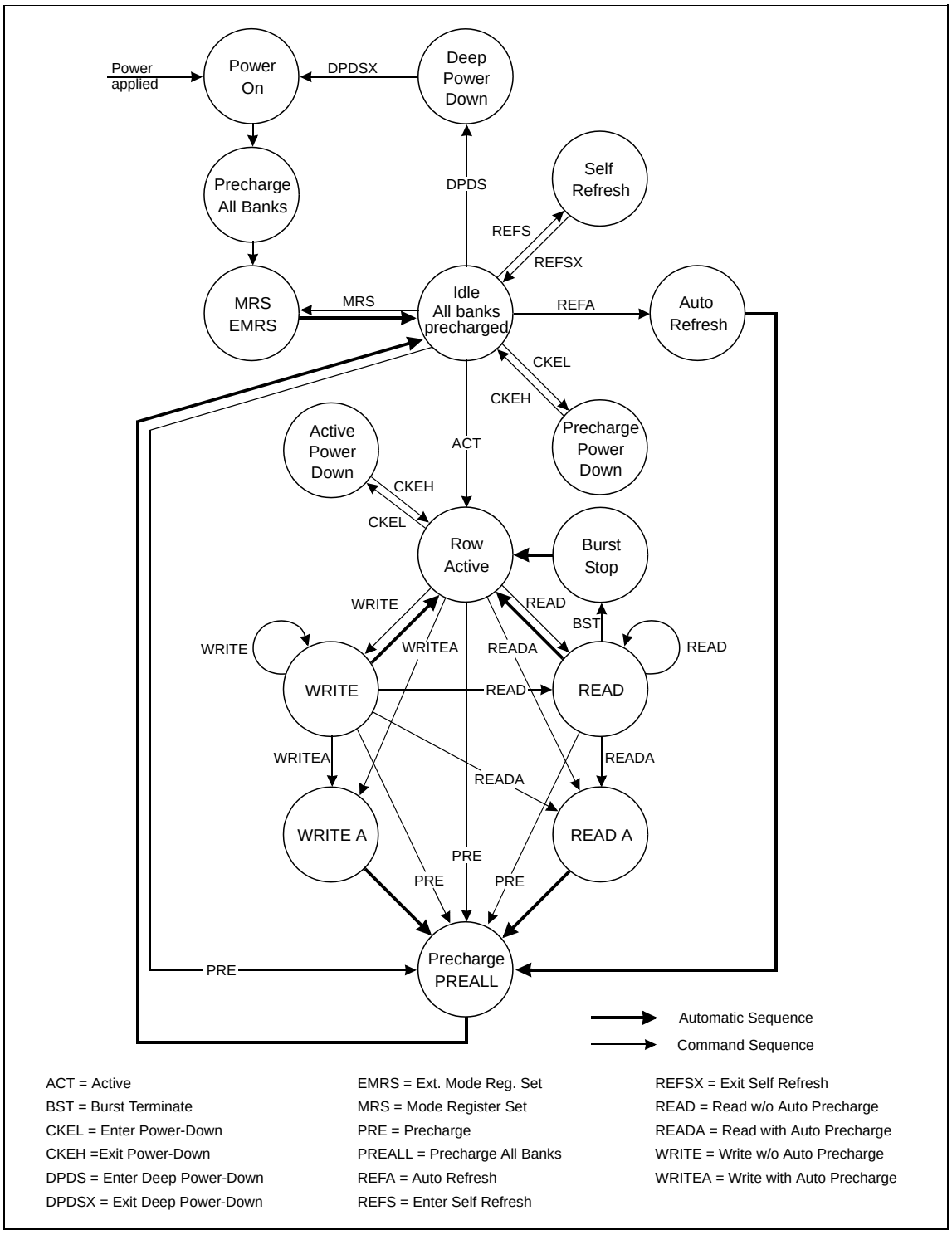
1. EMLSI is not designed or manufactured for use in a device or system that is used under circumstance in which human life is potentially at stake. Please contact to the memory marketing team in EMLSI when considering the use of a product contained herein for any specific purpose, such as medical, aerospace, nuclear, military, vehicular or undersea repeater use.

Table 2: Pad Description

Symbol	Type	Descriptions
CK, CKB	Input	Clock : CK and CKB are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CKB. Input and output data is referenced to the crossing of CK and CKB(both directions of crossing). Internal clock signals are derived from CK/CKB.
CKE	Input	Clock Enable : CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation(all banks idle), or ACTIVE POWER-DOWN(row ACTIVE in any bank). CKE is synchronous for all functions except for SELF REFRESH EXIT, which is achieved asynchronously. Input buffers, excluding CK, CKB and CKE, are disabled during power-down and self refresh mode which are contrived for low standby power consumption.
CSB	Input	Chip Select : CSB enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CSB is registered HIGH. CSB provides for external bank selection on systems with multiple banks. CSB is considered part of the command code.
RASB, CASB, WEB	Input	Command Inputs: CASB, RASB, and WEB(along with CSB) define the command being entered.
DM0~DM3	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled. HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Data Mask pins include dummy loading internally, to match the DQ and DQS loading.
BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
A0 ~ A11	Input	Address Inputs: provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ / WRITE commands, to select one location out of the memory array in the respective bank. The address inputs also provide the op-code during a MODE REGISTER SET command.
DQ0~DQ31	I/O	Data Bus: Input / Output
DQS0~DQS3	I/O	Data Strobe: Output with read data, input with write data. Edge-aligned with read data, center-aligned with write data. Used to capture write data. For x32 device, DQS0 corresponds to the data on DQ0-DQ7, DQS1 corresponds to the data on DQ8-DQ15, DQS2 corresponds to the data on DQ16-DQ23, and DQS3 corresponds to the data on DQ24-DQ31.
VDD	Supply	Power Supply

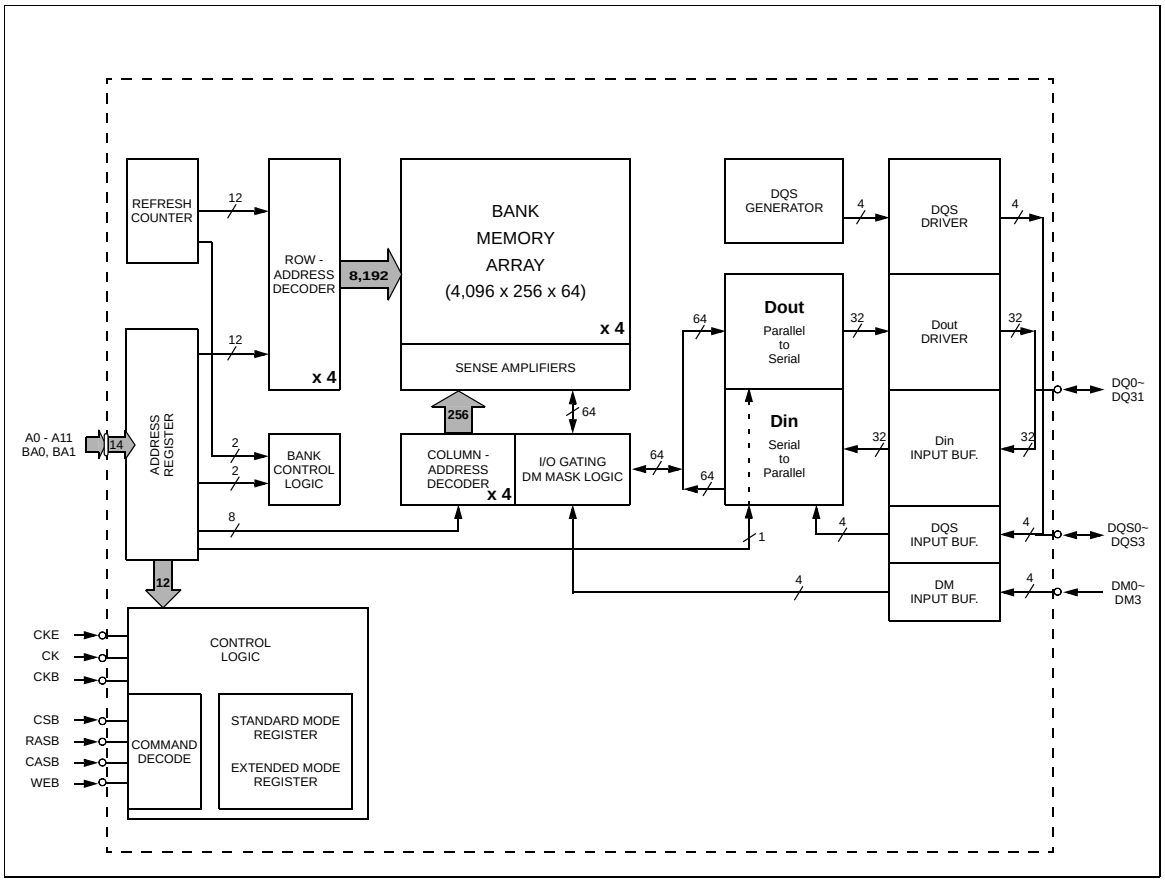
Device Operation

Simplified State Diagram



ACT = Active
BST = Burst Terminate
CKEL = Enter Power-Down
CKEH =Exit Power-Down
DPDS = Enter Deep Power-Down
DPDSX = Exit Deep Power-Down
EMRS = Ext. Mode Reg. Set
MRS = Mode Register Set
PRE = Precharge
PREALL = Precharge All Banks
REFA = Auto Refresh
REFS = Enter Self Refresh
REFSX = Exit Self Refresh
READ = Read w/o Auto Precharge
READA = Read with Auto Precharge
WRITE = Write w/o Auto Precharge
WRITEA = Write with Auto Precharge

FUNCTIONAL BLOCK DIAGRAM



Electrical Specifications

Table 3: ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-0.5 ~ 2.5	V
Voltage on V_{DD} and V_{DDQ} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-0.5 ~ 2.5	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	1.0	W
Short circuit current	I_{OS}	50	㎃

NOTE :
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

Table 4: DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = -25°C~ 85°C for Extended)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	1.7	1.8	1.95	V	1
	V_{DDQ}	1.7	1.8	1.95	V	1
Input logic high voltage	V_{IH}	0.8 x V_{DDQ}	1.8	V_{DDQ} + 0.3	V	2
Input logic low voltage	V_{IL}	-0.3	0	0.3	V	2
Output logic high voltage	V_{OH}	0.9 x V_{DDQ}	-	-	V	I_{OH} = -0.1㎃
Output logic low voltage	V_{OL}	-	-	0.1 x V_{DDQ}	V	I_{OL} = 0.1㎃
Input leakage current	I_{LI}	-2	-	2	㎂	
Output leakage current	I_{LO}	-5	-	5	㎂	

NOTE :
1. Under all conditions, VDDQ must be less than or equal to VDD.
2. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation.

Table 5: CAPACITANCE (V_{DD} = 1.8V, V_{DDQ} = 1.8V, T_A = 25℃, f=1㎒)

Pin	Symbol	Min	Max	Unit	Note
Input capacitance (ADD, BA0~1, RASB, CASB, WEB, CSB, CKE)	C_{IN1}	1.5	3.0	㎊	
Input capacitance(CK, CKB)	C_{IN2}	1.5	3.5	㎊	
Data & DQS input/output capacitance	C_{out}	2.0	4.5	㎊	
Input capacitance(DM)	C_{IN3}	2.0	4.5	㎊	

Table 6: DC CHARACTERISTICS

Recommended operating conditions (Voltage referenced to VSS = 0V, T_A = -25℃ to 85℃)

Parameter	Symbol	Test Condition		Version		Unit
				-60	-75	
Operating one bank active-precharge current	I_{DD0}	t_{RC} = t_{RCmin}; t_{CK} = t_{CKmin}; CKE is HIGH; CSB is HIGH between valid commands; address inputs are SWITCHING; data bus inputs are STABLE		100	80	mA
Precharge power-down standby current	I_{DD2P}	all banks idle, CKE is LOW; CSB is HIGH, t_{CK} = t_{CKmin}; address and control inputs are SWITCHING; data bus inputs are STABLE		0.4		mA
Precharge power-down standby current with clock stop	I_{DD2PS}	all banks idle, CKE is LOW; CSB is HIGH, CK = LOW, CKB = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE		0.4		
Precharge non power-down standby current	I_{DD2N}	all banks idle, CKE is HIGH; CSB is HIGH, t_{CK} = t_{CKmin}; address and control inputs are SWITCHING; data bus inputs are STABLE		25	20	mA
Precharge non power-down standby current with clock stop	I_{DD2NS}	all banks idle, CKE is HIGH; CSB is HIGH, CK = LOW, CKB = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE		5	5	
Active power-down standby current	I_{DD3P}	one bank active, CKE is LOW; CSB is HIGH, t_{CK} = t_{CKmin}; address and control inputs are SWITCHING; data bus inputs are STABLE		8		mA
Active power-down standby current with clock stop	I_{DD3PS}	one bank active, CKE is LOW; CSB is HIGH, CK = LOW, CKB = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE		5		
Active non power-down standby current	I_{DD3N}	one bank active, CKE is HIGH; CSB is HIGH, t_{CK} = t_{CKmin}; address and control inputs are SWITCHING; data bus inputs are STABLE		25	25	mA
Active non power-down standby current with clock stop	I_{DD3NS}	one bank active, CKE is HIGH; CSB is HIGH, CK = LOW, CKB = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE		10	10	mA
Operating burst read current	I_{DD4R}	one bank active; BL=4; CL=3; t_{CK} = t_{CKmin}; continuous read bursts; Iout = 0 mA; address inputs are SWITCHING; 50% data change each burst transfer		160	130	mA
Operating burst write current	I_{DD4W}	one bank active; t_{CK} = t_{CKmin}; continuous write bursts; address inputs are SWITCHING; 50% data change each burst transfer		130	105	mA
Auto-Refresh current	I_{DD5}	t_{RC} = t_{RFCmin}; burst refresh; CKE is HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE		120	120	mA
Self Refresh Current	I_{DD6}	CKE is LOW, CK = LOW, CKB = HIGH; Extended Mode Register set to all 0s; address and control inputs are STABLE; data bus inputs are STABLE	**TCSR Range**	**45*[1]**	**85**	°C
			Full Array	250	400	µA
			1/2 of Full Array	200	300	
			1/4 of Full Array	150	250	
Deep Power-Down Current	I_{DD8}	Address and Control inputs are STABLE; data bus inputs are STABLE		10	10	µA

NOTE :
1. IDD specifications are tested after the device is properly initialized
2. Input slew rate is 1V/ns.
3. Definitions for IDD:
   LOW is defined as $V_{IN} \leq 0.1 * VDDQ$;
   HIGH is defined as $V_{IN} \geq 0.9 * VDDQ$;
   STABLE is defined as inputs stable at a HIGH or LOW level ;
   SWITCHING is defined as :
   - address and command : inputs changing between HIGH and LOW once per two clock cycles ;
   - data bus inputs : DQ changing between HIGH and LOW once per clock cycle ; DM and DQS are STABLE

Table 7: AC OPERATING TEST CONDITIONS

(V_{DD} = 1.7V ~ 1.95V, T_A = -25℃ ~85℃ for Extended)

Parameter	Value	Unit	Note
AC input levels(Vih/Vil)	0.8 × V_{DDQ} / 0.2 × V_{DDQ}	V	
Input timing measurement reference level	0.5 × V_{DDQ}	V	
Input rise and fall time	1.0	V/ns	
Output timing measurement reference level	0.5 × V_{DDQ}	V	
Vix	0.4 × V_{DDQ}(Min) / 0.6 × V_{DDQ}(Max)	V	3
Output load condition	See Figure 2		

NOTE :
1. Under all conditions, VDDQ must be less than or equal to VDD.
2. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation.
3. CK and CKB crossing voltage.

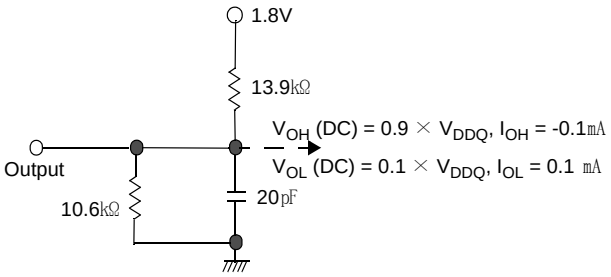


Figure 1. DC Output Load Circuit

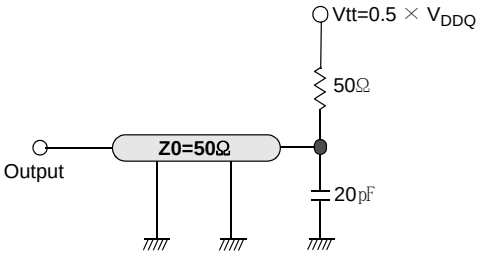


Figure 2. AC Output Load Circuit

Table 8: OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Sym-bol	-60		-75		Unit	Note
			Min	Max	Min	Max		
DQ output access time from CK/CKB		t_{AC}	2	5	2.5	6.0	ns	3
DQS output access time from CK/CKB		t_{DQSCK}	2	5	2.5	6.0	ns	
Clock high-level width		t_{CH}	0.45	0.55	0.45	0.55	t_{CK}	
Clock low-level width		t_{CL}	0.45	0.55	0.45	0.55	t_{CK}	
Clock half period		t_{HP}	min (t_{CL},t_{CH})		min (t_{CL},t_{CH})		ns	
Clock cycle time	CL = 3	t_{CK}	6	100	7.5	100	ns	
	CL = 2		12	100	12	100	ns	
DQ and DM input setup time		t_{DS}	0.6		0.75		ns	4,5
DQ and DM input hold time		t_{DH}	0.6		0.75		ns	4,5
DQ and DM input pulse width		t_{DIPW}	1.8		2.5		ns	
Address and control input setup time		t_{IS}	1.1		1.3		ns	1
Address and control input hold time		t_{IH}	1.1		1.3		ns	1
Address and control input pulse width		t_{IPW}	2.6		2.6		ns	
DQ & DQS low-impedance time from CK/CKB		t_{LZ}	1.0		1.0		ns	
DQ & DQS high-impedance time from CK/CKB		t_{HZ}		5		6.0	ns	
DQS - DQ skew		t_{DQSQ}		0.5		0.6	ns	
DQ / DQS output hold time from DQS		t_{QH}	t_{HP}-t_{QHS}		t_{HP}-t_{QHS}		ns	
Data hold skew factor		t_{QHS}		0.65		0.75	ns	
Write command to 1st DQS latching transition		t_{DQSS}	0.75	1.25	0.75	1.25	t_{CK}	
DQS input high-level width		t_{DQSH}	0.4	0.6	0.4	0.6	t_{CK}	
DQS input low-level width		t_{DQSL}	0.4	0.6	0.4	0.6	t_{CK}	
DQS falling edge to CK rising - setup time		t_{DSS}	0.2		0.2		t_{CK}	
DQS falling edge from CK rising - hold time		t_{DSH}	0.2		0.2		t_{CK}	
MODE REGISTER SET command period		t_{MRD}	2		2		t_{CK}	
Write preamble setup time		t_{WPRES}	0		0		ns	
Write postamble		t_{WPST}	0.4	0.6	0.4	0.6	t_{CK}	
Write preamble		t_{WPRE}	0.25		0.25		t_{CK}	

Parameter		Sym-bol	-60		-75		Unit	Note
			Min	Max	Min	Max		
Read preamble	CL = 2	t_{RPRE}	0.5	1.1	0.5	1.1	t_{CK}	
	CL = 3		0.9	1.1	0.9	1.1	t_{CK}	
Read postamble		t_{RPST}	0.4	0.6	0.4	0.6	t_{CK}	
ACTIVE to PRECHARGE command period		t_{RAS}	42	70,000	45	70,000	ns	
ACTIVE to ACTIVE command period		t_{RC}	60		60		ns	
AUTO REFRESH to ACTIVE / AUTO REFRESH command period		t_{RFC}	80		80		ns	6
ACTIVE to READ or WRITE delay		t_{RCD}	18		18		ns	
PRECHARGE command period		t_{RP}	18		22.5		ns	
ACTIVE bank A to ACTIVE bank b delay		t_{RRD}	12		15		ns	
Column address to Column address delay		t_{CCD}	1		1		t_{CK}	
WRITE recovery time		t_{WR}	2		2		t_{CK}	
Auto precharge write recovery + precharge time		t_{DAL}	$t_{WR}+t_{RP}$		$t_{WR}+t_{RP}$			2
Internal write to Read command delay		t_{WTR}	1		1		t_{CK}	
Self refresh exit to next valid command delay		t_{XSR}	120		120		ns	
Exit power down to next valid command delay		t_{XP}	$t_{CK}+t_{IS}$		$t_{CK}+t_{IS}$			
CKE min. pulse width(high and low pulse width)		t_{CKE}	1		2		t_{CK}	
Refresh Period		t_{REF}		64		64	ms	

Note:

Table 9: Input Setup/Hold Slew Rate

Input Setup/Hold Slew Rate	Δt_{IS}	Δt_{IH}
(V/ns)	(ps)	(ps)
1.0	0	0
0.8	+50	+50
0.6	+100	+100

1. This derating table is used to increase t_{IS}/t_{IH} in the case where the input slew rate is below 1.0V/ns.

2. Minimum 5CK of t_{DAL} (= t_{WR} + t_{RP}) is required because it need minimum 2CK for t_{WR} and minimum 3CK for t_{RP}.

3. t_{AC}(min) value is measured at the high Vdd(1.95V) and cold temperature(-25°C).
   t_{AC}(max) value is measured at the low Vdd(1.7V) and hot temperature(85°C).
   t_{AC} is measured in the device with half driver strength and under the AC output load condition (Fig.2 in Page 8).

Table 10: I/O Setup/Hold Slew Rate

I/O Setup/Hold Slew Rate	Δt_{DS}	Δt_{DH}
(V/ns)	(ps)	(ps)
1.0	0	0
0.8	+75	+75
0.6	+150	+150

4. This derating table is used to increase t_{DS}/t_{DH} in the case where the I/O slew rate is below 1.0V/ns.

Table 11: I/O Delta Rise/Fall Rate(1/slewrate)

Delta Rise/Fall Rate	Δt_{DS}	Δt_{DH}
(ns/V)	(ps)	(ps)
0	0	0
± 0.25	+50	+50
± 0.5	+100	+100

5. This derating table is used to increase t_{DS}/t_{DH} in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is calculated as 1/SlewRate1-1/SlewRate2. For example, if slew rate 1 = 1.0V/ns and slew rate 2 = 0.8V/ns, then the Delta Rise/Fall Rate = -0.25ns/V.
6. Maximum burst refresh cycle : 8

Functional Description

The 256Mb Mobile DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 268,435,456-bits. It is internally configured as a quad-bank DRAM. Each of the 67,108,864-bit banks is organized as 4,096 rows by 512 columns by 32 bits.

The 256Mb Mobile DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2n-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls. single read or write access for the 256Mb Mobile DDR SDRAM consists of a single 2n-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O balls.

Read and write accesses to the Mobile DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

It should be noted that the DLL signal that is typically used on standard DDR devices is not necessary on the Mobile DDR SDRAM. It has been omitted to save power. Prior to normal operation, the Mobile DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Initialization

Mobile DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. If there is an interruption to the device power, the initialization routine should be followed to ensure proper functionality of the Mobile DDR SDRAM. The clock stop feature is not available until the device has been properly initialized.

To properly initialize the Mobile DDR SDRAM, this sequence must be followed:

1. To prevent device latch-up, it is recommended the core power (VDD) and I/O power (VDDQ) be from the same power source and brought up simultaneously. If separate power sources are used, VDD must lead VDDQ.
2. Once power supply voltages are stable and the CKE has been driven HIGH, it is safe to apply the clock.
3. Once the clock is stable, a 200μs (minimum) delay is required by the Mobile DDR SDRAM prior to applying an exe cutable command. During this time, NOP or DESELECT commands must be issued on the command bus.
4. Issue a PRECHARGE ALL command.
5. Issue NOP or DESELECT commands for at least tRP time.
6. Issue an AUTO REFRESH command followed by NOP or DESELECT commands for at least tRFC time. Issue a second AUTO REFRESH command followed by NOP or DESELECT commands for at least tRFC time. As part of the initialization sequence, two AUTO REFRESH commands must be issued. Typically, both of these com mands are issued at this stage as described above. Alternately, the second AUTO-REFRESH command and NOP or DESELECT sequence can be issued between steps 10 and 11.
7. Using the LOAD MODE REGISTER command, load the standard mode register as desired.
8. Issue NOP or DESELECT commands for at least tMRD time.
9. Using the LOAD MODE REGISTER command, load the extended mode register to the desired operating modes. Note that the sequence in which the standard and extended mode registers are programmed is not critical.
10. Issue NOP or DESELECT commands for at least tMRD time.
11. The Mobile DDR SDRAM has been properly initialized and is ready to receive any valid command.

Register Definition

Mode Registers

The mode registers are used to define the specific mode of operation of the Mobile DDR SDRAM. There are two mode registers used to specify the operational characteristics of the device. The standard mode register, which exists for all SDRAM devices, and the extended mode register, which exists on all Mobile SDRAM devices.

Standard Mode Register

The standard mode register definition includes the selection of a burst length, a burst type, a CAS latency and an operating mode, as shown in page 15. The standard mode register is programmed via the LOAD MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again. Reprogramming the standard mode register will not alter the contents of the memory, provided it is performed correctly. The mode register must be loaded (reloaded) when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation. Mode register bits A0-A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4-A6 specify the CAS latency, and A7-A11 specify the operating mode.

Note: Standard refers to meeting JEDEC-standard mode register definitions.

Burst Length

Read and write accesses to the Mobile DDR SDRAM are burst oriented, with the burst length being programmable, as shown in page 15. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, 8, or 16 are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected by A3. The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address. See Table 17~20 on page 17~18 for more information.

CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 2 or 3 clocks, as shown in page 15.

For CL = 3, if the READ command is registered at clock edge n, then the data will nominally be available at (n + 2 clocks + tAC). For CL = 2, if the READ command is registered at clock edge n, then the data will be nominally be available at (n + 1 clock + tAC).

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Operating Mode

The normal operating mode is selected by issuing a LOAD MODE REGISTER SET command with bits A7-A11 each set to zero, and bits A0-A6 set to the desired values. All other combinations of values for A7-A11 are reserved for future use and/or test modes. Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Extended Mode Register

The extended mode register controls functions specific to low power operation. These additional functions include drive strength, temperature compensated self refresh, and partial array self refresh.

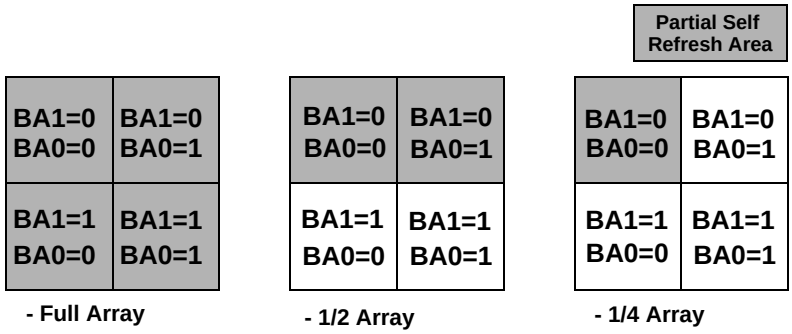
This device has default values for the extended mode register (if not programmed, the device will operate with the default values . PASR = Full Array, DS = Full Drive).

Temperature Compensated Self Refresh

On this version of the Mobile DDR SDRAM, a temperature sensor is implemented for automatic control of the self refresh oscillator on the device. Programming of the temperature compensated self refresh (TCSR) bits will have no effect on the device. The self refresh oscillator will continue refresh at the factory programmed optimal rate for the device temperature.

Partial Array Self Refresh

For further power savings during SELF REFRESH, the PASR feature allows the controller to select the amount of memory that will be refreshed during SELF REFRESH. Low Power DDR SDRAM supports 3 kinds of PASR in self refresh mode : Full Array, 1/2 of Full Array and 1/4 of Full Array.



Output Driver Strength

Because the Mobile DDR SDRAM is designed for use in smaller systems that are mostly point to point, an option to control the drive strength of the output buffers is available. Drive strength should be selected based on the expected loading of the memory bus. Bits A5 and A6 of the extended mode register can be used to select the driver strength of the DQ outputs.

Stopping the External Clock

One method of controlling the power efficiency in applications is to throttle the clock which controls the Mobile DDR SDRAM. There are two basic ways to control the clock:

1. Change the clock frequency, when the data transfers require a different rate of speed.

2. Stopping the clock altogether.

Both of these are specific to the application and its requirements and both allow power savings due to possible less transitions on the clock path.

The Mobile DDR SDRAM allows the clock to change frequency during operation, only if all the timing parameters are met with respect to that change and all refresh requirements are satisfied.

The clock can also be stopped all together, if there are no data accesses in progress, either WRITEs or READs that would be effected by this change; i.e., if a WRITE or a READ is in progress the entire data burst must be through the pipeline prior to stopping the clock. CKE must be held HIGH with CK = LOW and CKB = HIGH for the full duration of the clock stop mode. One clock cycle and at least one NOP is required after the clock is restarted before a valid command can be issued.

It is recommended that the Mobile DDR SDRAM should be in a precharged state if any changes to the clock frequency are expected. This will eliminate timing violations that may otherwise occur during normal operational accesses.

Table 12: MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with Normal MRS

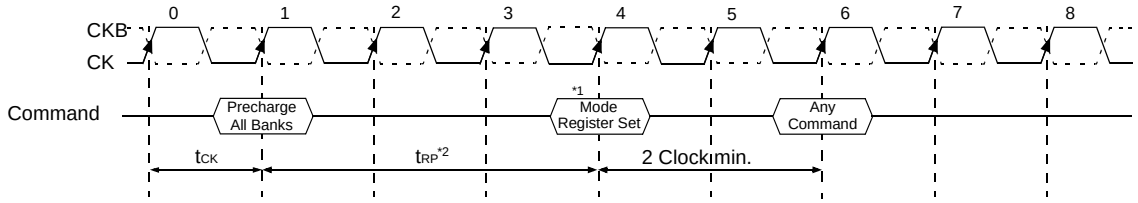
Address	BA0 ~ BA1	A11 ~ A10/AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	"0" Setting for Normal MRS	RFU*1		Operating Mode		CAS Latency			BT	Burst Length		

NOTE :
1. RFU(Reserved for future use) should stay “0” during MRS cycle.

Table 13: Normal MRS Mode

Operating Mode			CAS Latency				Burst Type			Burst Length			
A8	A7	Type	A6	A5	A4	Latency	A3	Type		A2	A1	A0	DDR
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential		0	0	0	Reserved
0	1	Reserved	0	0	1	Reserved	1	Interleave		0	0	1	2
1	0	Reserved	0	1	0	2	Mode Select			0	1	0	4
1	1	Reserved	0	1	1	3	BA1	BA0	Mode	0	1	1	8
-	-	-	1	0	0	Reserved	0	0	Setting for Normal MRS	1	0	0	16
-	-	-	1	0	1	Reserved				1	0	1	Reserved
-	-	-	1	1	0	Reserved				1	1	0	Reserved
-	-	-	1	1	1	Reserved				1	1	1	Reserved

Mode Register Set



NOTE :
1. MRS can be issued only at all bank precharge state.
2. Minimum tRP is required to issue MRS command.

Table 14: Register Programmed with Extended MRS

Address	BA1	BA0	A11 ~ A10/AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	Mode Select		RFU*1				DS		RFU*1		PASR		

NOTE :
1. RFU(Reserved for future use) should stay “0” during MRS and EMRS cycle.

Table 15: EMRS for PASR(Partial Array Self Refresh) & DS(Driver Strength)

Mode Select			Driver Strength			PASR			
BA1	BA0	MODE	A6	A5	Driver Strength	A2	A1	A0	Size of Refreshed Array
0	0	Normal MRS	0	0	Full	0	0	0	Full Array
0	1	Reserved	0	1	1/2	0	0	1	1/2 of Full Array
1	0	EMRS for DDR SDRAM	1	0	1/4	0	1	0	1/4 of Full Array
1	1	Reserved	1	1	Reserved	0	1	1	Reserved
						1	0	0	Reserved
						1	0	1	Reserved
						1	1	0	Reserved
						1	1	1	Reserved

Table 16: Internal Temperature Compensated Self Refresh (TCSR)

Temperature Range	Self Refresh Current (I_{DD} 6)			Unit
	Full Array	1/2 of Full Array	1/4 of Full Array	
Max 85℃	400	300	250	μA
Max 45℃	250	200	150	

NOTE :
1. In order to save power consumption, Mobile DDR SDRAM includes the internal temperature sensor and control units to control the self refresh cycle automatically according to the two temperature range : Max 85℃, Max 45℃
2. If the EMRS for external TCSR is issued by the controller, this EMRS code for TCSR is ignored.
3. It has +/- 5 ℃ tolerance.

BURST SEQUENCE

Table 17: BURST LENGTH = 2

Initial Address	Sequential		Interleave	
A0				
0	0	1	0	1
1	1	0	1	0

Table 18: BURST LENGTH = 4

Initial Address		Sequential				Interleave			
A1	A0								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

Table 19: BURST LENGTH = 8

Initial Address			Sequential								Interleave							
A2	A1	A0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

Table 20: BURST LENGTH = 16

Initial Address				Sequential																Interleave															
A3	A2	A1	A0																																
0	0	0	0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	1	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	0	3	2	5	4	7	6	9	8	11	10	13	12	15	14
0	0	1	0	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	0	1	6	7	4	5	10	11	8	9	14	15	12	13
0	0	1	1	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	2	1	0	7	6	5	4	11	10	9	8	15	14	13	12
0	1	0	0	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	0	1	2	3	12	13	14	15	8	9	10	11
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0	1	1	0	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	4	5	2	3	0	1	14	15	12	13	10	11	8	9
0	1	1	1	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8
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1	0	1	0	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	10	11	8	9	14	15	12	13	2	3	0	1	6	7	4	5
1	0	1	1	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	10	11	10	9	8	15	14	13	12	3	2	1	0	7	6	5	4
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1	1	0	1	13	14	15	0	1	2	3	4	5	6	7	8	9	10	11	12	13	12	15	14	9	8	11	10	5	4	7	6	1	0	3	2
1	1	1	0	14	15	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	12	13	10	11	8	9	6	7	4	5	2	3	0	1
1	1	1	1	15	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Commands

DESELECT

The DESELECT function (CSB HIGH) prevents new commands from being executed by the Mobile DDR SDRAM. The Mobile DDR SDRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected DDR SDRAM to perform a NOP (CSB = LOW, RASB = CASB = WEB = HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER

The mode register is loaded via inputs A0-A11, BA0, BA1. The LOAD MODE REGISTER and LOAD EXTENDED MODE REGISTER commands can only be issued when all banks are idle, and a subsequent executable command cannot be issued until tMRD is met.

The values of the mode register and extended mode register will be retained even when exiting deep power-down.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A11 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A8 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A8 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (tRP) after the precharge command is issued. Except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as “Don’t Care”. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank (idle state), or if the previously open row is already in the process of precharging.

AUTO PRECHARGE

AUTO PRECHARGE is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. Auto precharge is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command. This device supports concurrent auto precharge if the command to the other bank does not interrupt the data transfer to the current bank.

AUTO PRECHARGE ensures that the precharge is initiated at the earliest valid stage within a burst. This “earliest valid stage” is determined as if an explicit PRECHARGE command was issued at the earliest possible time, without violating tRAS (MIN), as described for each burst type in “Operations”. The user must not issue another command to the same bank until the precharge time (tRP) is completed.

BURST TERMINATE

The BURST TERMINATE command is used to truncate READ bursts (with auto precharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as shown in “Operations”. The open page which the READ burst was terminated from remains open.

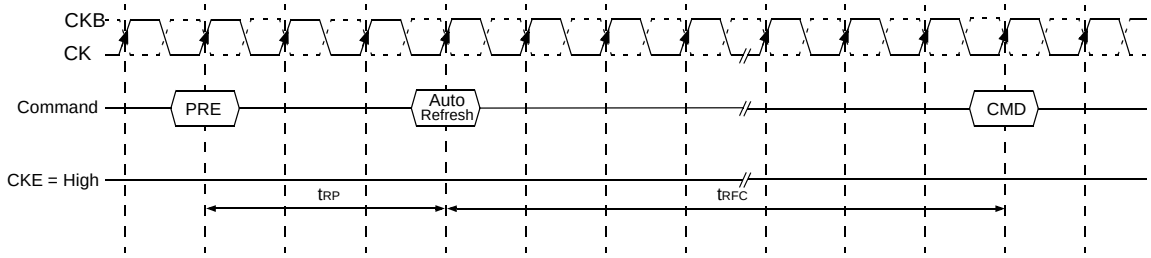
AUTO REFRESH

AUTO REFRESH is used during normal operation of the Mobile DDR SDRAM and is analogous to CAS-BEFORE-RAS (CBR) REFRESH in FPM/EDO DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required.

The addressing is generated by the internal refresh controller. This makes the address bits a “Don’t Care” during an AUTO REFRESH command. The 256Mb Mobile DDR SDRAM requires AUTO REFRESH cycles at an average interval of 15.625µs (maximum).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. Although not a JEDEC requirement, to provide for future functionality features, CKE must be active (HIGH) during the auto refresh period. The auto refresh period begins when the AUTO REFRESH command is registered and ends tRFC later.

Auto Refresh



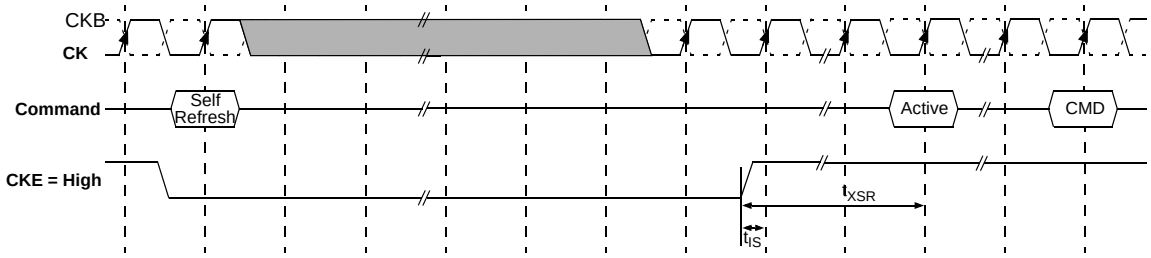
SELF REFRESH

The SELF REFRESH command can be used to retain data in the Mobile DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the Mobile DDR SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). All command and address input signals except CKE are “Don’t Care” during SELF REFRESH.

During SELF REFRESH, the device is refreshed as identified in the external mode register (see PASR setting). For the full array refresh, all four banks are refreshed simultaneously with the refresh frequency set by an internal self refresh oscillator. This oscillator changes due to the temperature sensor’s input. As the case temperature of the Mobile DDR SDRAM increases, the oscillation frequency will change to accommodate the change of temperature. This happens because the DRAM capacitors lose charge faster at higher temperatures. To ensure efficient power dissipation during self refresh, the oscillator will change to refresh at the slowest rate possible to maintain the devices data.

The procedure for exiting SELF REFRESH requires a sequence of commands. First, CK must be stable prior to CKE going back HIGH. Once CKE is HIGH, the Mobile DDR SDRAM must have NOP commands issued for tXSR is required for the completion of any internal refresh in progress.

Self Refresh



DEEP POWER-DOWN

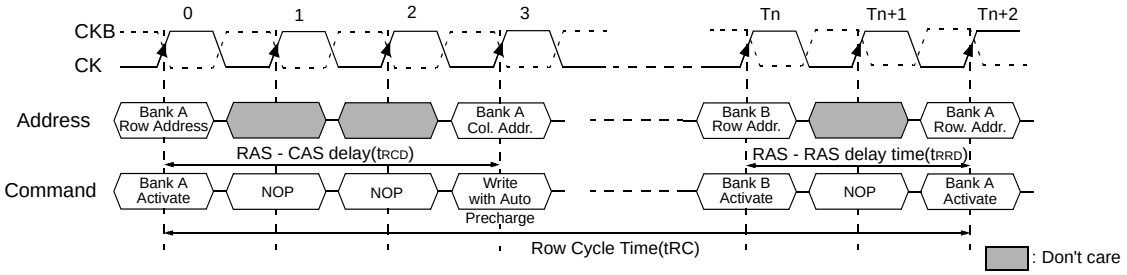
The operating mode deep power-down achieves maximum power reduction by eliminating the power of the whole memory array of the device. Array data will not be retained once the device enters deep power-down mode.
This mode is entered by having all banks idle then CSB and WEB held LOW with RASB and CASB held HIGH at the rising edge of the clock, while CKE is LOW. This mode is exited by asserting CKE HIGH.

Operations

Bank/Row Activation

The Bank Activation command is issued by holding CASB and WEB high with CSB and RASB low at the rising edge of the clock(CK). The DDR SDRAM has four independent banks, so two bank select addresses(BA0, BA1) are required. The Bank Activation command must be applied before any READ or WRITE operation is executed. The delay from the Bank Activation command to the first READ or WRITE command must meet or exceed the minimum of RAS to CAS delay time(tRCD min). Once a bank has been activated, it must be precharged before another Bank Activation command can be applied to the same bank. The minimum time interval between interleaved Bank Activation commands(Bank A to Bank B and vice versa) is the Bank to Bank delay time(tRRD min).

Bank Activation Command Cycle



READs

READ bursts are initiated with a READ command.

The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the READ commands used in the following illustrations, auto precharge is disabled.

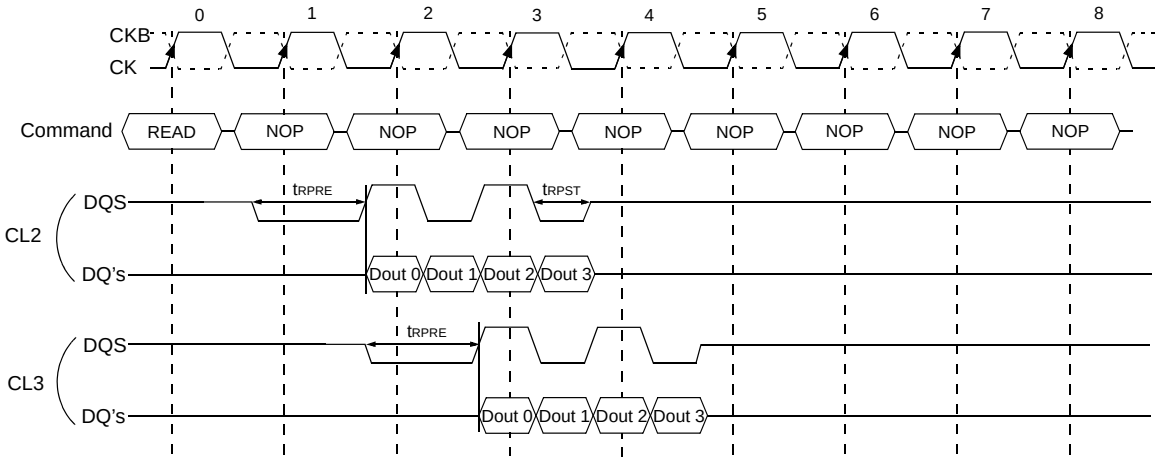
During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge (i.e., at the next crossing of CK and CKB). DQS is driven by the Mobile DDR SDRAM along with output data. The initial LOW state on DQS is known as the read preamble; the LOW state coincident with the last data-out element is known as the read postamble.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z.

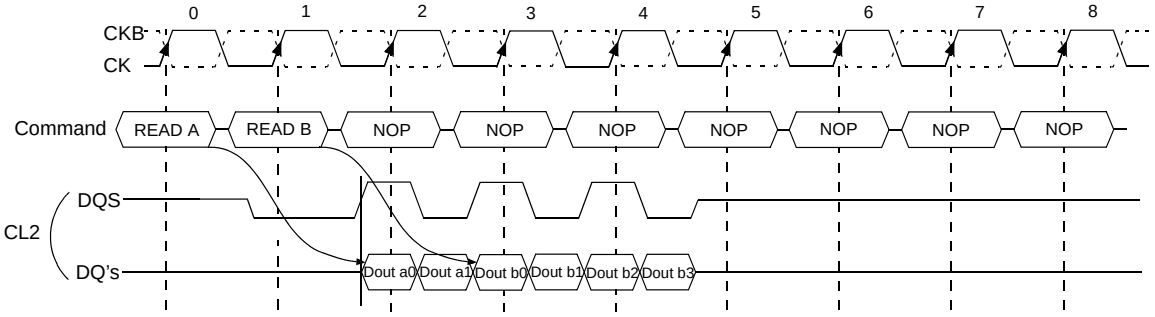
Data from any READ burst may be concatenated with or truncated with data from a subsequent READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new READ command should be issued x cycles after the first READ command, where x equals the number of desired data element pairs (pairs are required by the 2n-prefetch architecture).

A READ command can be initiated on any clock cycle following a previous READ command.

Burst Read Operation < Burst Length=4, CAS Latency=2, 3) >



Read Interrupted by a Read < Burst Length=4, CAS Latency = 2 >



Truncated READs

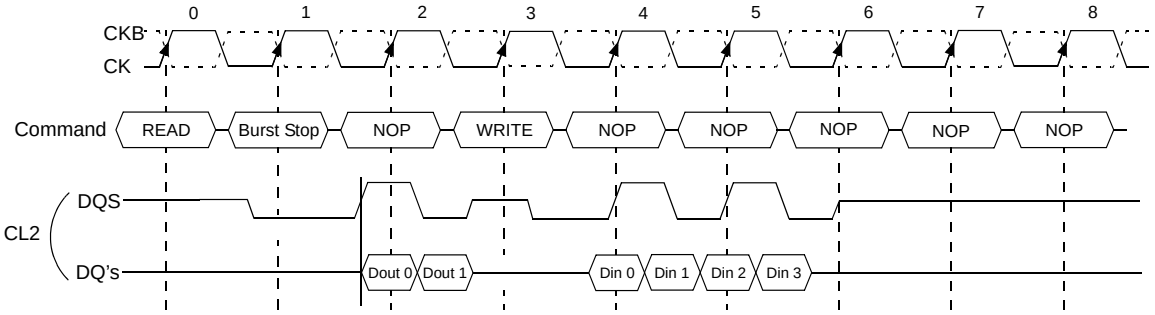
Data from any READ burst may be truncated with a BURST TERMINATE command. The BURST TERMINATE latency is equal to the READ (CAS) latency, i.e., the BURST TERMINATE command should be issued x cycles after the READ command, where x equals the number of desired data element pairs (pairs are required by the 2n-prefetch architecture).

Data from any READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used.

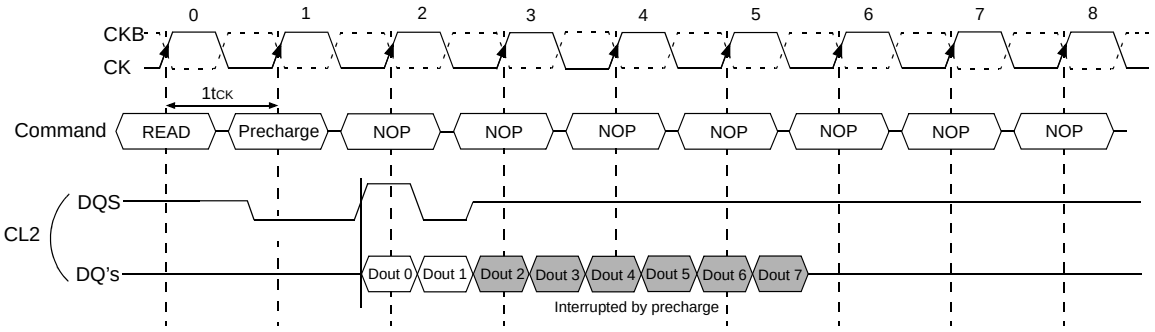
A READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank provided that auto precharge was not activated. The PRECHARGE command should be issued x cycles after the READ command, where x equals the number of desired data element pairs (pairs are required by the 2n-prefetch architecture). Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met.

Note: Part of the row precharge time is hidden during the access of the last data elements.

Read Interrupted by a Write & Burst Stop < Burst Length=4, CAS Latency = 2 >



Read Interrupted by a Precharge < Burst Length=8, CAS Latency = 2 >



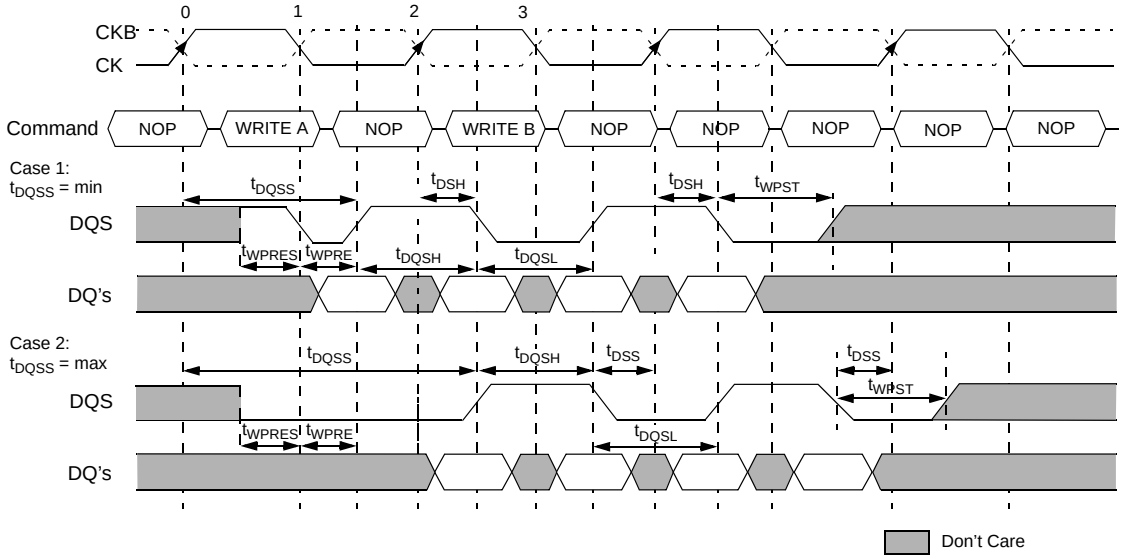
WRITEs

WRITE bursts are initiated with a WRITE command. The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the WRITE commands used in the following illustrations, auto precharge is disabled. During WRITE bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and subsequent data elements will be registered on successive edges of DQS. The LOW state on DQS between the WRITE command and the first rising edge is known as the write preamble; the LOW state on DQS following the last data-in element is known as the write postamble.

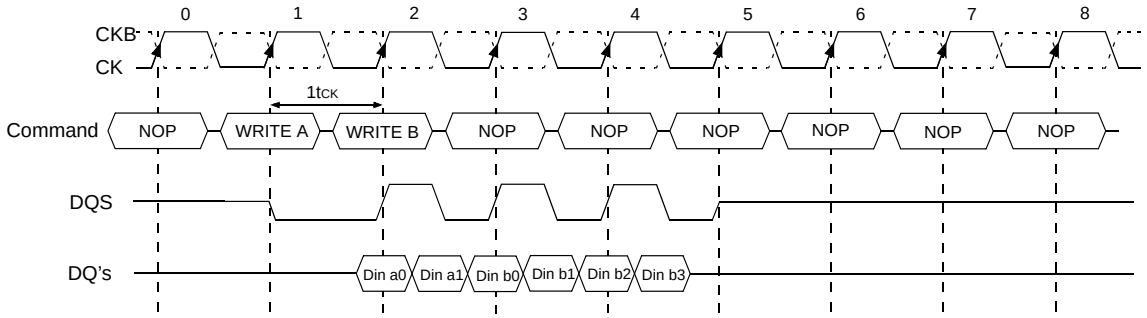
The time between the WRITE command and the first corresponding rising edge of DQS (tDQSS) is specified with a relatively wide range (from 75 percent to 125 percent of one clock cycle). Upon completion of a burst, assuming no other commands have been initiated, the DQs will remain High-Z and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data can be maintained. The new WRITE command can be issued on any positive edge of clock following the previous WRITE command. The first data element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new WRITE command should be issued x cycles after the first WRITE command, where x equals the number of desired data element pairs (pairs are required by the 2n-prefetch architecture).

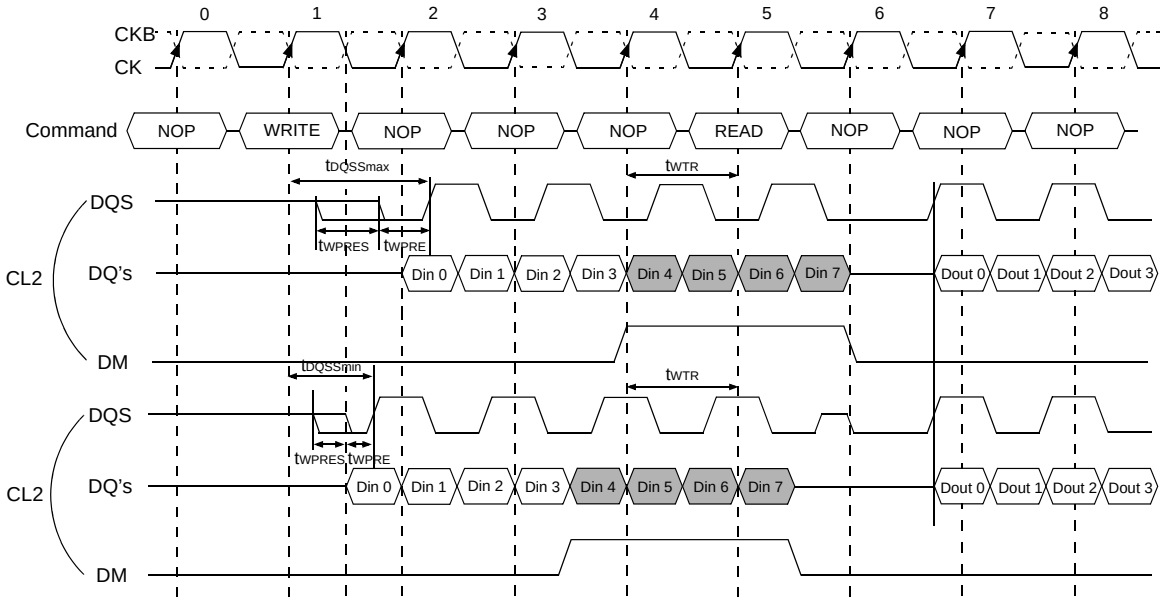
Burst Write Operation < Burst Length=4 >



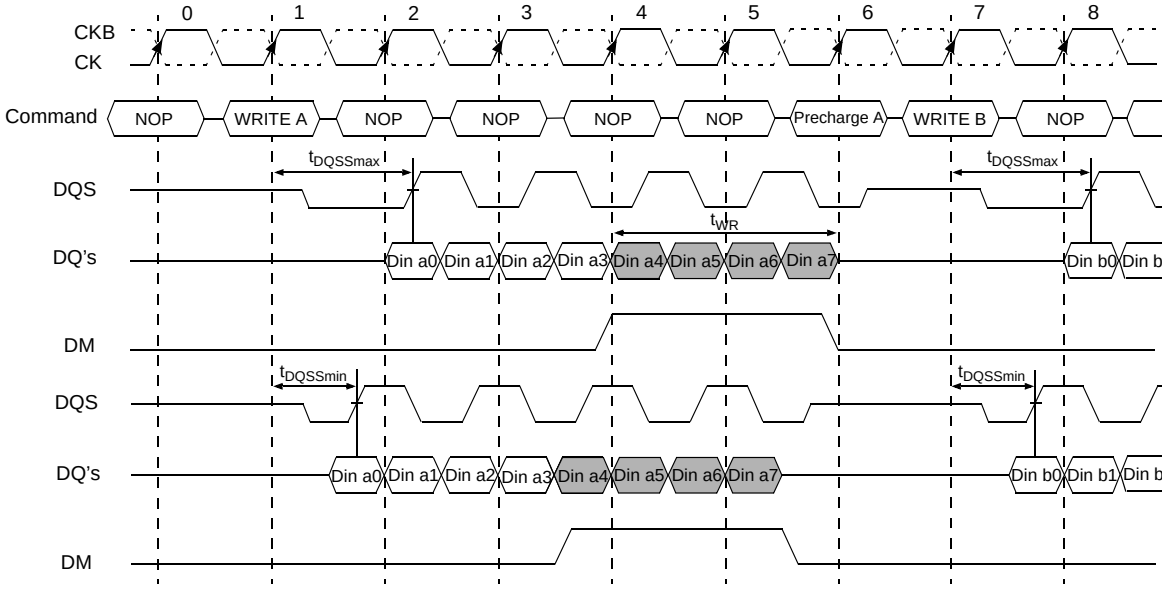
Write Interrupted by a Write < Burst Length=4 >



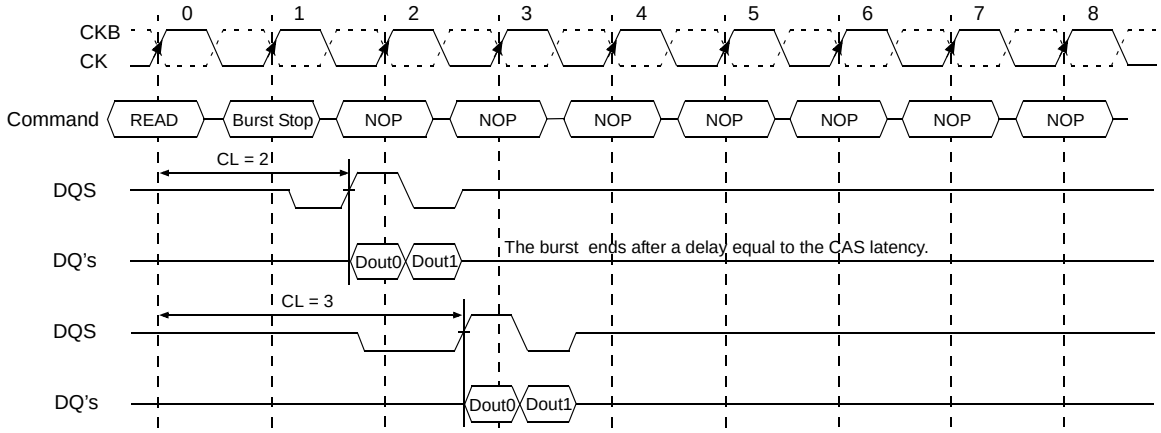
Write Interrupted by a Read & DM < Burst Length=8, CAS Latency =2 >



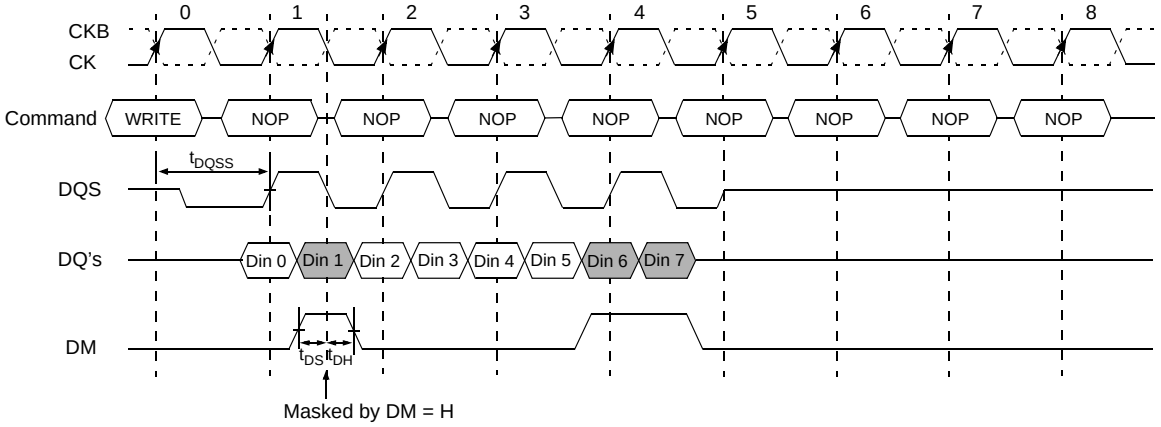
Write Interrupted by a Precharge & DM < Burst Length = 8 >



Burst Stop < Burst Length = 4, CAS Latency = 2, 3 >



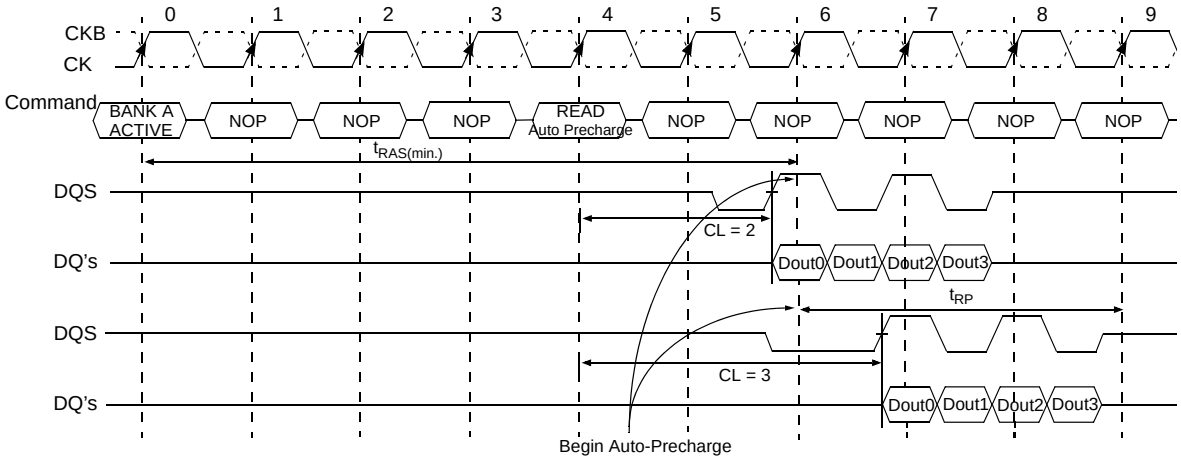
DM Masking < Burst Length = 8 >



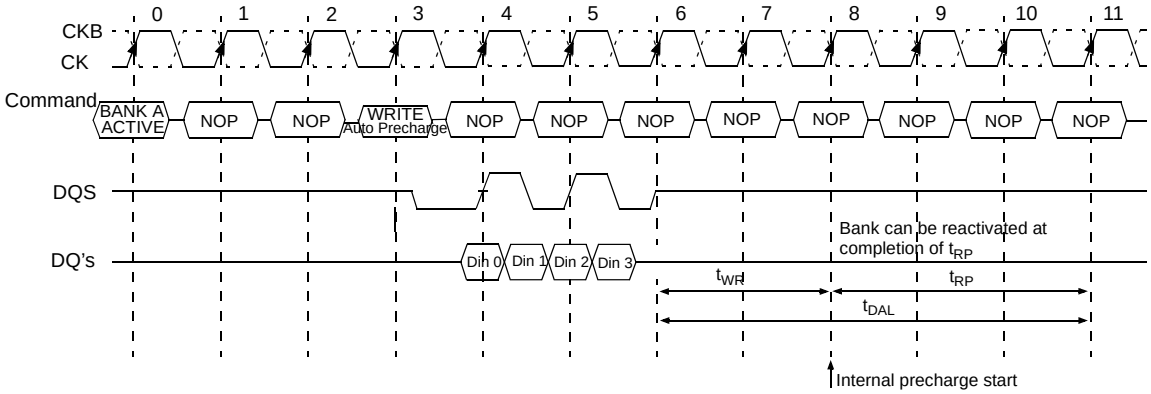
PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (tRP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as Don't Care. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

Read with Auto Precharge < Burst Length = 4, CAS Latency = 2, 3 >



Write with Auto Precharge < Burst Length = 4 >



POWER-DOWN

Power-down is entered when CKE is registered LOW. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, including CK and CKB. Exiting power-down requires the device to be at the same voltage as when it entered power-down and a stable clock.

Note: The power-down duration is limited by the refresh requirements of the device.

While in power-down, CKE LOW must be maintained at the inputs of the Mobile DDR SDRAM, while all other input signals are Don't Care. The power-down state is synchronously exited when CKE is registered HIGH (in conjunction with a NOP or DESELECT command). NOPs or DESELECT commands must be maintained on the command bus until t_{XP} is satisfied.

Power down

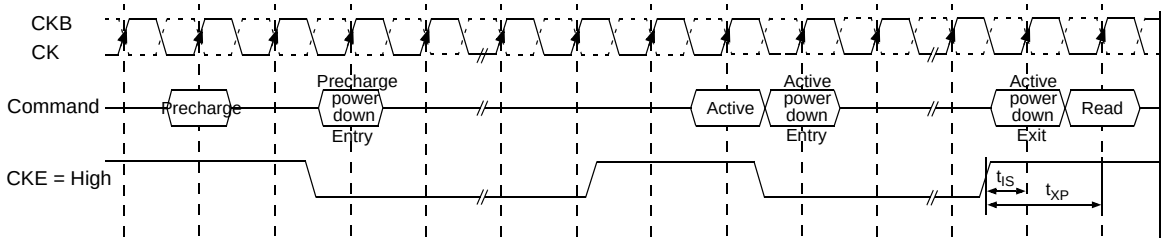


Table 21: SIMPLIFIED TRUTH TABLE

(V=Valid, X =Don't care, H=Logic High, L=Logic Low)

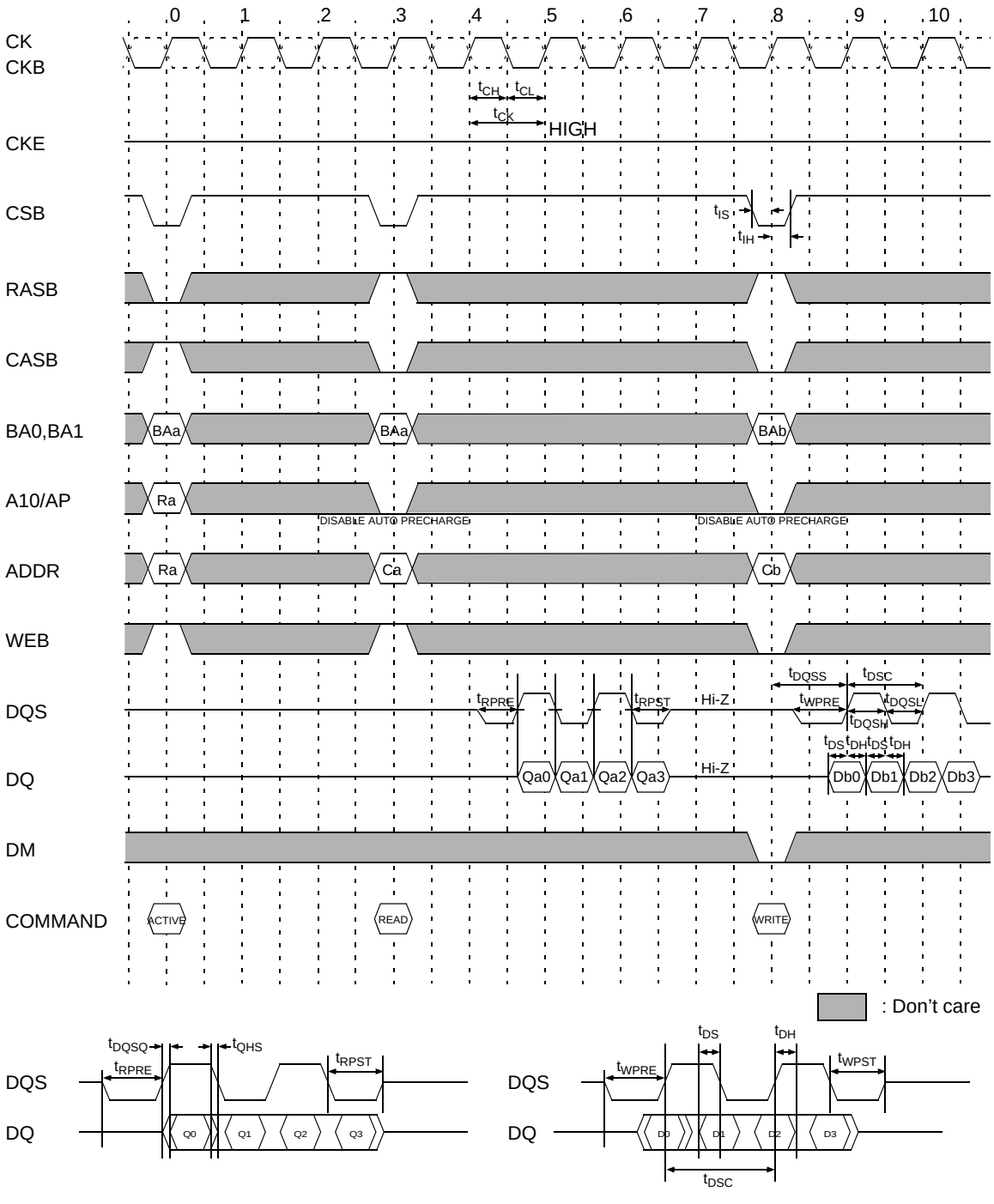
COMMAND			CKEn-1	CKEn	CSB	RASB	CASB	WEB	BA0,1	A10/AP	A11 A9 ~ A0	Note
Register	Mode Register Set		H	X	L	L	L	L	OP CODE			1, 2
Refresh	Auto Refresh		H	H	L	L	L	H	X			3
	Self Refresh	Entry		L								3
		Exit	L	H	L	H	H	H	X			3
					H	X	X	X				3
Bank Active & Row Addr.			H	X	L	L	H	H	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable									H		4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	L	Column Address (A0~A8)	4
	Auto Precharge Enable									H		4, 6
Burst Stop			H	X	L	H	H	L	X			7
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X	
	All Banks								X	H		5
Active Power Down		Entry	H	L	H	X	X	X	X			
					L	H	H	H				
		Exit	L	H	H	X	X	X				
					L	H	H	H				
Precharge Power Down		Entry	H	L	H	X	X	X	X			
					L	H	H	H				
		Exit	L	H	H	X	X	X				
					L	H	H	H				
Deep Power Down		Entry	H	L	L	H	H	L	X			
		Exit	L	H	H	X	X	X				10
DM			H	X					X			8
No Operation Command(NOP)			H	X	H	X	X	X	X			9
					L	H	H	H				9

NOTE :

1. OP Code : Operand Code
   A0 ~ A11 & BA0 ~ BA1 : Program keys. (@EMRS/MRS)
2. EMRS/MRS can be issued only at all banks precharge state.
   A new command can be issued 2 CLK cycles after EMRS or MRS.
3. Auto refresh functions are the same as CBR refresh of DRAM.
   Auto/self refresh can be issued only at all banks precharge state.
4. BA0 ~BA1 : Bank select addresses.
5. If A10/AP is “High” at row precharge, BA0 and BA1 are ignored and all banks are selected.
6. During burst write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
7. Burst stop command is valid at every burst length.
8. DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges(Write DM latency is 0).
9. This combination is not defined for any function, which means “No Operation(NOP)” in DDR SDRAM.
10. The Deep Power Down Mode is exited by asserting CKE high and full initialization is required after exiting Deep Power Down Mode.

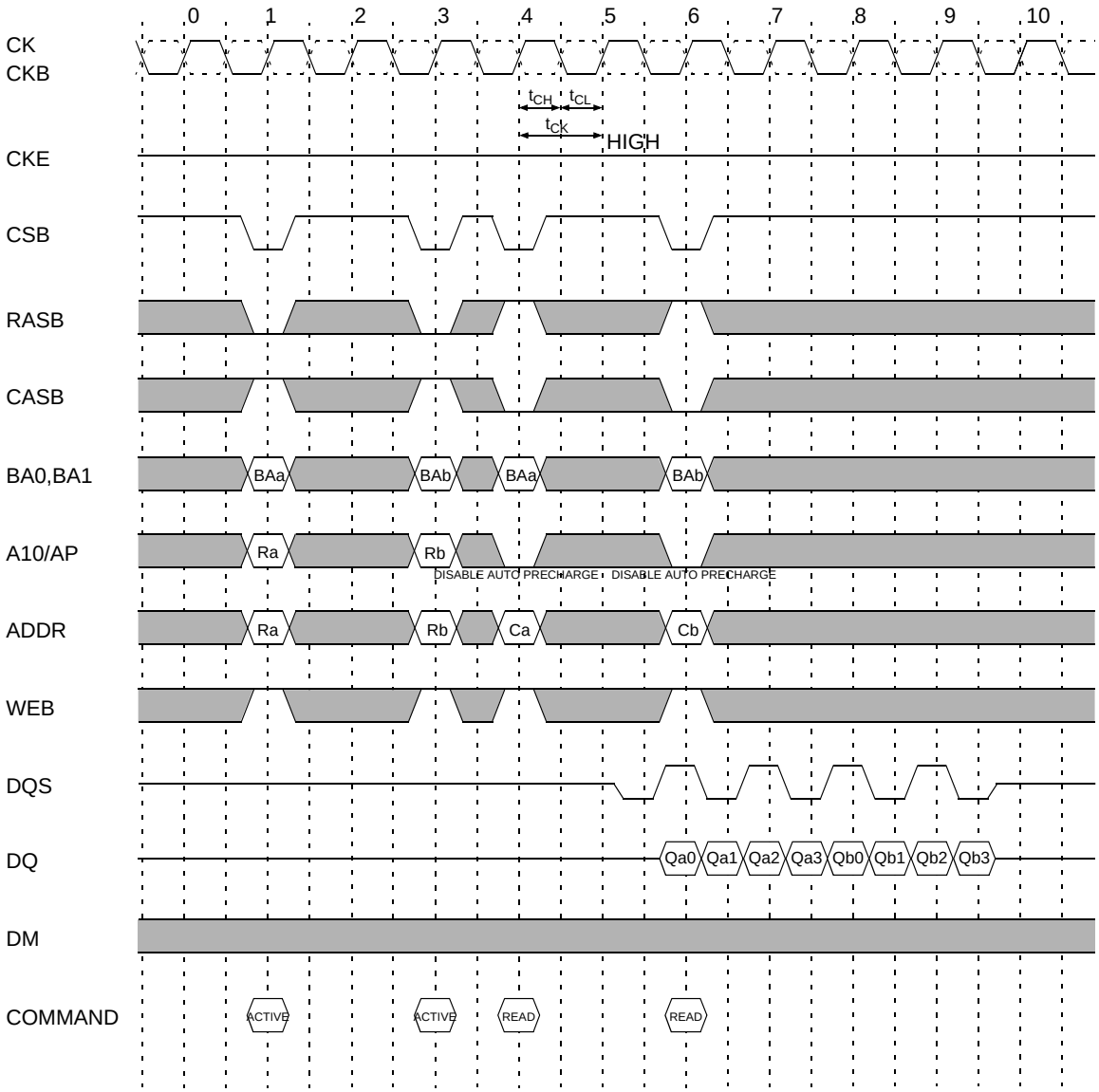
Timing Diagrams

Basic Timing (Setup, Hold and Access Time @ BL=4, CL=2)

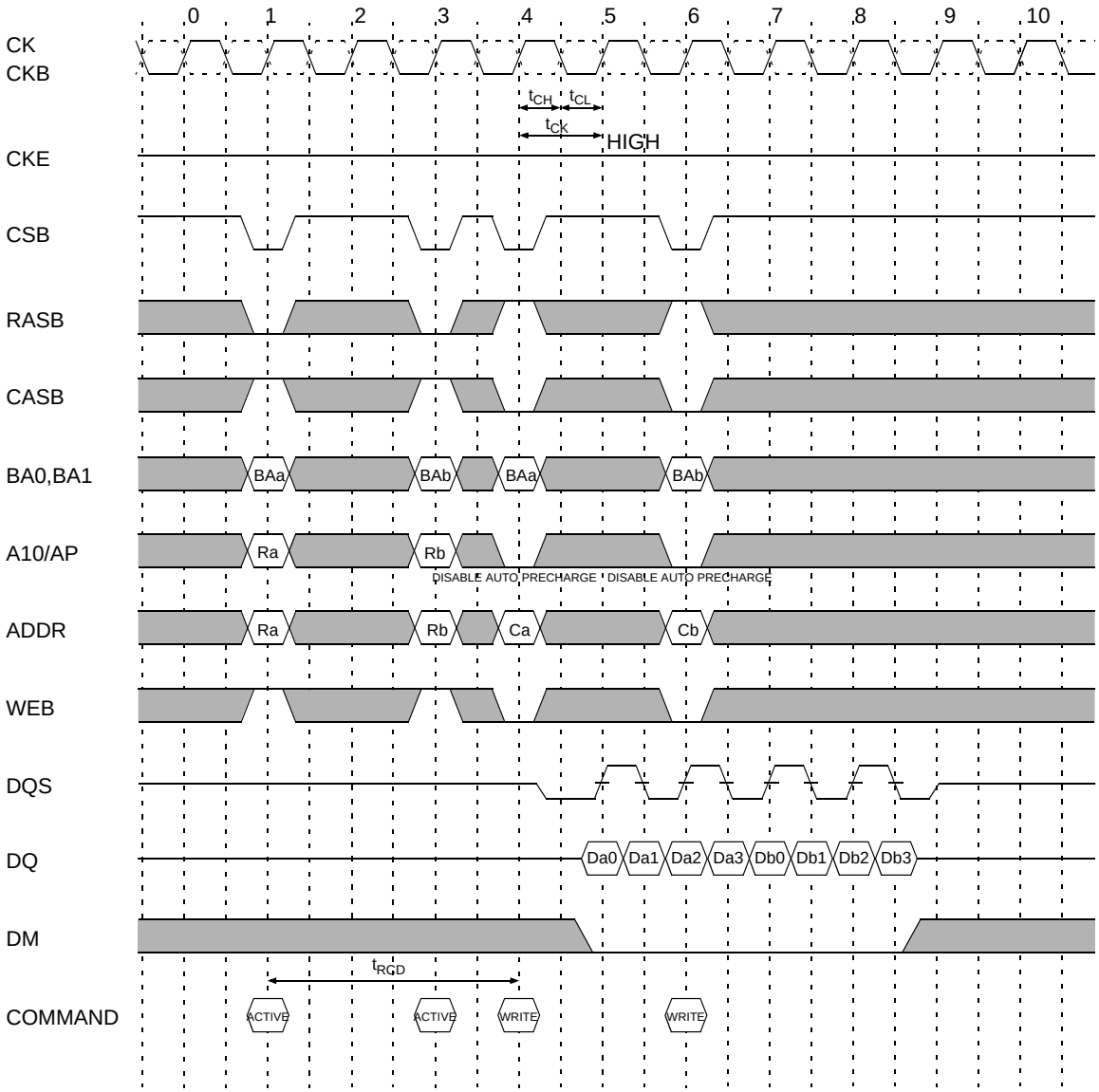


READ Operation **WRITE Operation**

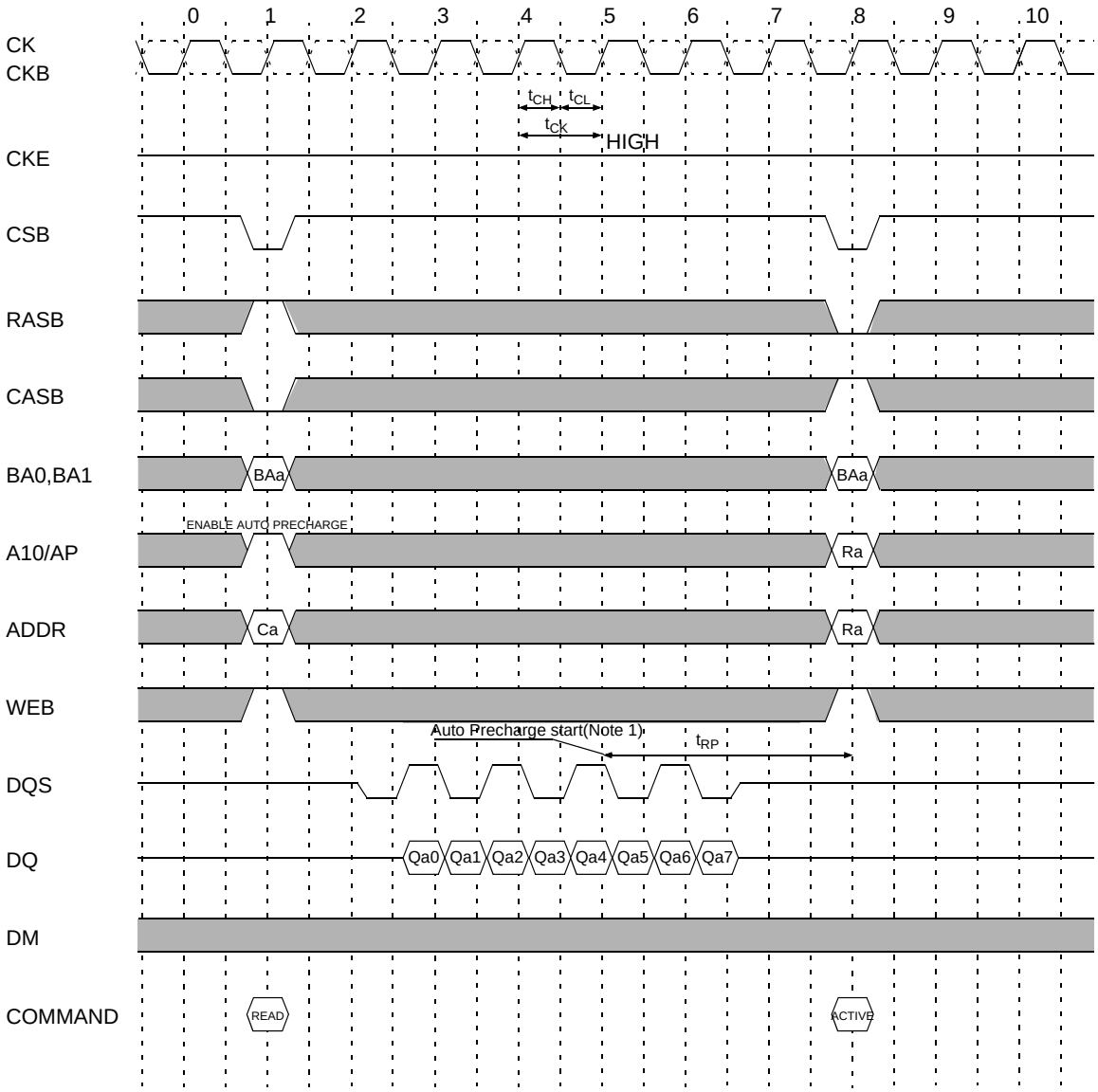
Multi Bank Interleaving READ (@ BL=4, CL=2)



Multi Bank Interleaving WRITE (@ BL=4)

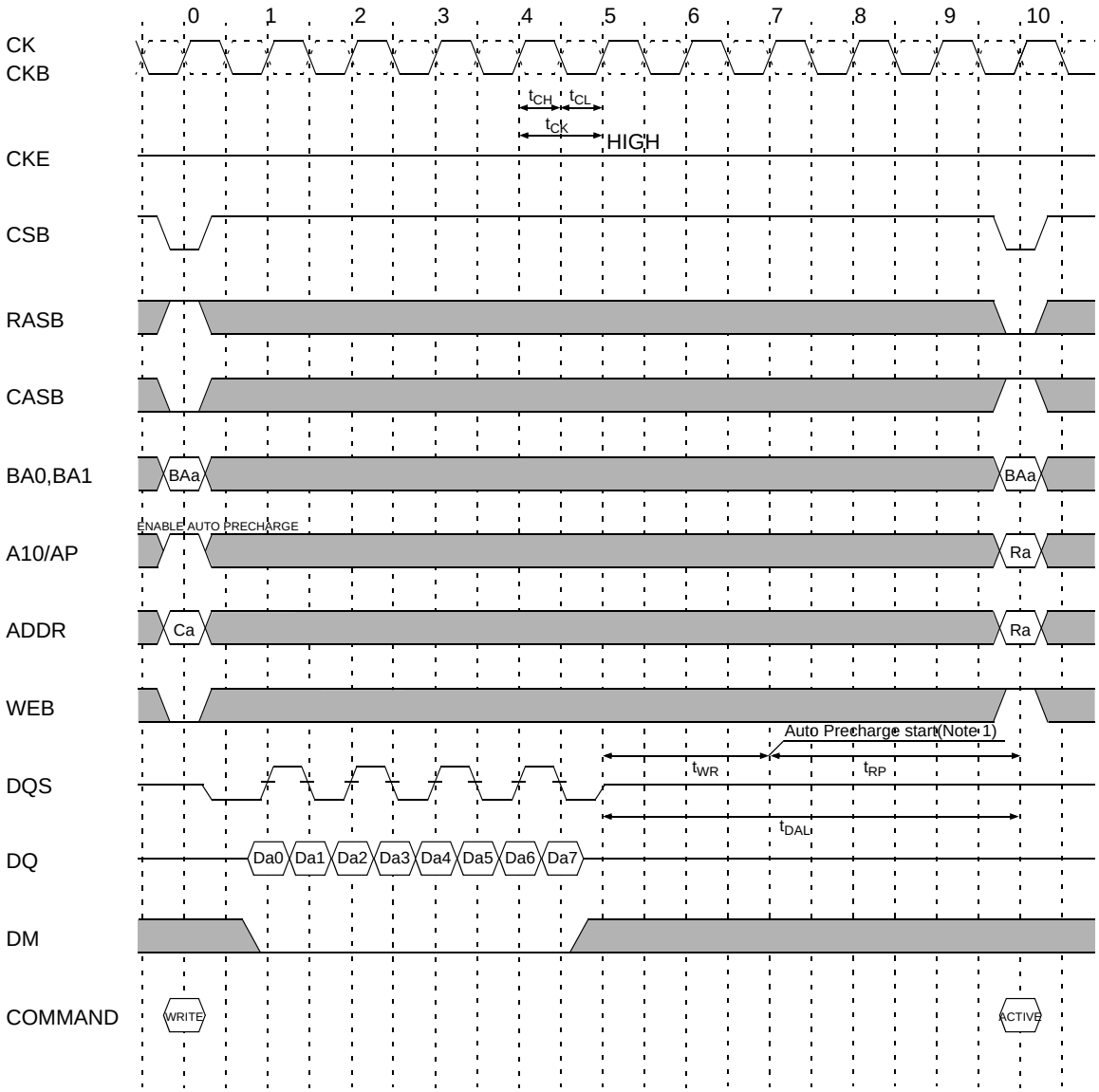


READ with Auto Precharge (@ BL=8, CL=2)



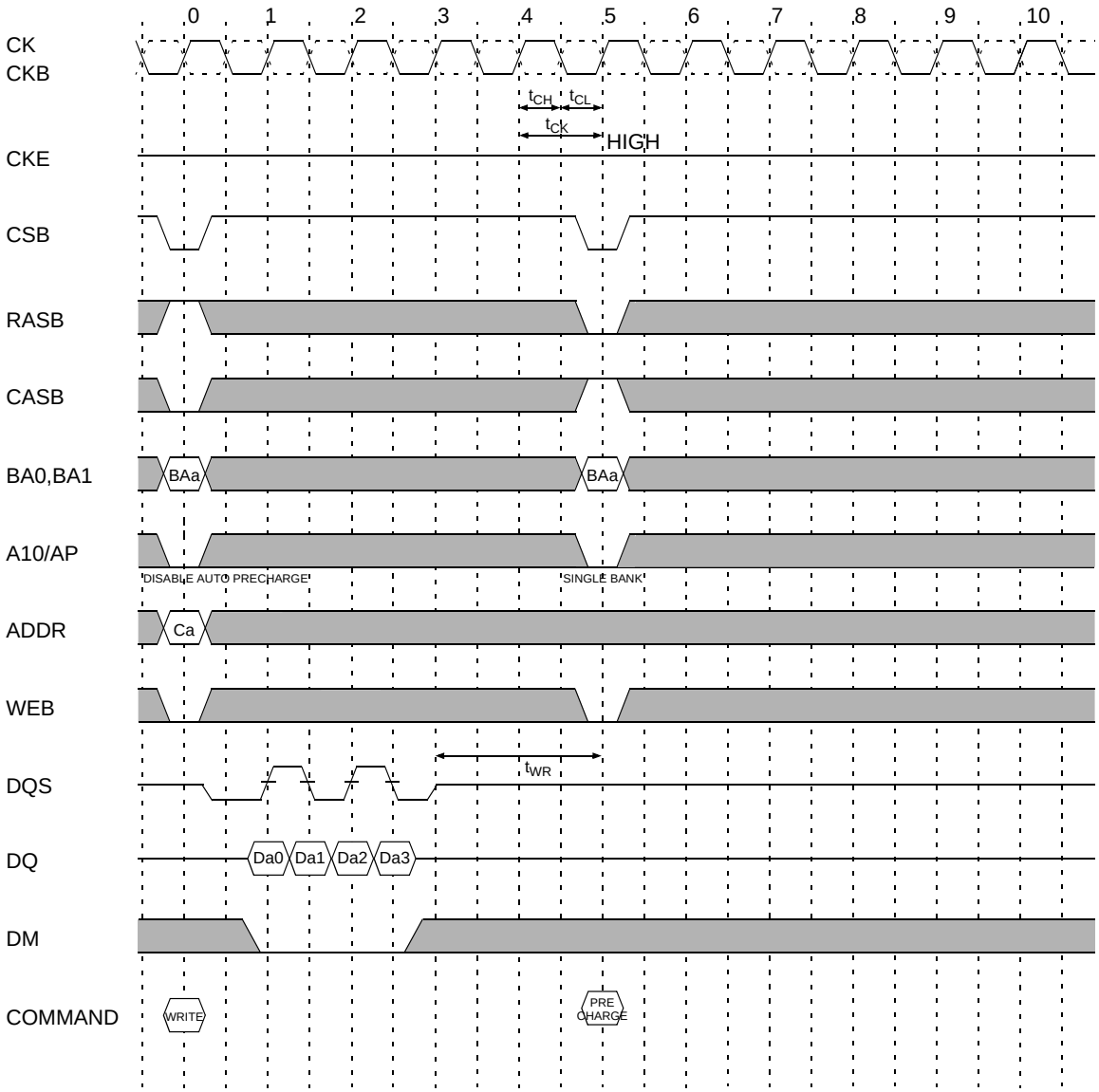
Note 1 The row active command of the precharged bank can be issued after tRP from this point
The new read/write command of another activated bank can be issued from this point
At burst read/write with auto precharge, CAS interrupt of the same is illegal

WRITE with Auto Precharge (@ BL=8)

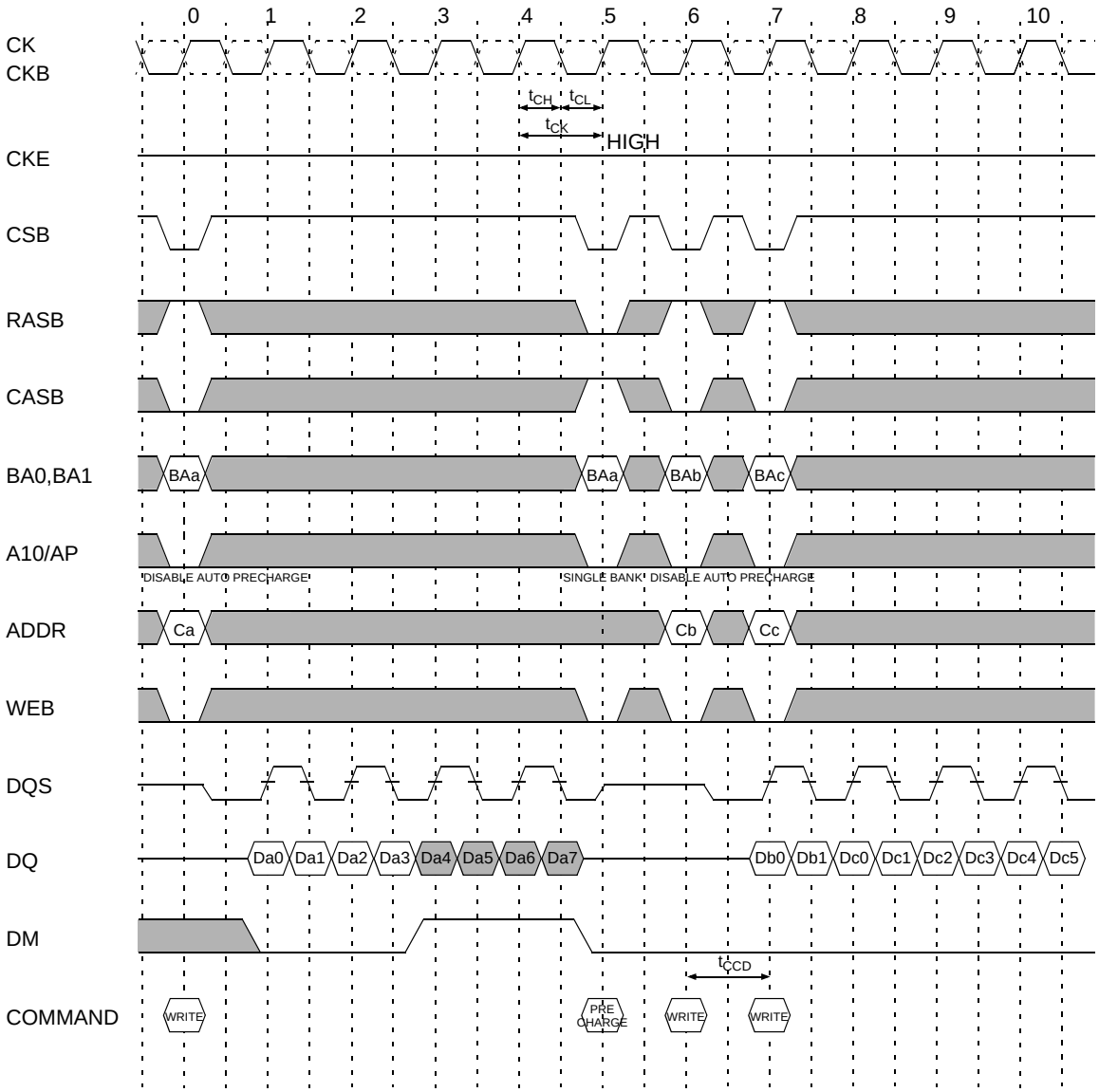


Note 1 The row active command of the precharged bank can be issued after tRP from this point
The new read/write command of another activated bank can be issued from this point
At burst read/write with auto precharge, CAS interrupt of the same bank/another bank is illegal

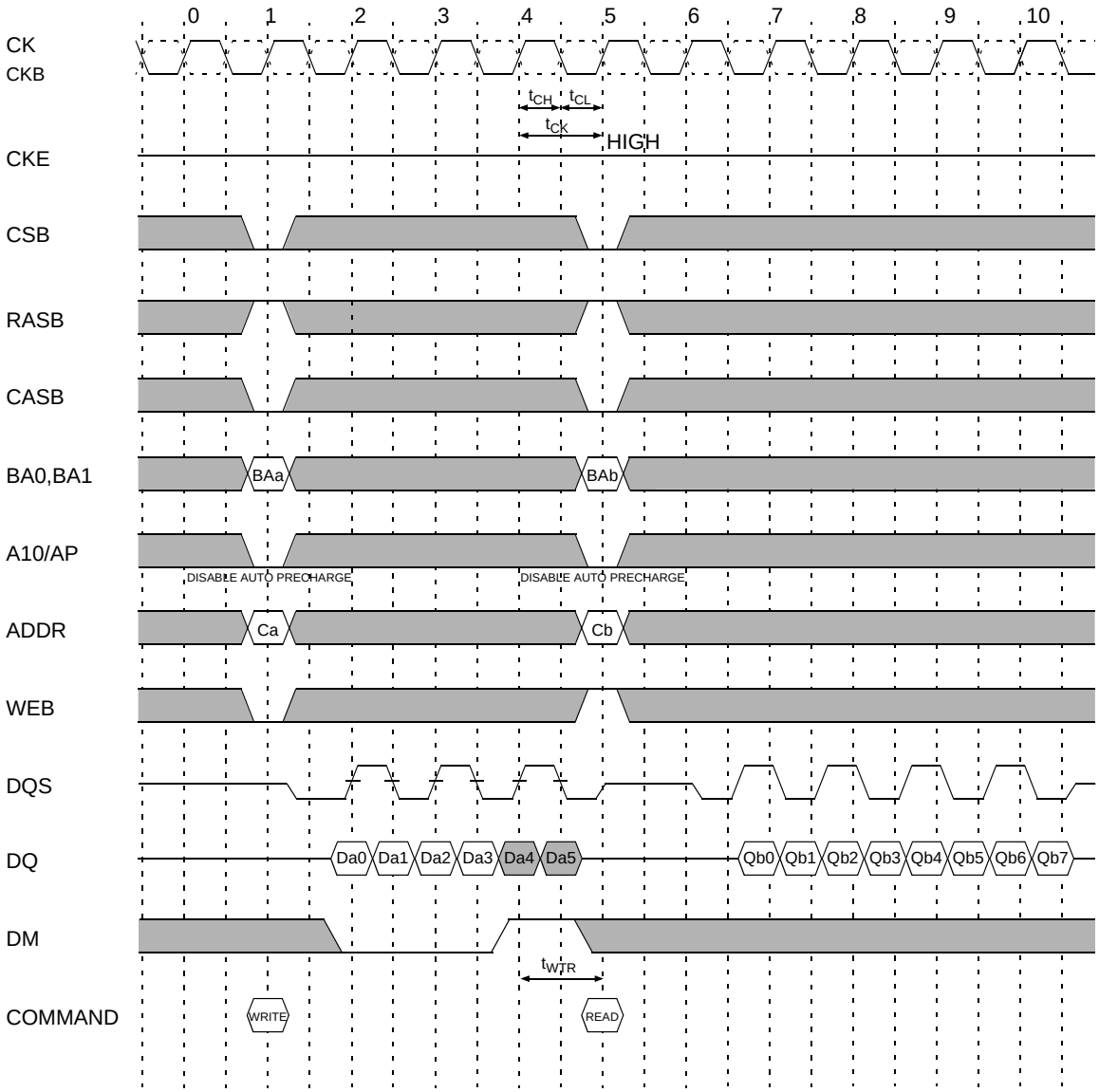
WRITE followed by Precharge (@ BL=4)



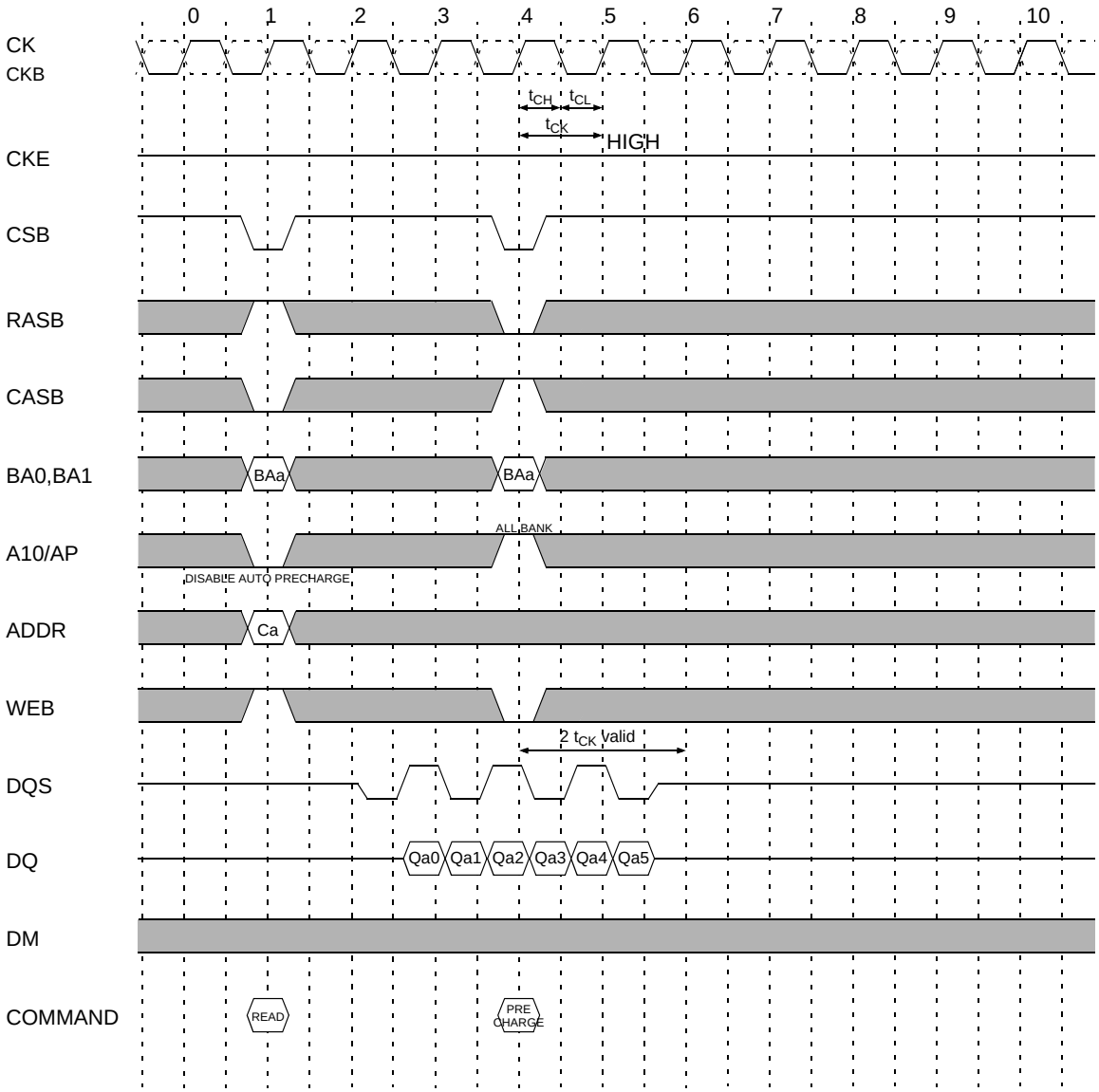
WRITE Interrupted by Precharge & DM (@ BL=8)



WRITE Interrupted by a READ (@ BL=8, CL=2)



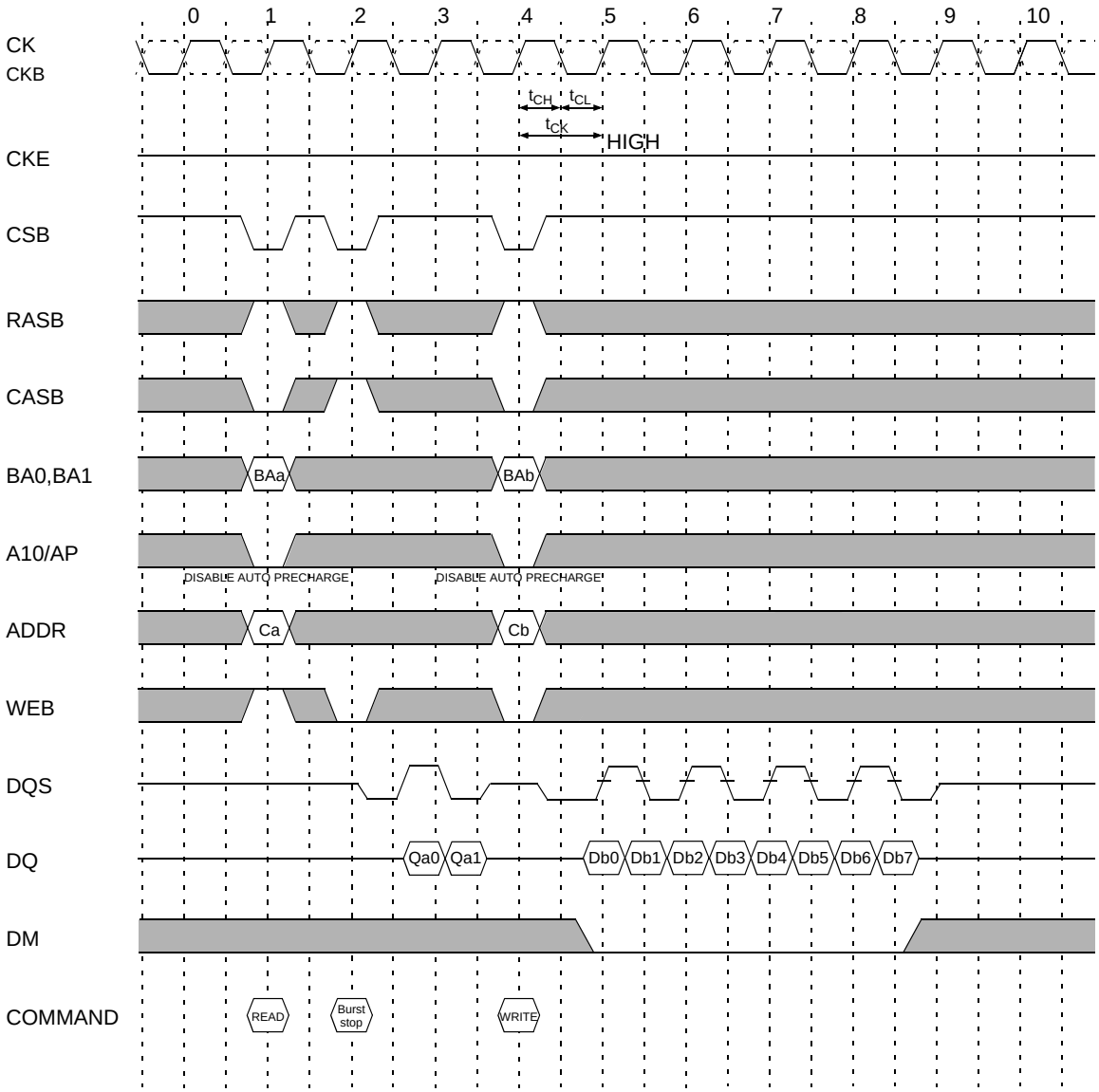
READ Interrupted by Precharge (@ BL=8, CL=2)



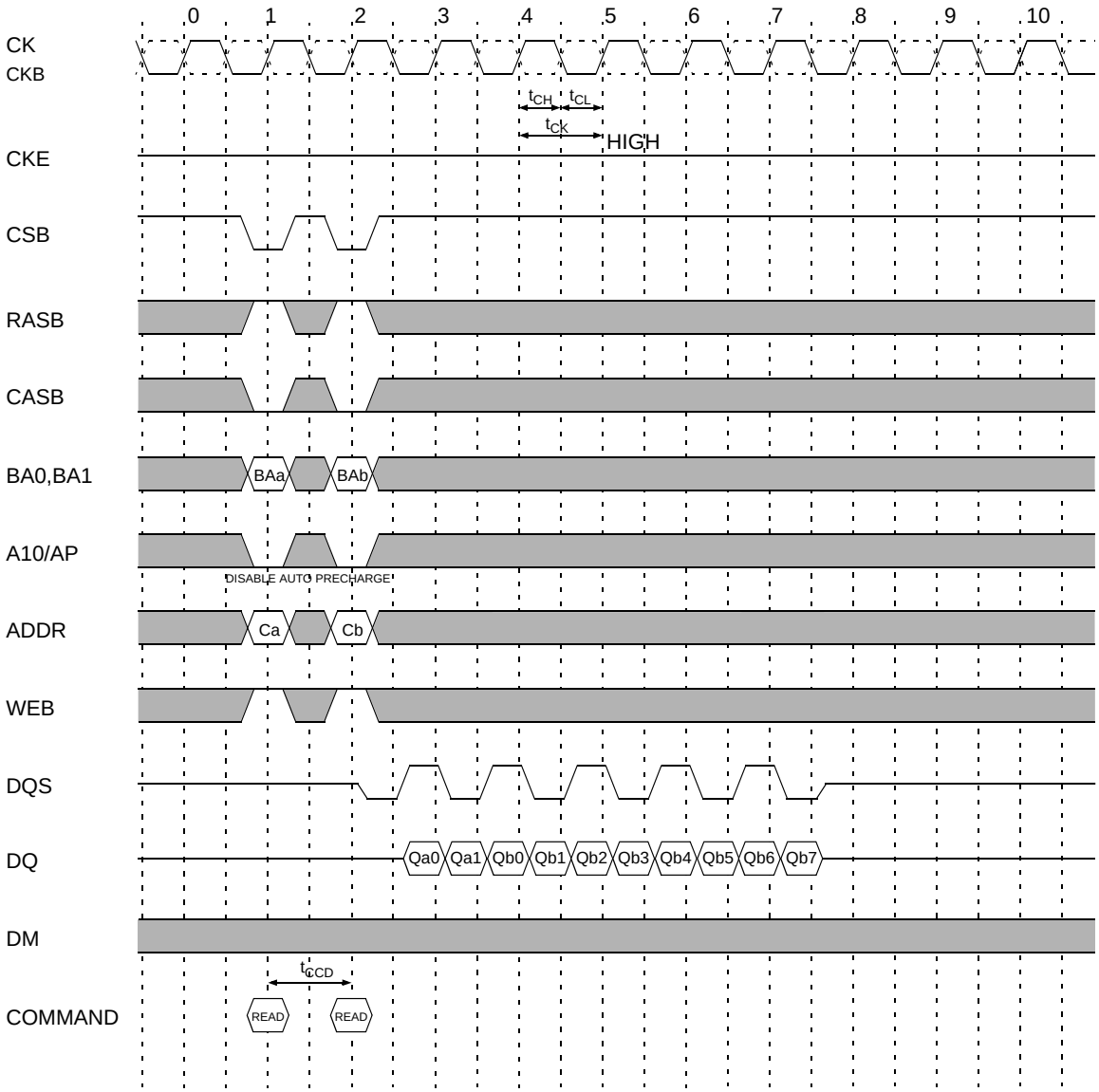
When a burst Read command is issued to a DDR SDRAM, a Prechcrge command may be issued to the same bank before the Read burst is complete. The following functionality determines when a Precharge command may be given during a Read burst and when a new Bank Activate command may be issued to the same bank.

1. For the earliest possible Precharge command without interrupting a Read burst, the Precharge command may be given on the rising clock edge which is CL clock cycles before the end of the Read burst where CL is the CAS Latency. A new Bank Activate command may be issued to the same bank after tRP.
2. When a Precharge command interrupts a Read burst operation, the Precharge command may be given on the rising clock edge which is CL clock cycles before the last data from the interrupted Read burst where CL is the CAS Latency. Once the last data word has been output, the output buffers are tristated. A new Bank Activate command may be issued to the same bank after tRP.

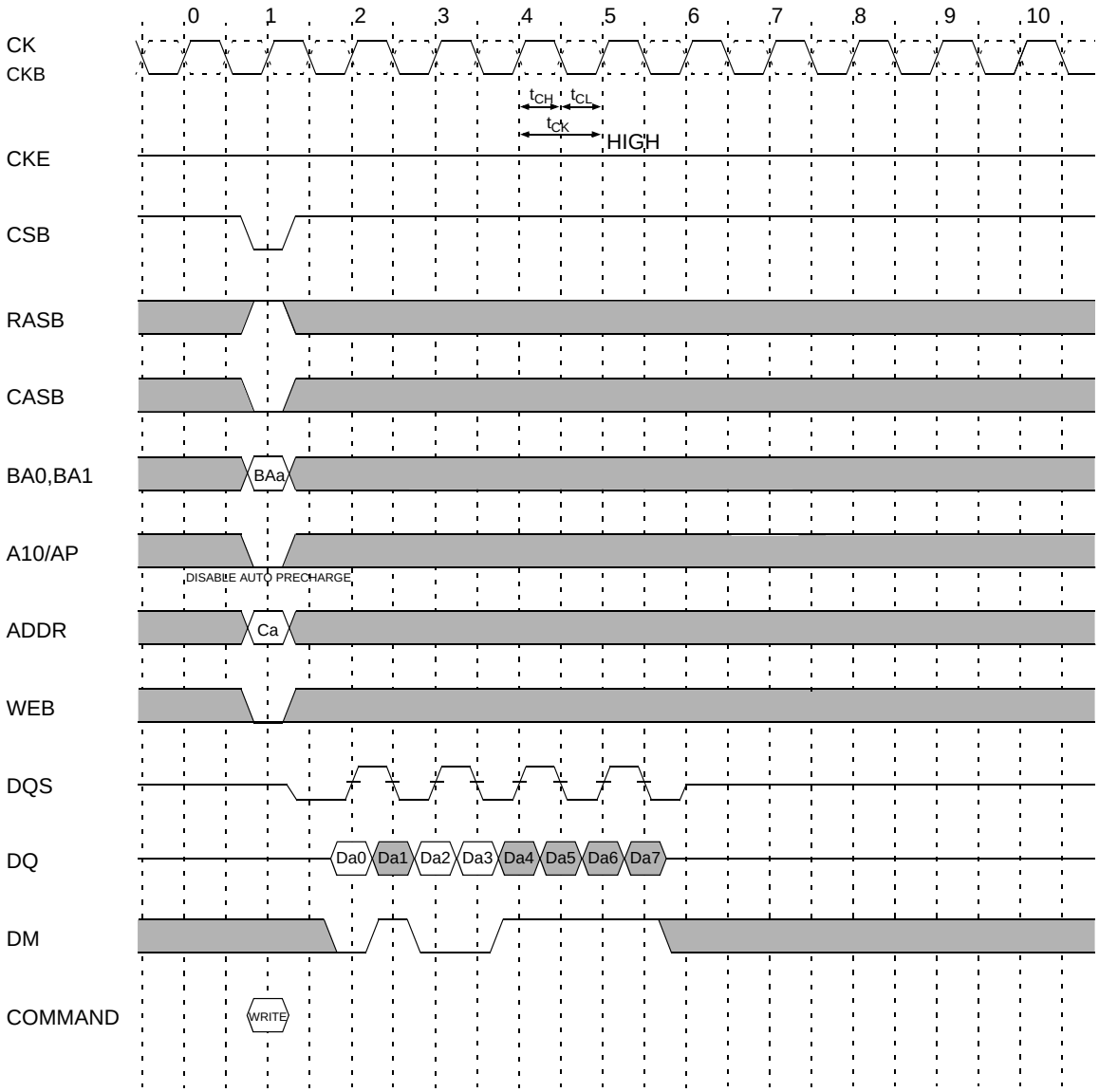
READ Interrupted by a WRITE & Burst Stop (@ BL=8, CL=2)



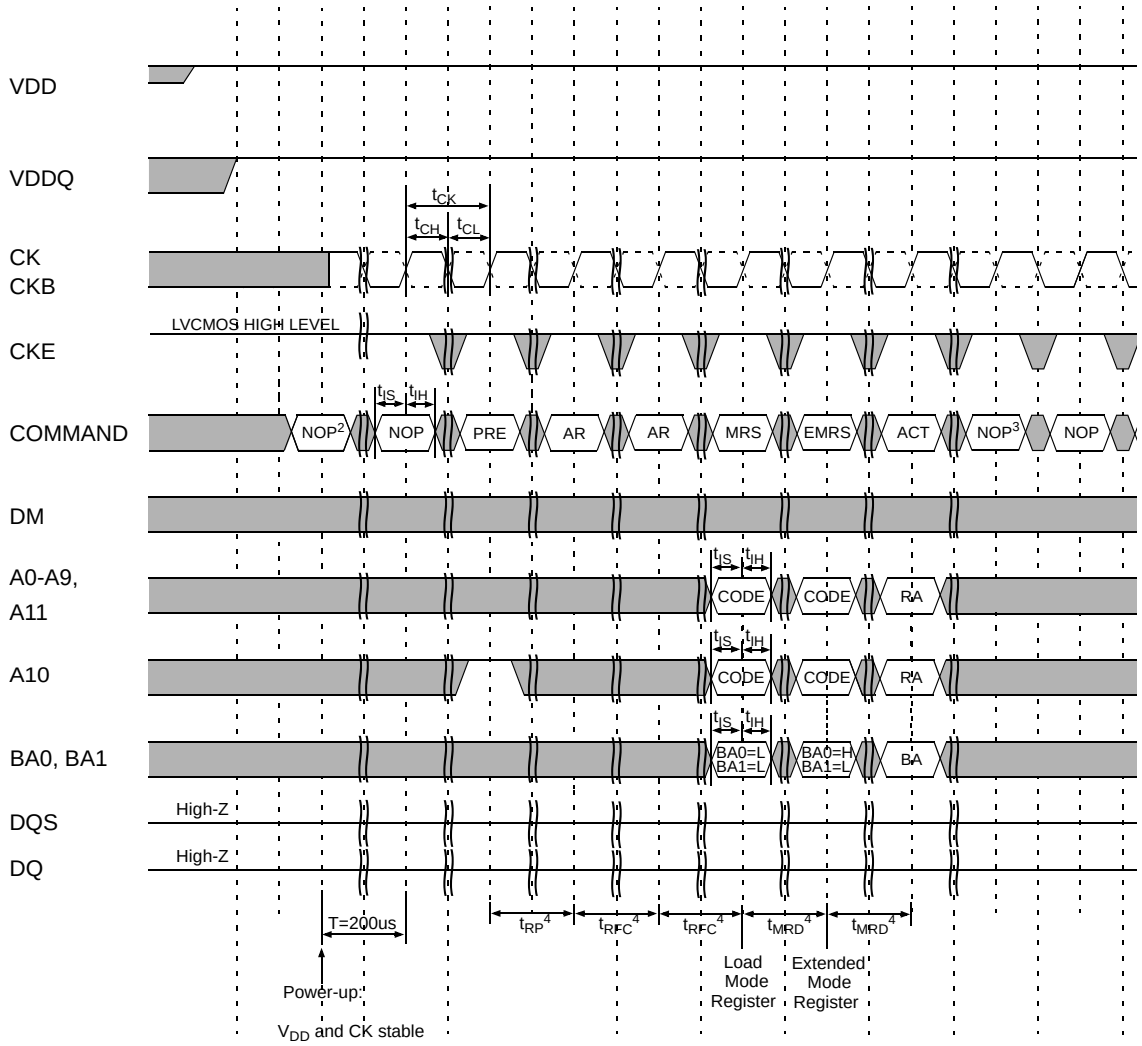
READ Interrupted by READ (@ BL=8, CL=2)



DM Function (@BL=8) only for write

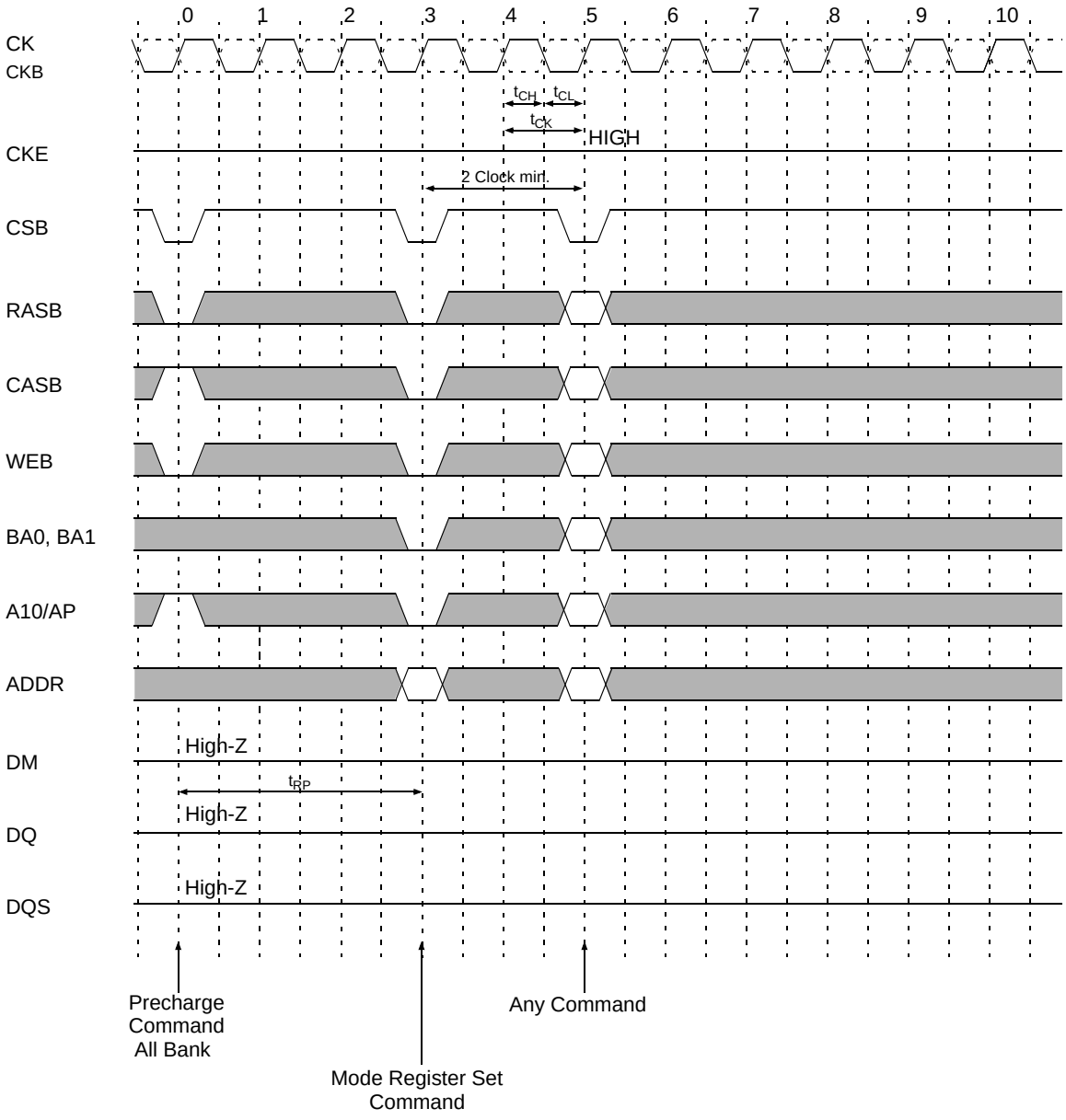


Power up & Initialization Sequence



Notes: 1. PRE = PRECHARGE command, MRS = LOAD MODE REGISTER command, AR = AUTO REFRESH command
ACT = ACTIVE command, RA = Row address, BA = Bank address
2. NOP or DESELECT commands are required for at least 200us.
3. Other valid commands are possible.
4. NOPs or DESELECTs are required during this time.

Mode Register Set



Note 1 Power & Clock must be stable for 200us before precharge all banks

SDRAM FUNCTION GUIDE

EM X XX XX X X X - XX X X X

1. EMLSI Memory
2. Device Type
3. Density
4. Organization
5. Bank
6. Interface (VDD,VDDQ)
7. Version
8. Package
9. Speed
10. Power
11. Temperature

1. Memory Component

2. Device Type
- 8 ---------- Low Power SDRAM
- 9 ---------- SDRAM
- D ---------- Mobile DDR

3. Density
- 32 ---------- 32M
- 64 ---------- 64M
- 28 ---------- 128M
- 56 ---------- 256M
- 12 ---------- 512M
- 1G ---------- 1G

4. Organization
- 04 ---------- x4 bit
- 08 ---------- x8 bit
- 16 ---------- x16 bit
- 32 ---------- x32 bit

5. Bank
- 2 ---------- 2 Bank
- 4 ---------- 4 Bank

6. Interface (VDD,VDDQ)
- V ---------- LVTTL (3.3V,3.3V)
- H---------- LVTTL (3.3V,2.5V)
- K ---------- LVTTL (3.0V,3.0V)
- X ---------- LVTTL (3.0V,2.5V)
- U ---------- P-LVTTL (3.0V,1.8V)
- S ---------- LVCMOS (2.5V,2.5V)
- R ---------- LVCMOS (2.5V,1.8V)
- P ---------- LVCMOS (1.8V,1.8V)

7. Version
- Blank ---------- 1st generation
- A ----------2nd generation
- B ---------- 3rd generation
- C ---------- 4th generation
- D ---------- 5th generation

8. Package
- Blank ---------- KGD
- U ----------44 TSOP2
- P ---------- 48 FpBGA
- Z ---------- 52 FpBGA
- Y ---------- 54 FpBGA
- V ---------- 90 FpBGA

9. Speed
- 60 ---------- 6.0ns (166MHz CL=3)
- 70 ---------- 7.0ns (143MHz CL=3)
- 75 ---------- 7.5ns (133MHz CL=3)
- 7C ---------- 7.5ns (133MHz CL=2)
- 80 ---------- 8.0ns (125MHz CL=3)
- 8C ---------- 8.0ns (125MHz CL=2)
- 90 ---------- 9.0ns (111MHz CL=3)
- 10 ---------- 10.0ns (100MHz CL=3)
- 1C ---------- 10.0ns (100MHz CL=2)
- 12 ---------- 12.0ns (83MHz CL=2)
- 1L ---------- 25.0ns (40MHz CL=1)

10. Power
- U ---------- Low Low Power
- L ---------- Low Power
- S ---------- Standard Power

11. Temperature
- C ---------- Commercial (0'C ~ 70'C)
- E ---------- Extended (-25'C ~ 85'C)
- I ---------- Industrial (-40'C ~ 85'C)