**CY7C026A**

16K x 16 Dual-Port Static RAM

Features

- True dual-ported memory cells that allow simultaneous access of the same memory location
- 16K x 16 organization (CY7C026A)
- 0.35 micron CMOS for optimum speed and power
- High speed access: 15, and 20 ns
- Low operating power
- Active: I_{CC} = 180 mA (typical)
- Standby: I_{SB3} = 0.05 mA (typical)
- Fully asynchronous operation
- Automatic power-down

- Expandable data bus to 32 bits or more using Master/Slave chip select when using more than one device
- On-chip arbitration logic
- Semaphores included to permit software handshaking between ports
- $\overline{INT}$ flags for port-to-port communication
- Separate upper-byte and lower-byte control
- Pin select for Master or Slave
- Commercial and Industrial temperature ranges
- Available in 100-pin thin quad plastic flatpack (TQFP)
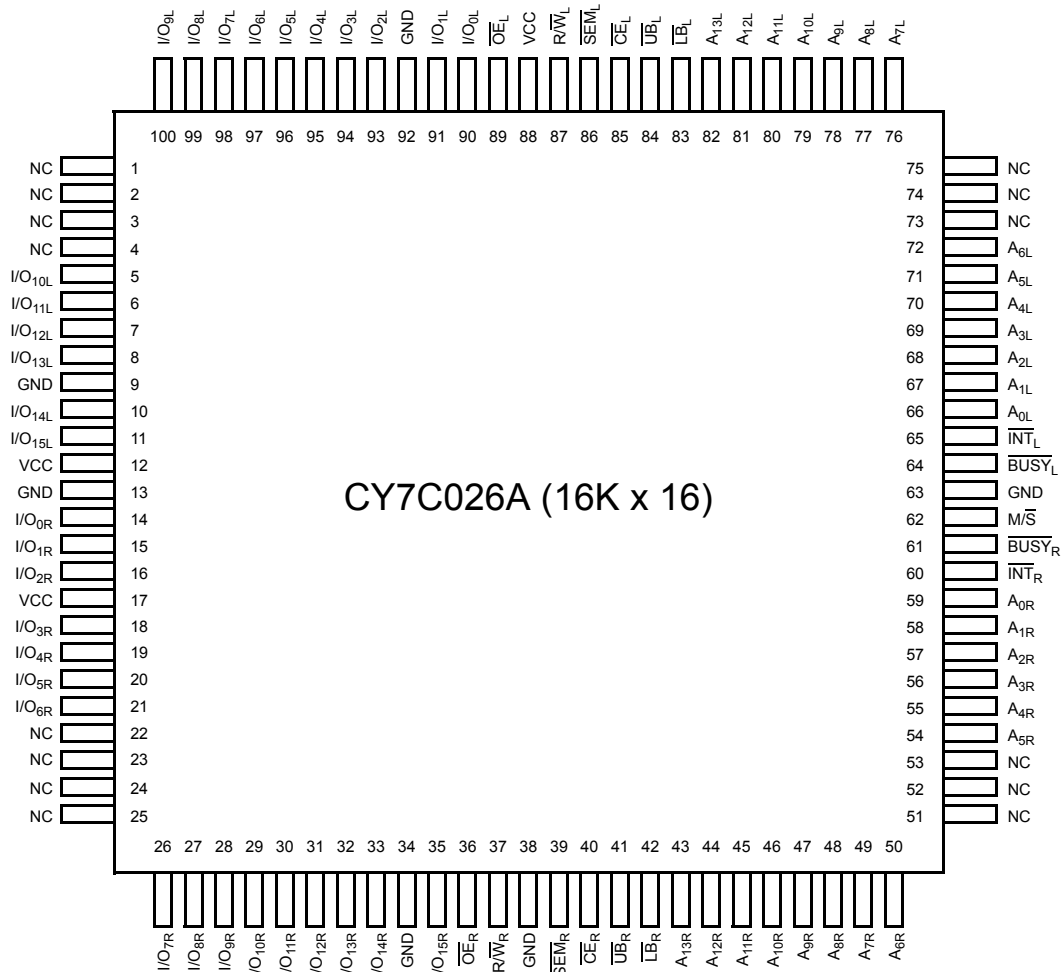- Pb-free packages available

Logic Block Diagram
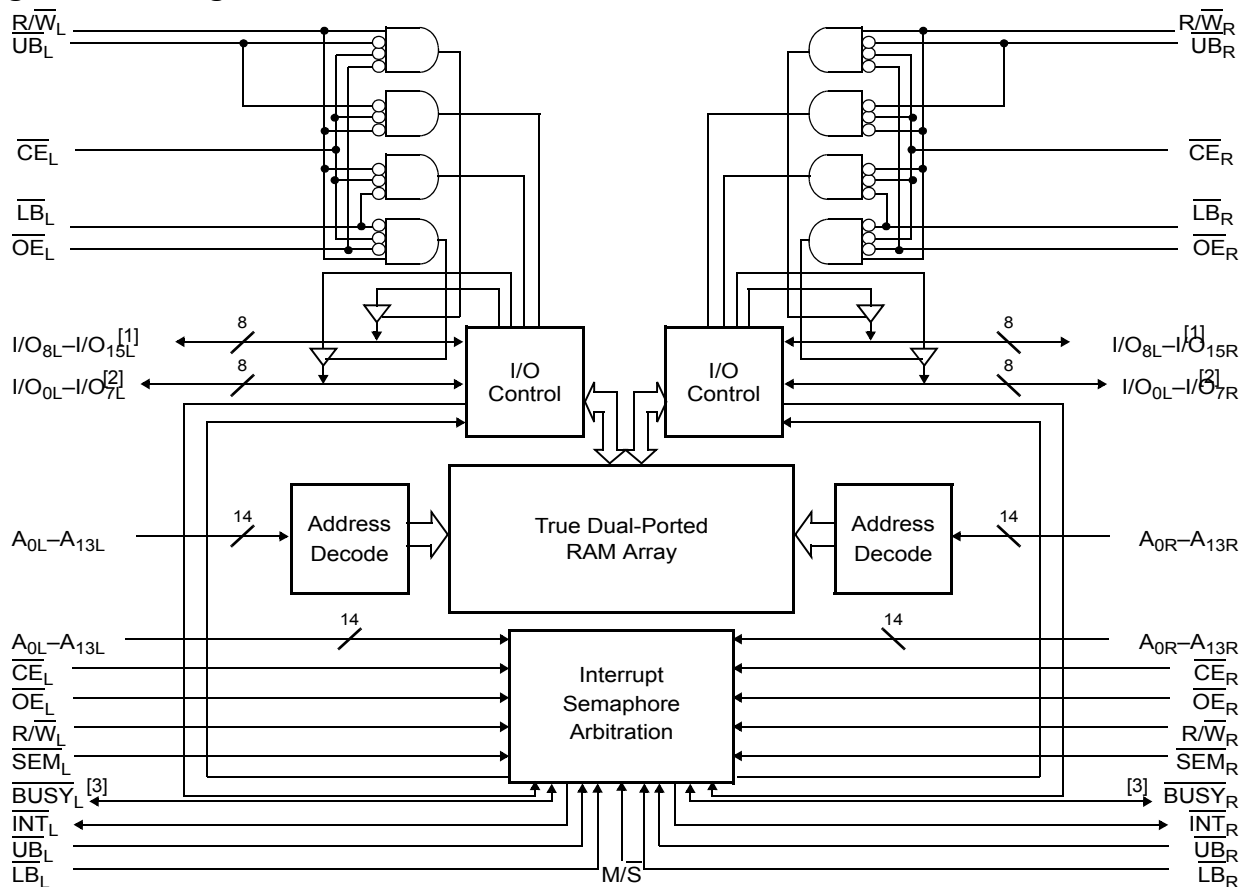
Notes
1. $I/O_8–I/O_{15}$ for x16 devices.
2. $I/O_0–I/O_7$ for x16 devices.
3. $\overline{BUSY}$ is an output in master mode and an input in slave mode.

[+] Feedback

Contents

Pin Configurations

Figure 1. 100-Pin TQFP (Top View)

CY7C026A (16K x 16)

Top pins (100–76): I/O_{9L}, I/O_{8L}, I/O_{7L}, I/O_{6L}, I/O_{5L}, I/O_{4L}, I/O_{3L}, I/O_{2L}, GND, I/O_{1L}, I/O_{0L}, $\overline{OE}_L$, VCC, $R/\overline{W}_L$, $\overline{SEM}_L$, $\overline{CE}_L$, $\overline{UB}_L$, $\overline{LB}_L$, A_{13L}, A_{12L}, A_{11L}, A_{10L}, A_{9L}, A_{8L}, A_{7L}

Left pins (1–25): NC, NC, NC, NC, I/O_{10L}, I/O_{11L}, I/O_{12L}, I/O_{13L}, GND, I/O_{14L}, I/O_{15L}, VCC, GND, I/O_{0R}, I/O_{1R}, I/O_{2R}, VCC, I/O_{3R}, I/O_{4R}, I/O_{5R}, I/O_{6R}, NC, NC, NC, NC

Right pins (75–51): NC, NC, NC, A_{6L}, A_{5L}, A_{4L}, A_{3L}, A_{2L}, A_{1L}, A_{0L}, $\overline{INT}_L$, $\overline{BUSY}_L$, GND, $M/\overline{S}$, $\overline{BUSY}_R$, $\overline{INT}_R$, A_{0R}, A_{1R}, A_{2R}, A_{3R}, A_{4R}, A_{5R}, NC, NC, NC

Bottom pins (26–50): I/O_{7R}, I/O_{8R}, I/O_{9R}, I/O_{10R}, I/O_{11R}, I/O_{12R}, I/O_{13R}, I/O_{14R}, GND, I/O_{15R}, $\overline{OE}_R$, $R/\overline{W}_R$, GND, $\overline{SEM}_R$, $\overline{CE}_R$, $\overline{UB}_R$, $\overline{LB}_R$, A_{13R}, A_{12R}, A_{11R}, A_{10R}, A_{9R}, A_{8R}, A_{7R}, A_{6R}

Selection Guide

Parameter	CY7C026A -15	CY7C026A -20	Unit
Maximum access time	15	20	ns
Typical operating current	190	180	mA
Typical standby current for I_{SB1} (Both ports TTL level)	50	45	mA
Typical standby current for I_{SB3} (Both ports CMOS level)	0.05	0.05	mA

Pin Definitions

Left Port	Right Port	Description
CE_L	CE_R	Chip enable
R/W_L	R/W_R	Read/Write enable
$\overline{OE}_L$	$\overline{OE}_R$	Output enable
A_{0L}–A_{13L}	A_{0R}–A_{13R}	Address
I/O_{0L}–I/O_{15L}	I/O_{0R}–I/O_{15R}	Data bus input/output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore enable
$\overline{UB}_L$	$\overline{UB}_R$	Upper byte select (I/O_8–I/O_{15} for x16 devices)
$\overline{LB}_L$	$\overline{LB}_R$	Lower byte select (I/O_0–I/O_7 for x16 devices)
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy flag
M/S		Master or slave select
V_{CC}		Power
GND		Ground
NC		No connect

Architecture

The CY7C026A consist of an array of 16K words of 16 bits each of dual-port RAM cells, I/O and address lines, and control signals ($\overline{CE}$, $\overline{OE}$, R/W). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a BUSY pin is provided on each port. Two Interrupt (INT) pins can be utilized for port-to-port communication. Two Semaphore (SEM) control pins are used for allocating shared resources. With the M/S pin, the devices can function as a master (BUSY pins are outputs) or as a slave (BUSY pins are inputs). The devices also have an automatic power down feature controlled by $\overline{CE}$. Each port is provided with its own Output Enable control ($\overline{OE}$), which allows data to be read from the device.

Functional Description

The CY7C026A is a low power CMOS 16K x 16 dual-port static RAM. Various arbitration schemes are included on the devices to handle situations when multiple processors access the same piece of data. Two ports are provided, permitting independent, asynchronous access for reads and writes to any location in memory. The device can be utilized as standalone 16-bit dual-port static RAM or multiple devices can be combined to function as a 32-bit or wider master/slave dual-port static RAM. An M/S pin is provided for implementing 32-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: Chip Enable ($\overline{CE}$), Read or Write Enable (R/$\overline{W}$), and Output Enable ($\overline{OE}$). Two flags are provided on each port (BUSY and INT). BUSY signals that the port is trying to access the same location currently being accessed by the other port. The Interrupt flag ($\overline{INT}$) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power down feature is controlled independently on each port by the chip enable pin.

The CY7C026A is available in 100-pin thin quad plastic flatpack (TQFP) packages.

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/$\overline{W}$ to either the R/$\overline{W}$ pin (see Figure 6) or the $\overline{CE}$ pin (see Figure 7). Required inputs for non-contention operations are summarized in Table 1.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must occur before the data is read on the output; otherwise the data read is not deterministic. Data is valid on the port t_{DDD} after the data is presented on the other port.

Read Operation

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$ pins. Data is available t_{ACE} after $\overline{CE}$ or t_{DOE} after $\overline{OE}$ is asserted. If the user wishes to access a semaphore flag, then the $\overline{SEM}$ pin must be asserted instead of the $\overline{CE}$ pin, and $\overline{OE}$ must also be asserted.

Interrupts

The upper two memory locations may be used for message passing. The highest memory location (3FFF) is the mailbox for the right port and the second highest memory location (3FFE) is the mailbox for the left port. When one port writes to the other port's mailbox, an interrupt is generated to the owner. The interrupt is reset when the owner reads the contents of the mailbox. The message is user defined.

Each port can read the other port's mailbox without resetting the interrupt. The active state of the busy signal (to a port) prevents

the port from setting the interrupt to the winning port. Also, an active busy to a port prevents that port from reading its own mailbox and, thus, resetting the interrupt to it.

If an application does not require message passing, do not connect the interrupt pin to the processor's interrupt request input pin.

The operation of the interrupts and their interaction with Busy are summarized in Table 2.

Busy

The CY7C026A provides on-chip arbitration to resolve simultaneous memory location access (contention). If both ports' CEs are asserted and an address match occurs within t_{PS} of each other, the busy logic determines which port has access. If t_{PS} is violated, one port definitely gains permission to the location, but it is not predictable which port gets that permission. BUSY is asserted t_{BLA} after an address match or t_{BLC} after CE is taken LOW.

Master/Slave

A M/S pin is provided to expand the word width by configuring the device as either a master or a slave. The BUSY output of the master is connected to the BUSY input of the slave. This allows the device to interface to a master device with no external components. Writing to slave devices must be delayed until after the BUSY input has settled (t_{BLC} or t_{BLA}), otherwise, the slave chip may begin a write cycle during a contention situation. When tied HIGH, the M/S pin allows the device to be used as a master and, therefore, the BUSY line is an output. BUSY can then be used to send the arbitration outcome to a slave.

Semaphore Operation

The CY7C026A provides eight semaphore latches, which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it

sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, SEM or OE must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value is available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a zero), it assumes control of the shared resource, otherwise (reads a one) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side succeeds in gaining control of the semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting SEM LOW. The SEM pin functions as a chip select for the semaphore latches (CE must remain HIGH during SEM LOW). A_{0-2} represents the semaphore address. OE and R/W are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a zero is written to the left port of an available semaphore, a one appears at the same semaphore address on the right port. That semaphore can now only be modified by the side showing zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore is set to one for both sides. However, if the right port had requested the semaphore (written a zero) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. Table 3 shows sample semaphore operations.

When reading a semaphore, all sixteen/eighteen data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore is definitely obtained by one side or the other, but there is no guarantee which side controls the semaphore.

Maximum Ratings[4]

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ....–65 °C to +150 °C

Ambient temperature with
power applied ....–55 °C to +125 °C

Supply voltage to ground potential ....–0.3 V to +7.0 V

DC voltage applied to outputs
in High Z state ....–0.5 V to +7.0 V

DC input voltage[5] ....–0.5 V to + 7.0 V

Output current into outputs (LOW) .... 20 mA

Static discharge voltage.. >2001 V

Latch-up current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	5V $\pm$ 10%
Industrial	–40 °C to +85 °C	5V $\pm$ 10%

Electrical Characteristics Over the Operating Range

Parameter	Description		CY7C026A						Unit
			-15			**-20**			
			Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH voltage (V_{CC} = Min., I_{OH} = –4.0 mA)		2.4		–	2.4		–	V
V_{OL}	Output LOW voltage (V_{CC} = Min., I_{OH} = +4.0 mA)		–		0.4	–		0.4	V
V_{IH}	Input HIGH voltage		2.2		–	2.2		–	V
V_{IL}	Input LOW voltage				0.8			0.8	V
I_{OZ}	Output leakage current		–10		10	–10		10	μA
I_{CC}	Operating current (V_{CC} = Max, I_{OUT} = 0 mA) outputs disabled	Com'l.		190	285	–	180	275	mA
		Indust.		215	305		–		mA
I_{SB1}	Standby current (Both ports TTL level) $\overline{CE}_L$ & $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}	Com'l.		50	70		45	65	mA
		Indust.		65	95		–		mA
I_{SB2}	Standby current (One port TTL level) $\overline{CE}_L$ | $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}	Com'l.		120	180		110	160	mA
		Indust.		135	205		–		mA
I_{SB3}	Standby current (Both port CMOS level) $\overline{CE}_L$ & $\overline{CE}_R \geq V_{CC}$–0.2V, f = 0	Com'l.		0.05	0.5		0.05	0.5	mA
		Indust.		0.05	0.5		–		mA
I_{SB4}	Standby current (One port CMOS level) $\overline{CE}_L$ | $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}[6]	Com'l.		110	160		100	140	mA
		Indust.		125	175		–		mA

Capacitance[7]

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	10	pF
C_{OUT}	Output capacitance		10	pF

Notes
4. The voltage on any input or I/O pin cannot exceed the power pin during power up.
5. Pulse width < 20 ns.
6. f_{MAX} = $1/t_{RC}$ = All inputs cycling at f = $1/t_{RC}$ (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.
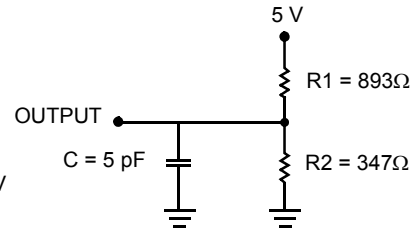7. Tested initially and after any design or process changes that may affect these parameters.

Figure 2. AC Test Loads and Waveforms
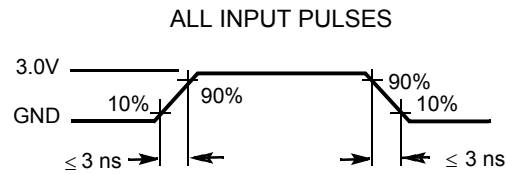
(a) Normal Load (Load 1)

5V

R1 = 893Ω

OUTPUT

C = 30 pF

R2 = 347 Ω
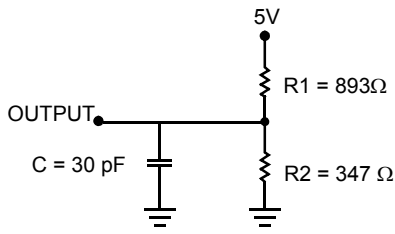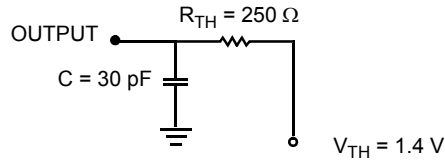
(b) Thévenin Equivalent (Load 1)

OUTPUT

R_{TH} = 250 Ω

C = 30 pF

V_{TH} = 1.4 V

(c) Three-State Delay (Load 2)
(Used for t_{LZ}, t_{HZ}, t_{HZWE}, & t_{LZWE}
including scope and jig)

5 V

R1 = 893Ω

OUTPUT

C = 5 pF

R2 = 347Ω

ALL INPUT PULSES

3.0V

GND

10%

90%

90%

10%

$\leq$ 3 ns

$\leq$ 3 ns

Capacitance (pF)

Δ (ns) for all -12 access times

Load Derating Curve

Switching Characteristics Over the Operating Range[8]

Parameter	Description	CY7C026A -15 Min	CY7C026A -15 Max	CY7C026A -20 Min	CY7C026A -20 Max	Unit
READ CYCLE						
t_{RC}	Read cycle time	15	–	20	–	ns
t_{AA}	Address to data valid	–	15	–	20	ns
t_{OHA}	Output hold from address change	3	–	3	–	ns
t_{ACE}[9]	$\overline{CE}$ LOW to data valid	–	15	–	20	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	10	–	12	ns
t_{LZOE}[10, 11, 12]	$\overline{OE}$ LOW to Low Z	3	–	3	–	ns
t_{HZOE}[10, 11, 12]	$\overline{OE}$ HIGH to High Z	–	10	–	12	ns
t_{LZCE}[10, 11, 12]	$\overline{CE}$ LOW to Low Z	3	–	3	–	ns
t_{HZCE}[10, 11, 12]	$\overline{CE}$ HIGH to High Z	–	10	–	12	ns
t_{PU}[12]	$\overline{CE}$ LOW to Power-up	0	–	0	–	ns
t_{PD}[12]	$\overline{CE}$ HIGH to Power-down	–	15	–	20	ns
t_{ABE}[9]	Byte enable access time	–	15	–	20	ns
WRITE CYCLE						
t_{WC}	Write cycle time	15	–	20	–	ns
t_{SCE}[9]	$\overline{CE}$ LOW to write end	12	–	15	–	ns
t_{AW}	Address valid to write end	12	–	15	–	ns
t_{HA}	Address hold From write end	0	–	0	–	ns
t_{SA}[9]	Address setup to write start	0	–	0	–	ns
t_{PWE}	Write pulse width	12	–	15	–	ns
t_{SD}	Data setup to write end	10	–	15	–	ns
t_{HD}[14]	Data hold from write end	0	–	0	–	ns
t_{HZWE}[11, 12]	R/$\overline{W}$ LOW to High Z	–	10	–	12	ns
t_{LZWE}[11, 12]	R/$\overline{W}$ HIGH to Low Z	3	–	3	–	ns
t_{WDD}[13]	Write pulse to data delay	–	30	–	45	ns
t_{DDD}[13]	Write data valid to read data valid	–	25	–	30	ns

Notes
8. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OI}/I_{OH} and 30 pF load capacitance.
9. To access RAM, $\overline{CE}$ = L, $\overline{UB}$ = L, $\overline{SEM}$ = H. To access semaphore, $\overline{CE}$ = H and $\overline{SEM}$ = L. Either condition must be valid for the entire t_{SCE} time.
10. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
11. Test conditions used are Load 2.
12. This parameter is guaranteed but not tested.
13. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Figure 10.
14. For 15 ns industrial parts t_{HD} minimum is 0.5 ns.

[+] Feedback

Switching Characteristics Over the Operating Range[8] (continued)

Parameter	Description	CY7C026A -15 Min	CY7C026A -15 Max	CY7C026A -20 Min	CY7C026A -20 Max	Unit
BUSY TIMING[15]						
t_{BLA}	BUSY LOW from address match	–	15	–	20	ns
t_{BHA}	BUSY HIGH from address mismatch	–	15	–	20	ns
t_{BLC}	BUSY LOW from CE LOW	–	15		20	ns
t_{BHC}	BUSY HIGH from CE HIGH	–	15	–	17	ns
t_{PS}	Port setup for priority	5	–	5	–	ns
t_{WB}	R/W HIGH after BUSY (Slave)	0	–	0	–	ns
t_{WH}	R/W HIGH after BUSY HIGH (Slave)	13	–	15	–	ns
t_{BDD}[16]	BUSY HIGH to data valid	–	15	–	20	ns
INTERRUPT TIMING[15]						
t_{INS}	INT set time	–	15	–	20	ns
t_{INR}	INT reset time	–	15	–	20	ns
SEMAPHORE TIMING						
t_{SOP}	SEM flag update pulse (OE or SEM)	10	–	10	–	ns
t_{SWRD}	SEM flag write to read time	5	–	5	–	ns
t_{SPS}	SEM flag contention window	5	–	5	–	ns
t_{SAA}	SEM address access time	–	15	–	20	ns

Data Retention Mode

The CY7C026A is designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules ensure data retention:

1. Chip Enable (CE) must be held HIGH during data retention, within V_{CC} to $V_{CC} – 0.2$ V.
2. CE must be kept between $V_{CC} – 0.2$ V and 70% of V_{CC} during the power up and power down transitions.
3. The RAM can begin operation $> t_{RC}$ after V_{CC} reaches the minimum operating voltage (4.5 V).

Timing
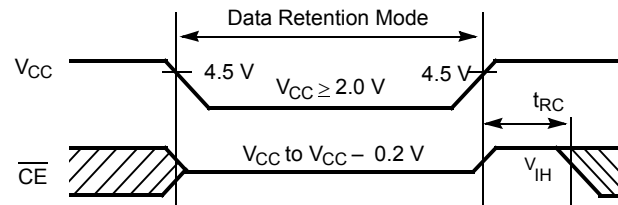
Parameter	Test Conditions[17]	Max	Unit
ICC_{DR1}	At $VCC_{DR} = 2$ V	1.5	mA

Notes
15. Test conditions used are Load 2.
16. t_{BDD} is a calculated parameter and is the greater of $t_{WDD}–t_{PWE}$ (actual) or $t_{DDD}–t_{SD}$ (actual).
17. CE = V_{CC}, V_{in} = GND to V_{CC}, T_A = 25 °C. This parameter is guaranteed but not tested.

Switching Waveforms

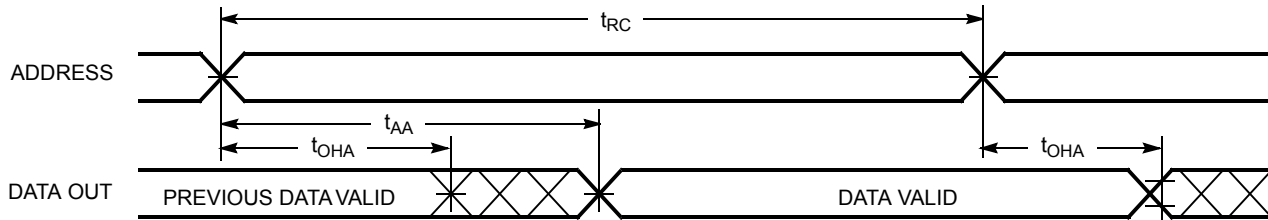**Figure 3. Read Cycle No.1 (Either Port Address Access)**[18, 19, 20]

Figure 4. Read Cycle No.2 (Either Port $\overline{CE}/\overline{OE}$ Access)[18, 21, 22]

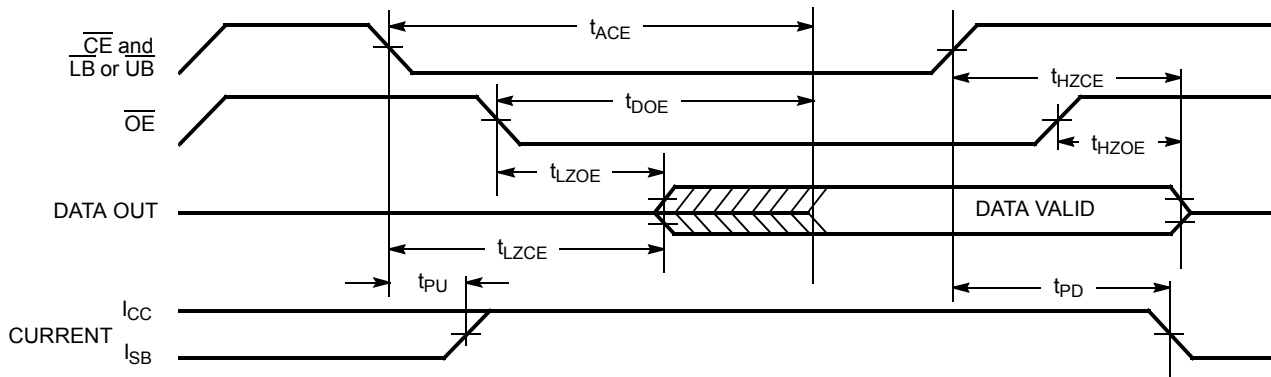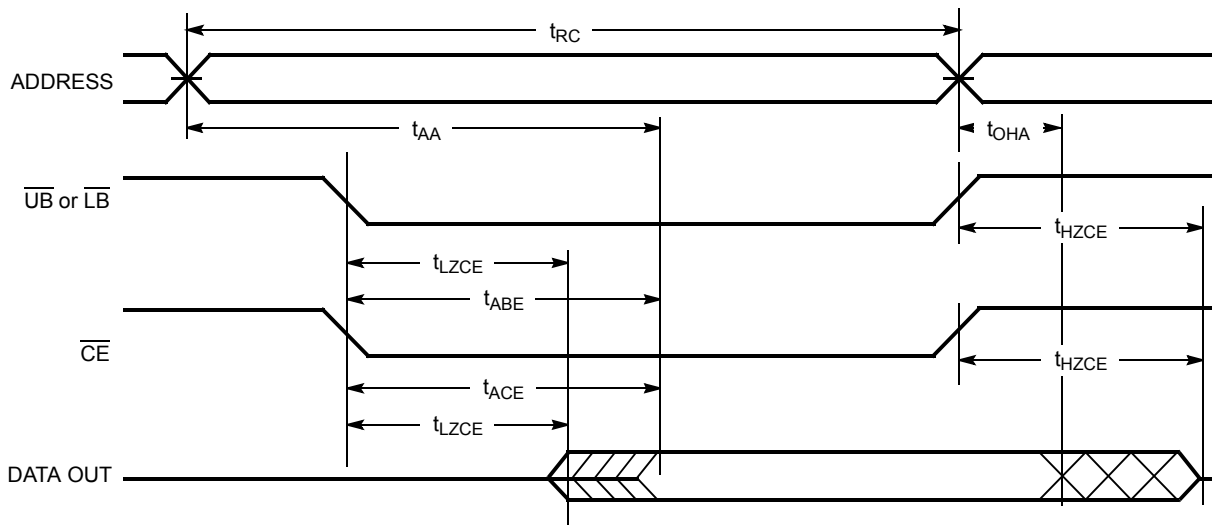**Figure 5. Read Cycle No. 3 (Either Port)**[18, 20, 21, 22]

Notes
18. R/$\overline{W}$ is HIGH for read cycles.
19. Device is continuously selected $\overline{CE}$ = V_{IL} and $\overline{UB}$ or $\overline{LB}$ = V_{IL}. This waveform cannot be used for semaphore reads.
20. $\overline{OE}$ = V_{IL}.
21. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
22. To access RAM, $\overline{CE}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH}, $\overline{SEM}$ = V_{IL}.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1: R/W Controlled Timing[23, 24, 25, 26]
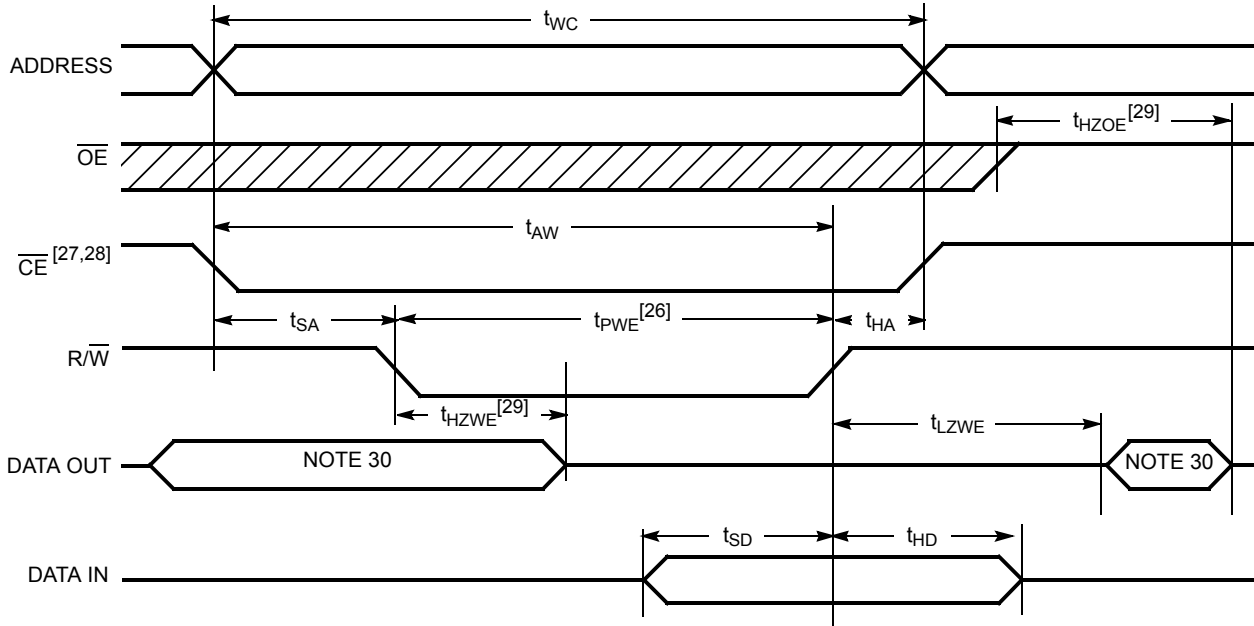
Figure 7. Write Cycle No. 2: $\overline{CE}$ Controlled Timing[23, 24, 25, 31]
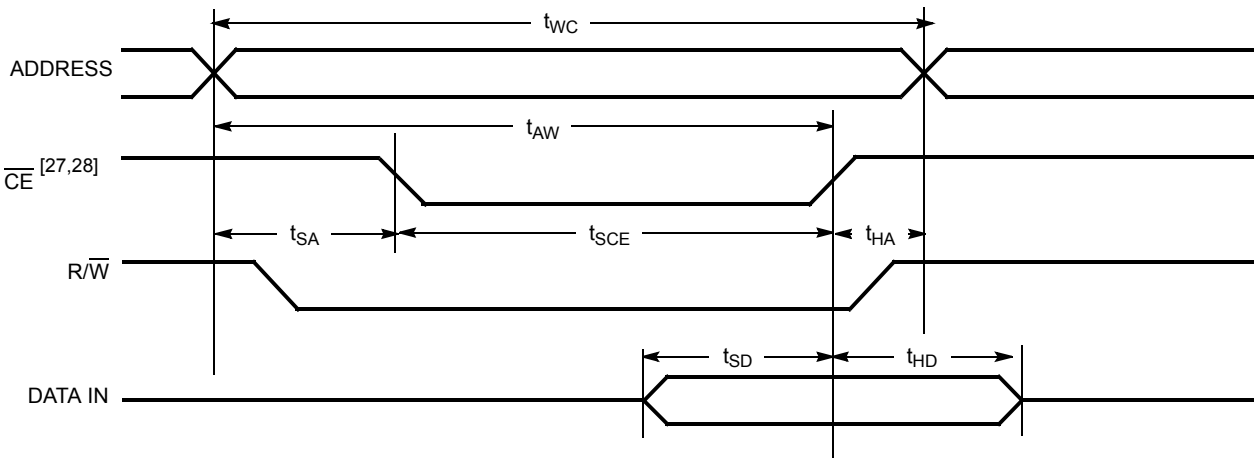
Notes
23. R/$\overline{W}$ must be HIGH during all address transitions.
24. A write occurs during the overlap (t_{SCE} or t_{PWE}) of a LOW $\overline{CE}$ or $\overline{SEM}$ and a LOW $\overline{UB}$ or $\overline{LB}$.
25. t_{HA} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ or ($\overline{SEM}$ or R/$\overline{W}$) going HIGH at the end of write cycle.
26. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or ($t_{HZWE} + t_{SD}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
27. To access RAM, $\overline{CE}$ = V_{IL}, $\overline{SEM}$ = V_{IH}.
28. To access upper byte, $\overline{CE}$ = V_{IL}, $\overline{UB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}.
    To access lower byte, $\overline{CE}$ = V_{IL}, $\overline{LB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}.
29. Transition is measured ±500 mV from steady state with a 5 pF load (including scope and jig). This parameter is sampled and not 100% tested.
30. During this period, the I/O pins are in the output state, and input signals must not be applied.
31. If the $\overline{CE}$ or $\overline{SEM}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high impedance state.

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[+] Feedback

Switching Waveforms (continued)

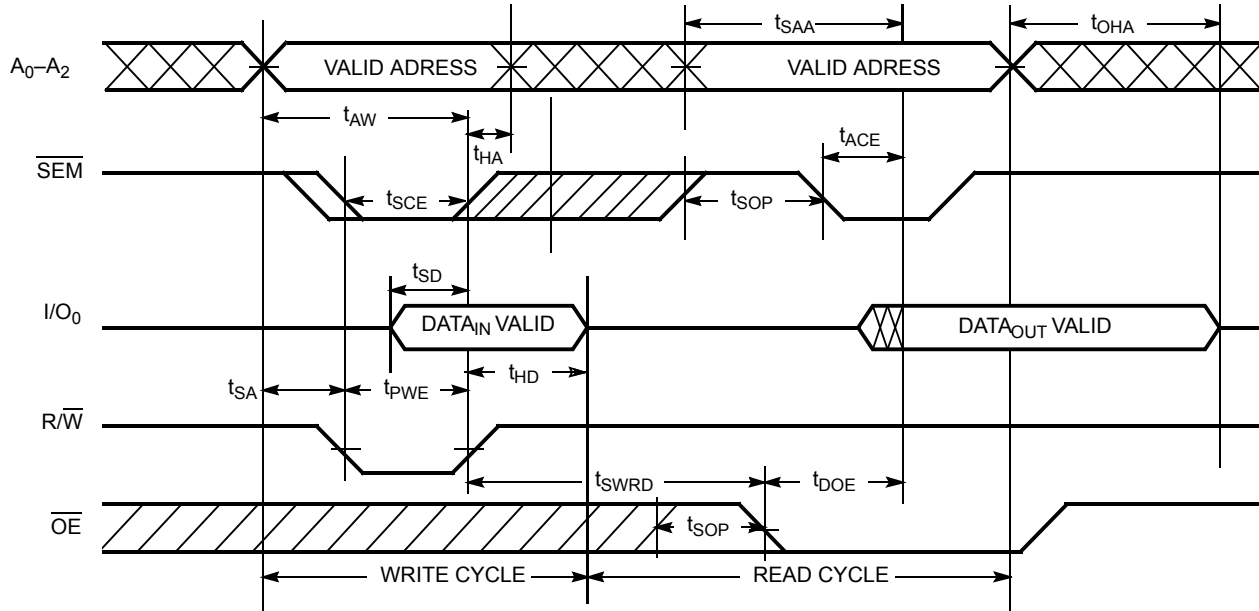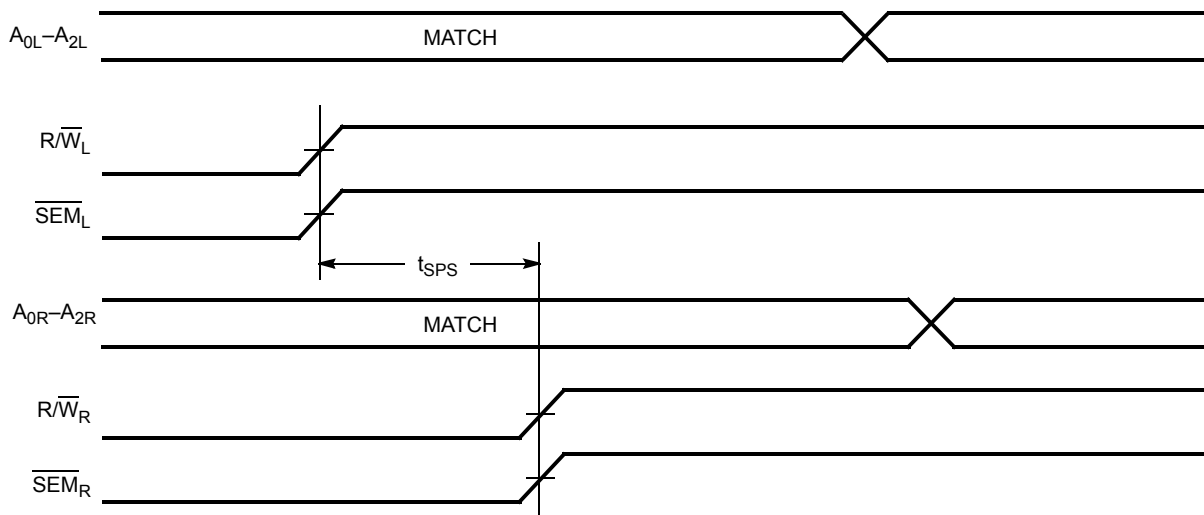**Figure 8. Semaphore Read After Write Timing, Either Side[32]**

Figure 9. Timing Diagram of Semaphore Contention[33, 34, 35]

Notes
32. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).
33. I/O_{0R} = I/O_{0L} = LOW (request semaphore); $\overline{CE}_R$ = $\overline{CE}_L$ = HIGH.
34. Semaphores are reset (available to both ports) at cycle start.
35. If t_{SPS} is violated, the semaphore is definitely obtained by one side or the other, but which side gets the semaphore is unpredictable.

Switching Waveforms (continued)

Figure 10. Timing Diagram of Read with $\overline{\text{BUSY}}$ (M/$\overline{\text{S}}$ = HIGH)[36]
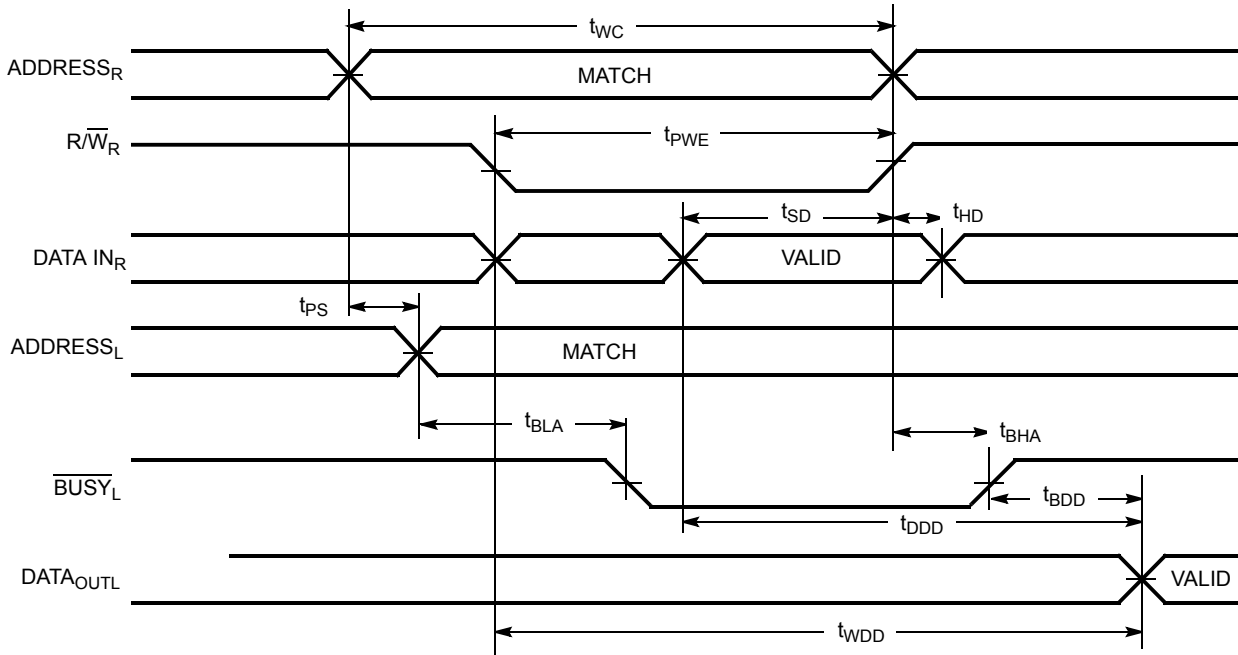
Figure 11. Write Timing with Busy Input (M/$\overline{\text{S}}$ = LOW)
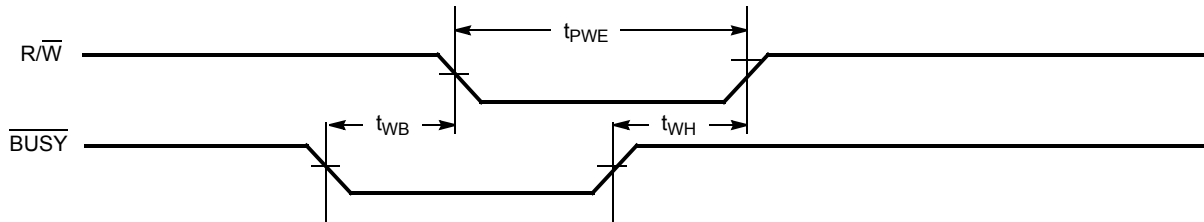
Note
36. $\overline{\text{CE}}_L = \overline{\text{CE}}_R$ = LOW.

Switching Waveforms (continued)

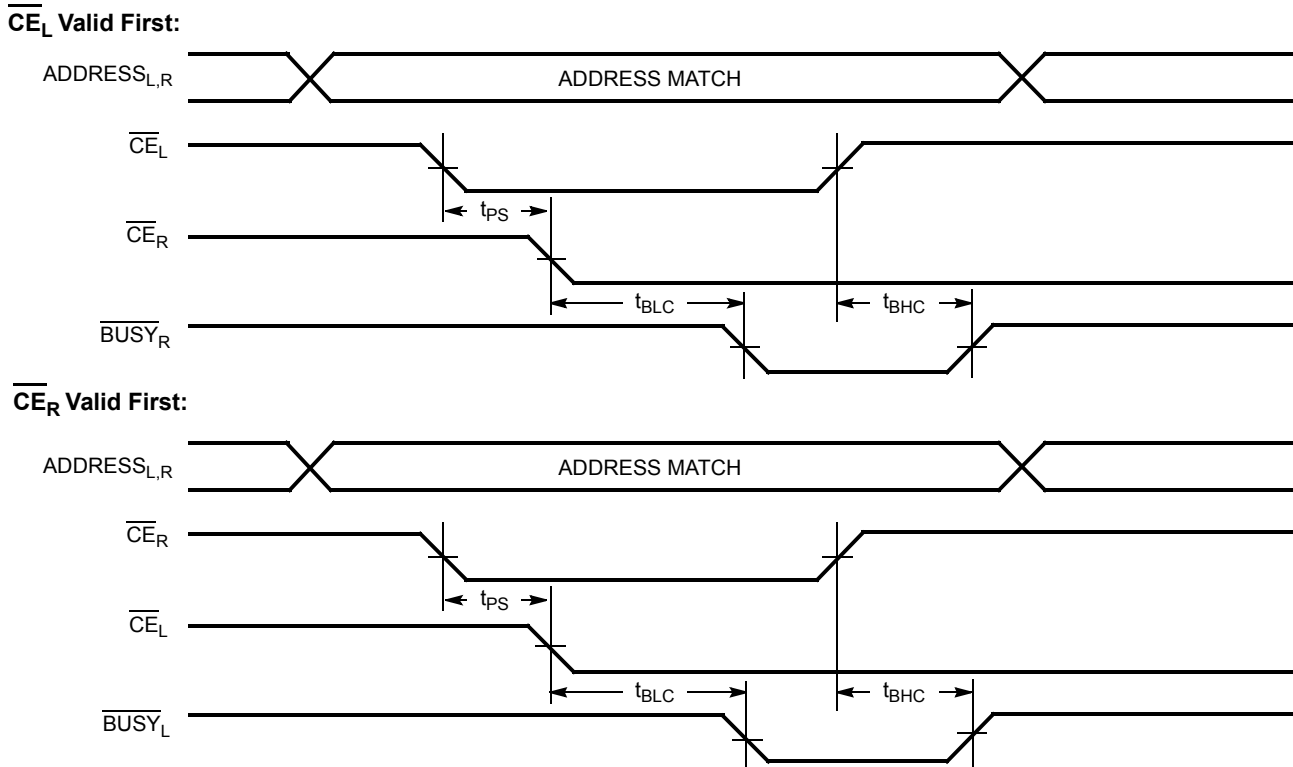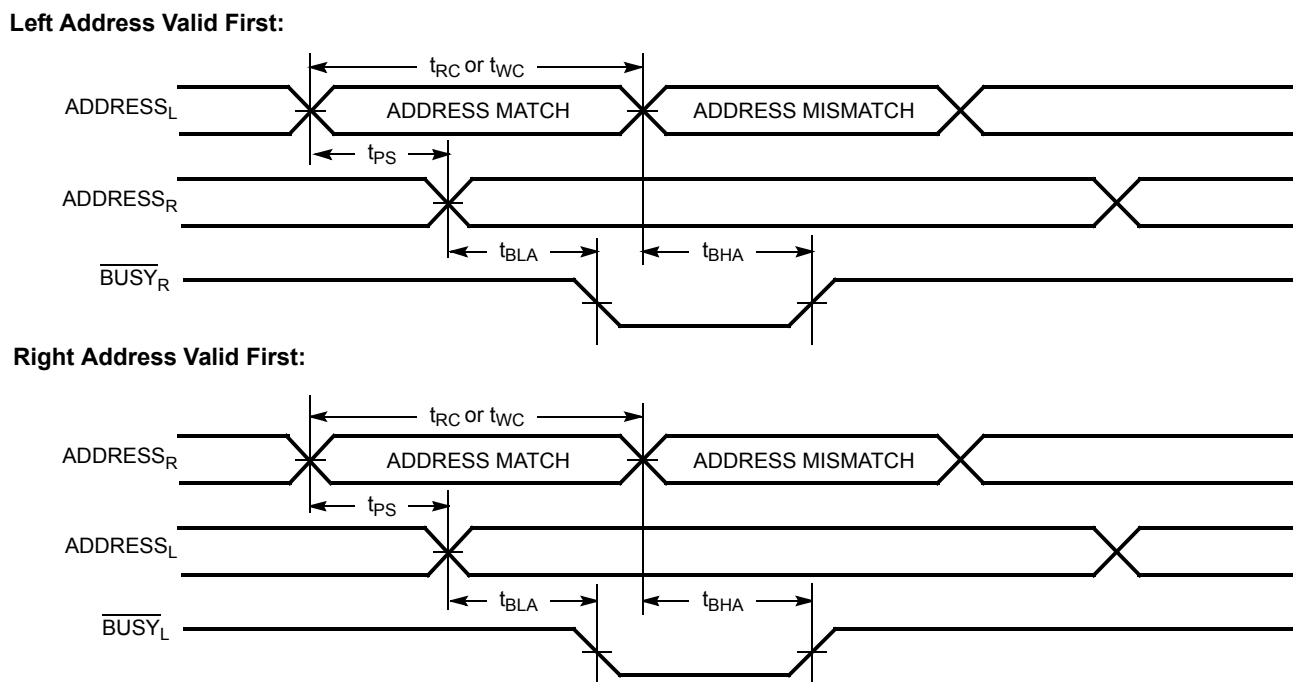### Figure 12. Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)[37]

$\overline{CE}_L$ Valid First:

ADDRESS$_{L,R}$ — ADDRESS MATCH

$\overline{CE}_L$

t_{PS}

$\overline{CE}_R$

t_{BLC} t_{BHC}

$\overline{BUSY}_R$

$\overline{CE}_R$ Valid First:

ADDRESS$_{L,R}$ — ADDRESS MATCH

$\overline{CE}_R$

t_{PS}

$\overline{CE}_L$

t_{BLC} t_{BHC}

$\overline{BUSY}_L$

Figure 13. Busy Timing Diagram No. 2 (Address Arbitration)[37]

Left Address Valid First:

t_{RC} or t_{WC}

ADDRESS$_L$ — ADDRESS MATCH — ADDRESS MISMATCH

t_{PS}

ADDRESS$_R$

t_{BLA} t_{BHA}

$\overline{BUSY}_R$

Right Address Valid First:

t_{RC} or t_{WC}

ADDRESS$_R$ — ADDRESS MATCH — ADDRESS MISMATCH

t_{PS}

ADDRESS$_L$

t_{BLA} t_{BHA}

$\overline{BUSY}_L$

Note
37. If t_{PS} is violated, the busy signal is asserted on one side or the other, but there is no guarantee to which side $\overline{BUSY}$ is asserted.

Switching Waveforms (continued)

Figure 14. Interrupt Timing Diagrams
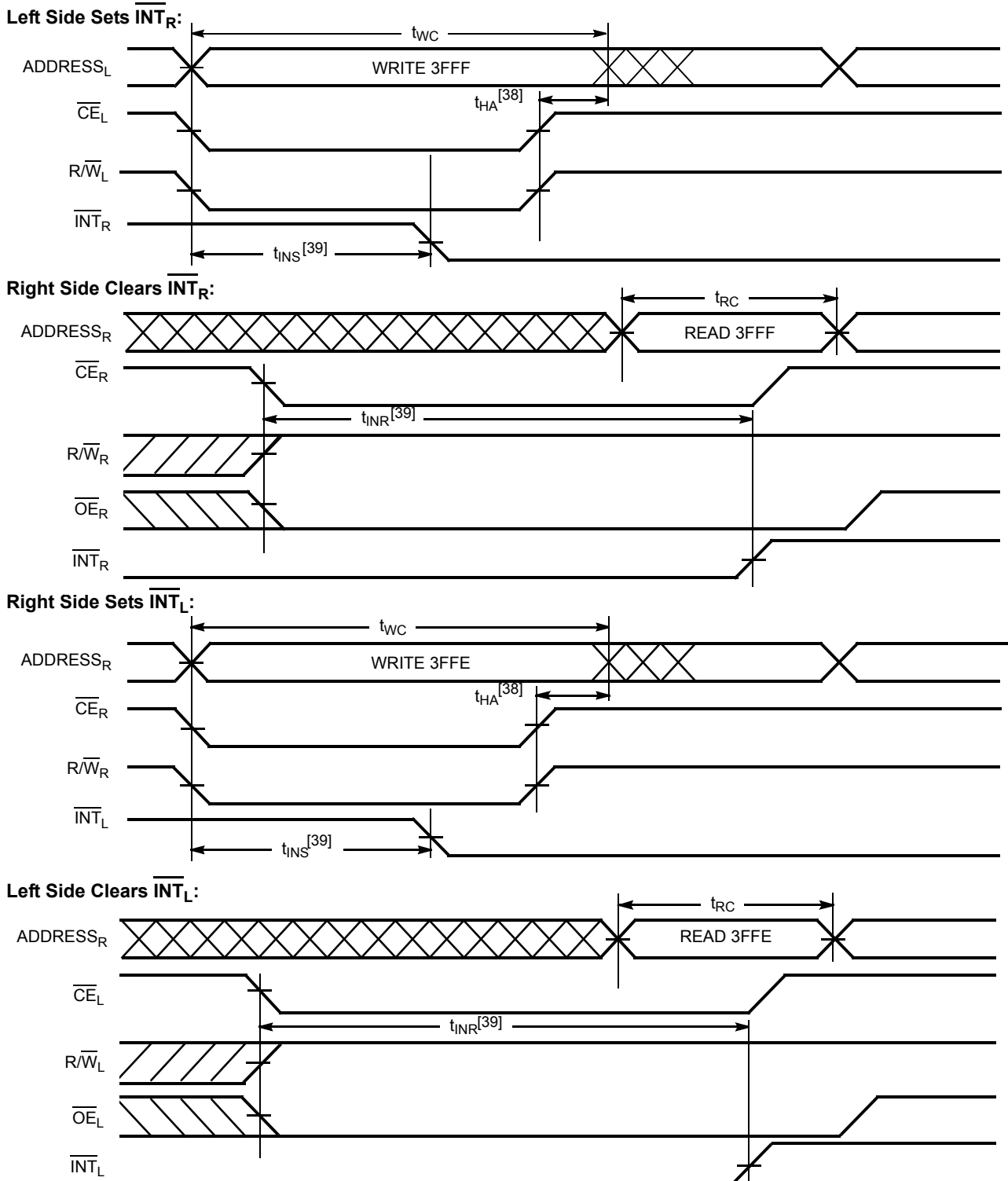
Notes
38. t_{HA} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is deasserted first.
39. t_{INS} or t_{INR} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is asserted last.

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Table 1. Non-Contending Read/Write

CE	R/W	OE	UB	LB	SEM	I/O$_8$–I/O$_{15}$	I/O$_0$–I/O$_7$	Operation
H	X	X	X	X	H	High Z	High Z	Deselected: Power-down
X	X	X	H	H	H	High Z	High Z	Deselected: Power-down
L	L	X	L	H	H	Data in	High Z	Write to upper byte only
L	L	X	H	L	H	High Z	Data in	Write to lower byte only
L	L	X	L	L	H	Data in	Data in	Write to both bytes
L	H	L	L	H	H	Data out	High Z	Read upper byte only
L	H	L	H	L	H	High Z	Data out	Read lower byte only
L	H	L	L	L	H	Data out	Data out	Read both bytes
X	X	H	X	X	X	High Z	High Z	Outputs disabled
H	H	L	X	X	L	Data out	Data out	Read data in semaphore flag
X	H	L	H	H	L	Data out	Data out	Read data in semaphore flag
H	⌐	X	X	X	L	Data in	Data in	Write D$_{IN0}$ into semaphore flag
X	⌐	X	H	H	L	Data in	Data in	Write D$_{IN0}$ into semaphore flag
L	X	X	L	X	L			Not allowed
L	X	X	X	L	L			Not allowed

The column headers Inputs spans CE, R/W, OE, UB, LB, SEM; Outputs spans I/O$_8$–I/O$_{15}$, I/O$_0$–I/O$_7$.

Table 2. Interrupt Operation Example (assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = HIGH)

	Left Port					Right Port				
Function	R/W$_L$	CE$_L$	OE$_L$	A$_{0L-13L}$	$\overline{INT}_L$	R/W$_R$	CE$_R$	OE$_R$	A$_{0R-13R}$	$\overline{INT}_R$
Set right $\overline{INT}_R$ flag	L	L	X	3FFF	X	X	X	X	X	L[41]
Reset right $\overline{INT}_R$ flag	X	X	X	X	X	X	L	L	3FFF	H[40]
Set left $\overline{INT}_L$ flag	X	X	X	X	L[40]	L	L	X	3FFE	X
Reset left $\overline{INT}_L$ flag	X	L	L	3FFE	H[41]	X	X	X	X	X

Table 3. Semaphore Operation Example

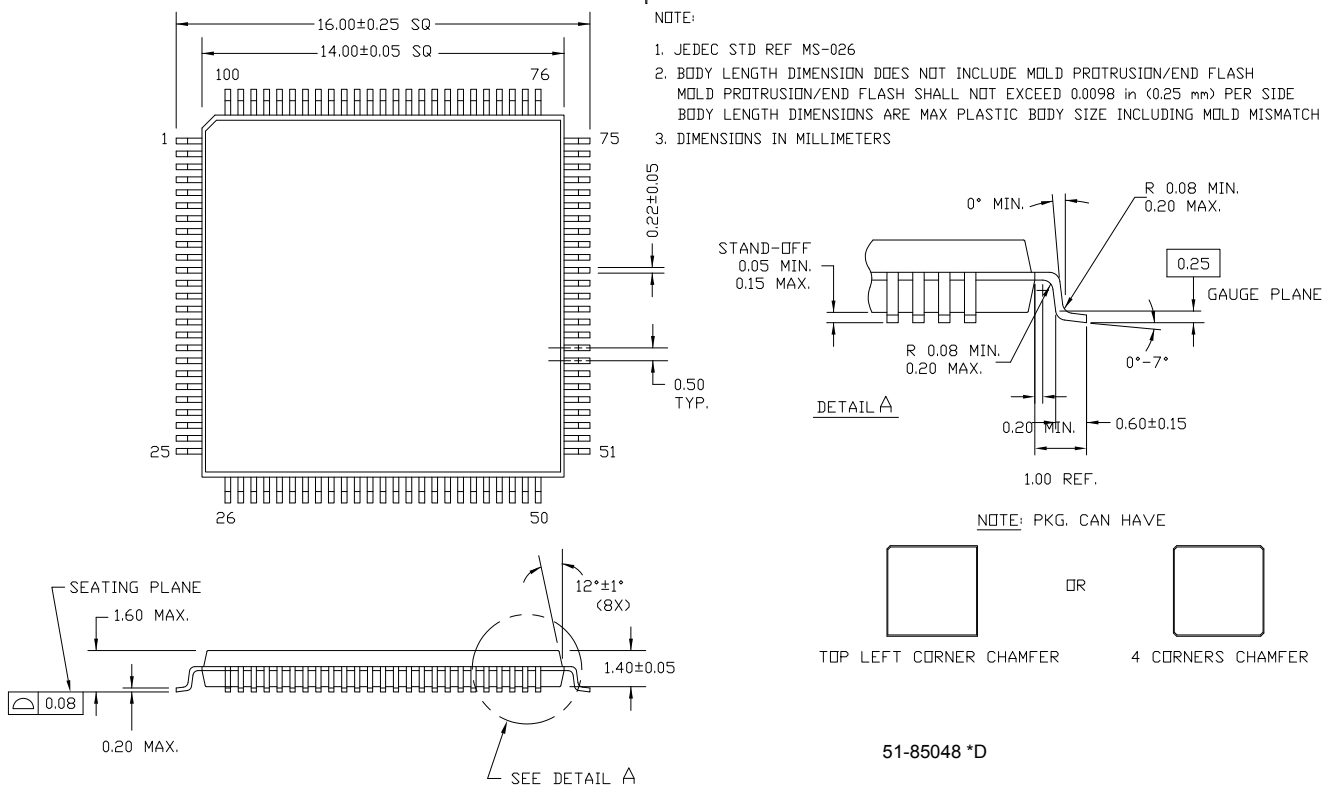| Function	I/O$_0$–I/O$_{15}$ Left	I/O$_0$–I/O$_{15}$ Right	Status
No action	1	1	Semaphore free
Left port writes 0 to semaphore	0	1	Left port has semaphore token
Right port writes 0 to semaphore	0	1	No change. Right side has no write access to semaphore
Left port writes 1 to semaphore	1	0	Right port obtains semaphore token
Left port writes 0 to semaphore	1	0	No change. Left port has no write access to semaphore
Right port writes 1 to semaphore	0	1	Left port obtains semaphore token
Left port writes 1 to semaphore	1	1	Semaphore free
Right port writes 0 to semaphore	1	0	Right port has semaphore token
Right port writes 1 to semaphore	1	1	Semaphore free
Left port writes 0 to semaphore	0	1	Left port has semaphore token
Left port writes 1 to semaphore	1	1	Semaphore free

Notes
40. If $\overline{BUSY}_L$=L, then no change.
41. If $\overline{BUSY}_R$=L, then no change.

Ordering Information

16K x16 Asynchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C026A-15AXI	A100	100-Pin Pb-free Thin Quad Flat Pack	Industrial
20	CY7C026A-20AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C026A-20AXC	A100	100-Pin Pb-free Thin Quad Flat Pack	

Ordering Code Definition

CY7C 026A XX A X C

Temperature Grades
C = Commercial I = Industrial

X: Pb-free

Package Type
A: 100 pin TQFP

Speed Bin: XX = 15 or 20

Density

Company ID: CY = Cypress SRAMs

Package Diagram

Figure 15. 100-Pin Pb-free Thin Plastic Quad Flat Pack (TQFP) A100

Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
TQFP	thin quad plastic flatpack
I/O	input/output
SRAM	static random access memory

Document Conventions

Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	Volts
µA	micro Amperes
mA	milli Amperes
Ω	Ohms
mV	milli Volts
MHz	Mega Hertz
pF	pico Farad
W	Watts
°C	degree Celcius

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Document History Page

Document Title: CY7C026A 16K X 16 Dual-Port Static RAM Document Number: 38-06046				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	110198	SZV	09/29/01	Change from Spec number: 38-00832 to 38-06046
*A	122296	RBI	12/27/02	Power up requirements added to Maximum Ratings Information
*B	237621	YDT	See ECN	Removed cross information from features section
*C	393454	YIM	See ECN	Added Pb-free Logo Added Pb-free parts to ordering information: CY7C026A-15AXC, CY7C026A-20AXC
*D	2623540	VKN/PYRS	12/17/08	Added CY7C026B part Added CY7C026A-15AXI part in the Ordering Information table
*E	2896038	RAME	03/19/10	Removed inactive parts from ordering information table Updated package diagram
*F	3081925	ADMU	11/10/2010	Changed title from CY7C026A/026B, CY7C036A 16K X 16/18 DUAL-PORT STATIC RAM to CY7C026A 16K X 16 DUAL- PORT STATIC RAM Removed all information on CY7C026B and CY7C036A Removed information on speed bin 12. Added Acronyms and Units of Measure table. Added Ordering Code Definition. Updated as per new template

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