256 Kb (64 K × 4) Static RAM

Features

- Fast access time: 15 ns
- Wide voltage range: 5.0V ± 10% (4.5V to 5.5V)
- CMOS for optimum speed/power
- TTL-compatible inputs and outputs
- CY7C194BN is available in 24 DIP, 24 SOJ packages.

General Description

The CY7C194BN is a high-performance CMOS Asynchronous SRAM organized as 64K × 4 bits that supports an asynchronous memory interface. The device features an automatic power-down feature that significantly reduces power consumption when deselected.

See the Truth Table in this data sheet for a complete description of read and write modes.

The CY7C194BN is available in 24 DIP, 24 SOJ package(s).

For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.
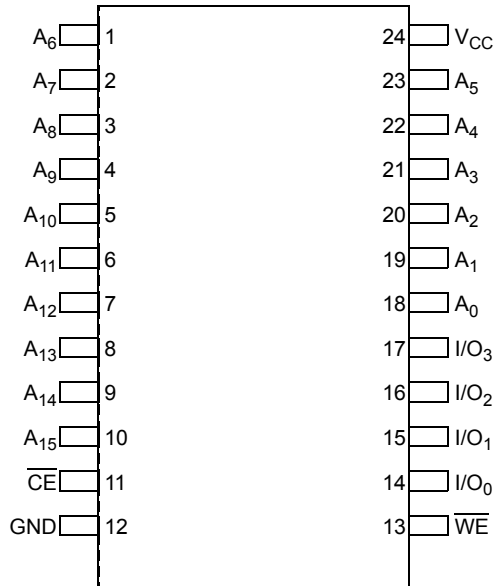
Logic Block Diagram
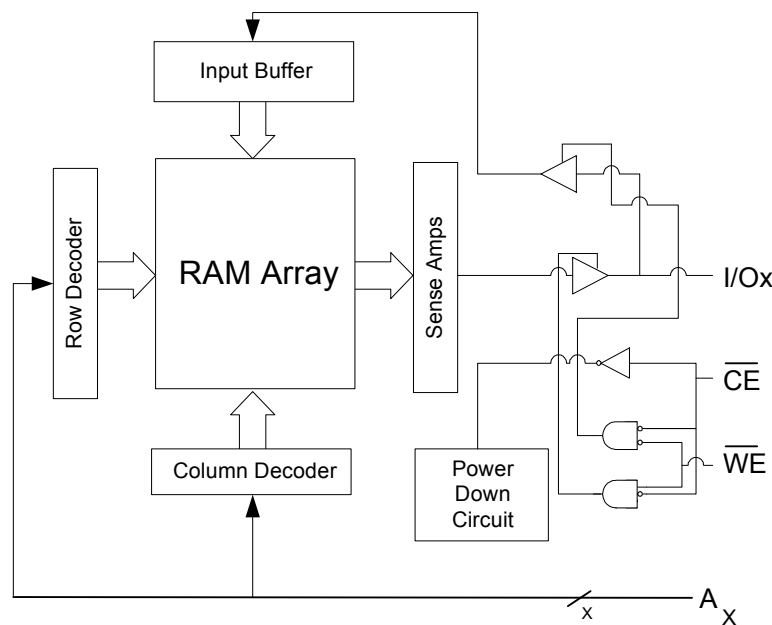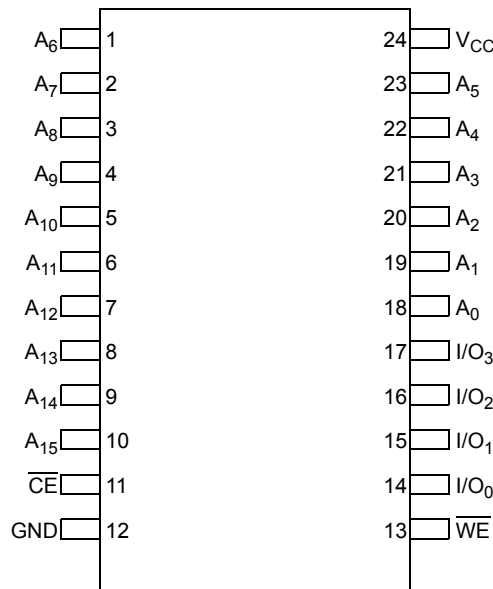

Product Portfolio

Description	-15	Unit
Maximum Access Time	15	ns
Maximum Operating Current	80	mA
Maximum CMOS Standby Current	10	mA

Cypress Semiconductor Corporation • 198 Champion Court • San Jose, CA 95134-1709 • 408-943-2600
Document #: 001-06446 Rev. *B
Revised December 13, 2010

[+] Feedback

Pin Layout and Specification

CY7C194BN 24 SOJ (8 × 15 × 3.5 mm)

A_6	1	24	V_{CC}
A_7	2	23	A_5
A_8	3	22	A_4
A_9	4	21	A_3
A_{10}	5	20	A_2
A_{11}	6	19	A_1
A_{12}	7	18	A_0
A_{13}	8	17	I/O_3
A_{14}	9	16	I/O_2
A_{15}	10	15	I/O_1
$\overline{CE}$	11	14	I/O_0
GND	12	13	$\overline{WE}$

CY7C194BN 24 DIP (6.6 × 31.8 × 3.5 mm)

A_6	1	24	V_{CC}
A_7	2	23	A_5
A_8	3	22	A_4
A_9	4	21	A_3
A_{10}	5	20	A_2
A_{11}	6	19	A_1
A_{12}	7	18	A_0
A_{13}	8	17	I/O_3
A_{14}	9	16	I/O_2
A_{15}	10	15	I/O_1
$\overline{CE}$	11	14	I/O_0
GND	12	13	$\overline{WE}$

[+] Feedback

Pin Description

Pin	Type	Description	CY7C194BN	
			24 DIP	**24 SOJ**
A_X	Input	**Address Inputs**.	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 18, 19, 20, 21, 22, 23	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 18, 19, 20, 21, 22, 23
$\overline{CE}$	Control	**Chip Enable**.	11	11
I/O_X	Input or Output	**Data Input/Outputs**.	14, 15, 16, 17	14, 15, 16, 17
NC	–	**No Connect**. Pins are not internally connected to the die.	–	–
V_{CC}	Supply	**Power (5.0V)**.	24	24
$\overline{WE}$	Control	**Write Enable**.	13	13

CY7C194BN Truth Table

$\overline{CE}$	$\overline{WE}$	I/Ox	Mode	Power
H	X	High Z	Power-Down	Standby (I_{SB})
L	H	Data Out	Read	Active (I_{CC})
L	L	Data In	Write	Active (I_{CC})

Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested.)

Parameter	Description	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_{AMB}	Ambient Temperature with Power Applied (i.e. case temperature)	–55 to +125	°C
V_{CC}	Core Supply Voltage Relative to V_{SS}	–0.5 to +7.0	V
V_{IN}, V_{OUT}	DC Voltage Applied to any Pin Relative to V_{SS}	–0.5 to V_{CC} + 0.5	V
I_{OUT}	Output Short-Circuit Current	20	mA
V_{ESD}	Static Discharge Voltage (per MIL-STD-883, Method 3015)	> 2001	V
I_{LU}	Latch-up Current	> 200	mA

Operating Range

Range	Ambient Temperature (T_A)	Voltage Range (V_{CC})
Commercial	0°C to 70°C	5.0V ± 10%

DC Electrical Characteristics[2]

Parameter	Description	Condition	15 ns Min.	15 ns Max.	Unit
V_{IH}	Input HIGH Voltage		2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.8	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min., Ioh = –4.0 ma	2.4	–	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., Iol = 8.0 ma	–	0.4	V
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = F_{MAX} = 1 / t_{RC}	–	80	mA
I_{SB1}	Automatic $\overline{CE}$ Power-down Current TTL Inputs	V_{CC} = Max., $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = F_{MAX}	–	30	mA
I_{SB2}	Automatic $\overline{CE}$ Power-down Current CMOS Inputs	V_{CC} = Max., $\overline{CE} \geq V_{CC}$ - 0.3v, V_{IN} > V_{CC} - 0.3v or $V_{IN} \leq 0.3$, f = 0, Commercial	–	10	mA
I_{OZ}	Output Leakage Current	GND $\leq$ Vi $\leq V_{CC}$, Output Disabled	–5	+5	µA
I_{IX}	Input Load Current	GND $\leq$ Vi $\leq V_{CC}$	–5	+5	µA

Capacitance[1]

Parameter	Description	Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	7	pF
C_{OUT}	Output Capacitance		10	

Thermal Resistance[3]

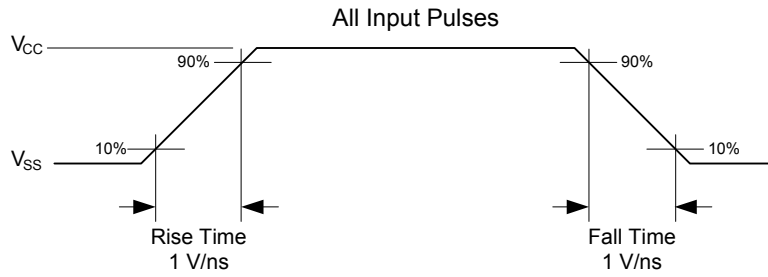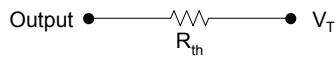| Parameter	Description	Conditions	CY7C194BN 24 DIP	CY7C194BN 24 SOJ	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 square inches, two-layer printed circuit board	75.69	84.15	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		33.80	37.56	

Note
1. Tested initially and after any design or process change that may affect these parameters
2. V_{IL}(min) = –2.0V for pulse durations of less than 20 ns.
3. Test Conditions assume a transition time of 3ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V

[+] Feedback

AC Test Loads

Output Loads

(A)*

Output Loads
for t_{HZCE} & t_{HZWE}

(B)*

Thevenin Equivalent

All Input Pulses

Rise Time
1 V/ns

Fall Time
1 V/ns
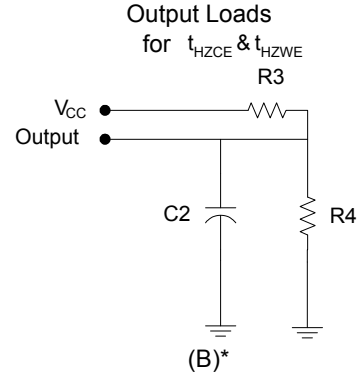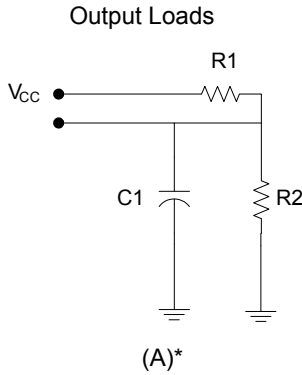
* including scope and jig capacitance

AC Test Conditions

Parameter	Description	Nom.	Unit
C1	Capacitor 1	30	pF
C2	Capacitor 2	5	
R1	Resistor 1	480	Ω
R2	Resistor 2	255	
R3	Resistor 3	480	
R4	Resistor 4	255	
R_{TH}	Resistor Thevenin	167	
V_{TH}	Voltage Thevenin	1.73	V

AC Electrical Characteristics[1, 4, 5, 6]

Parameter	Description	15 ns		Unit
		Min	Max	
t_{RC}	Read Cycle Time	15	–	ns
t_{AA}	Address to Data Valid	–	15	ns
t_{OHA}	Data Hold from Address Change	3	–	ns
t_{ACE}	$\overline{CE}$ to Data Valid	–	15	ns
t_{LZCE}	$\overline{CE}$ to Low Z	3	–	ns
t_{HZCE}	$\overline{CE}$ to High Z	–	7	ns
t_{PU}	$\overline{CE}$ to Power-up	0	–	ns
t_{PD}	$\overline{CE}$ to Power-down	–	15	ns
t_{WC}	Write Cycle Time	15	–	ns
t_{SCE}	$\overline{CE}$ to Write End	10	–	ns
t_{AW}	Address Set-up to Write End	10	–	ns
t_{HA}	Address Hold from Write End	0	–	ns
t_{SA}	Address Set-up to Write Start	0	–	ns
t_{PWE}	$\overline{WE}$ Pulse Width	9	–	ns
t_{SD}	Data Set-Up to Write End	8	–	ns
t_{HD}	Data Hold from Write End	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z	–	7	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z	3	–	ns

Timing Waveforms

Read Cycle No. 1[7, 8]
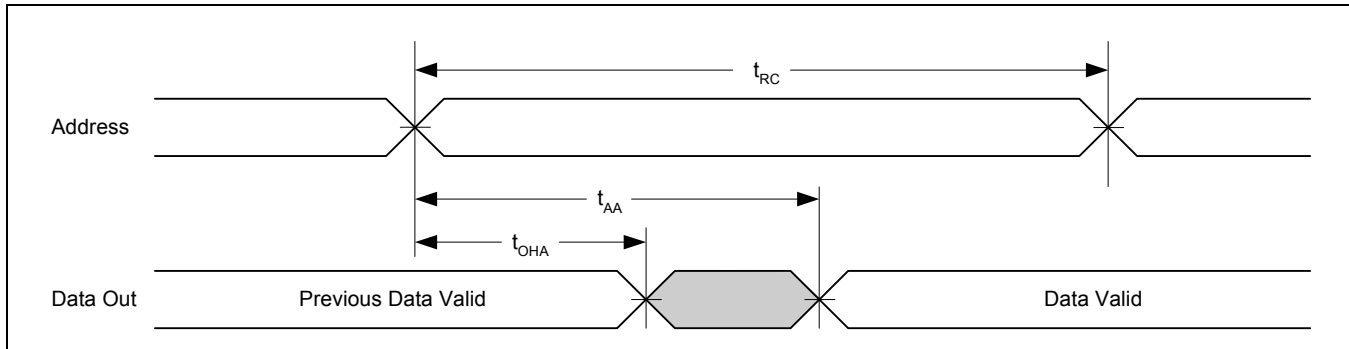
Notes
4. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, and t_{HZWE} is less than t_{LZWE} for any given device.
5. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
6. t_{HZCE}, t_{HZWE} are specified as in part (b) of the A/C Test Loads. Transitions are measured ± 200 mV from steady state voltage.
7. Device is continuously selected. $\overline{CE} = V_{IL}$.
8. $\overline{WE}$ is HIGH for Read Cycle.

[+] Feedback

Timing Waveforms (continued)

Read Cycle No. 2[1, 9, 10]
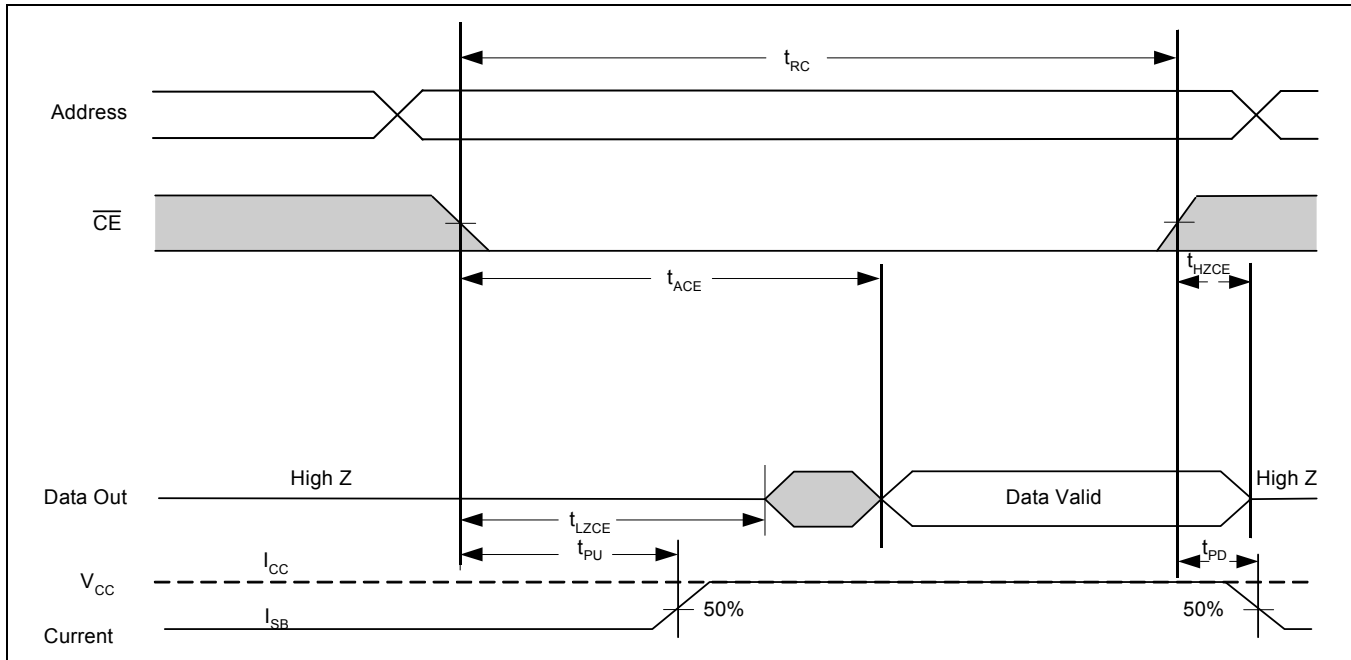
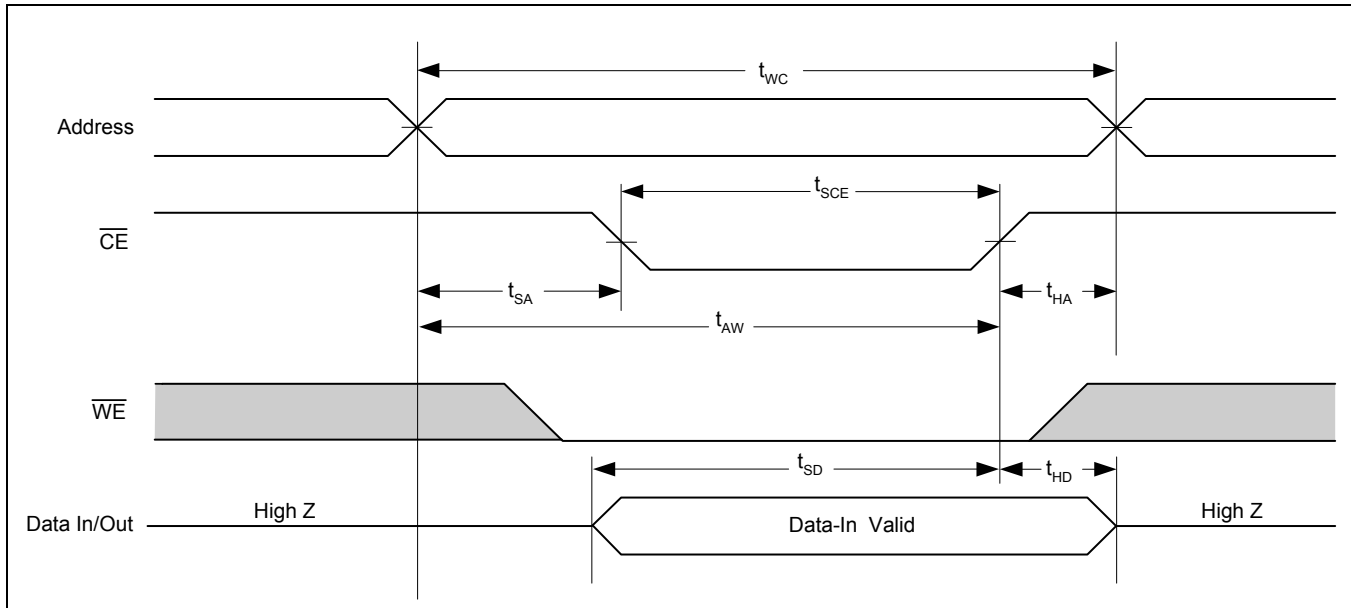### Write Cycle No. 1 ($\overline{WE}$ Controlled)[1, 11]
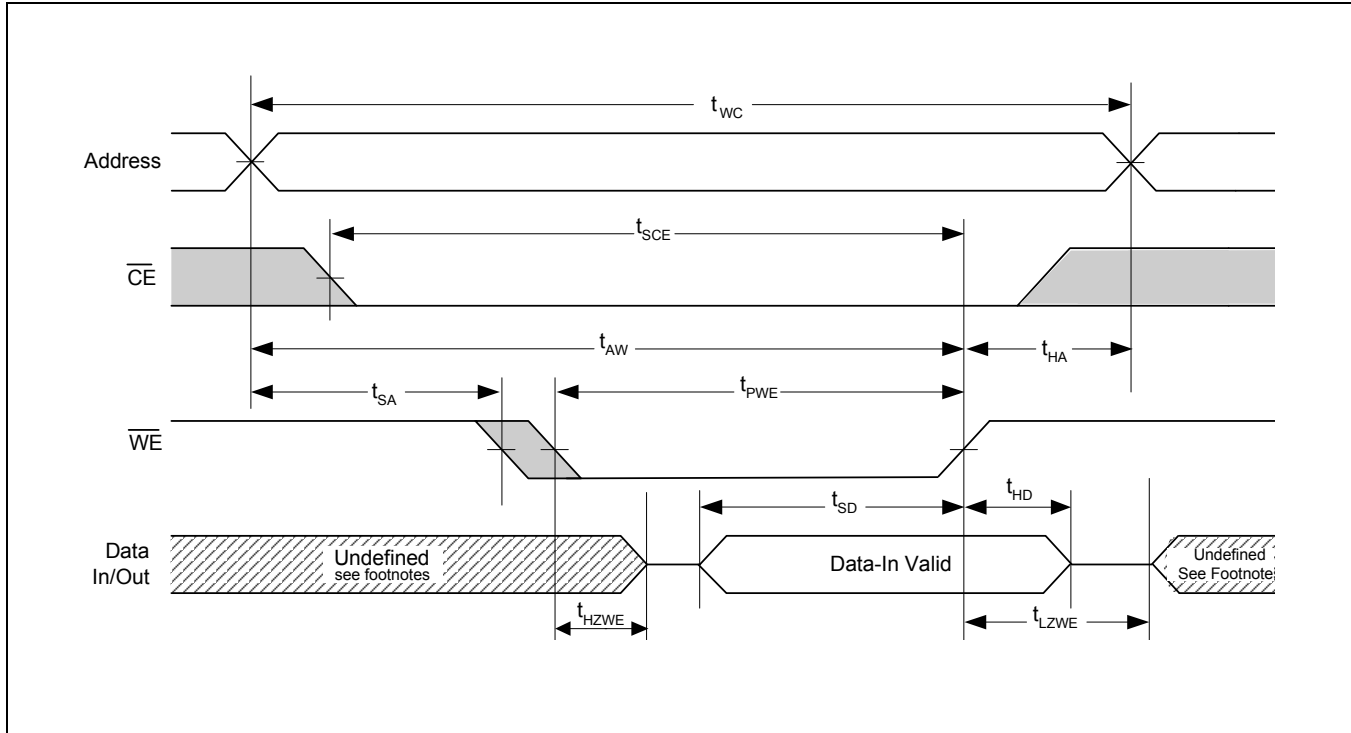
Notes
9. $\overline{WE}$ is HIGH in read cycle.
10. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
11. The minimum write cycle time is the sum of t_{HZWE} and t_{SD}.

Timing Waveforms (continued)
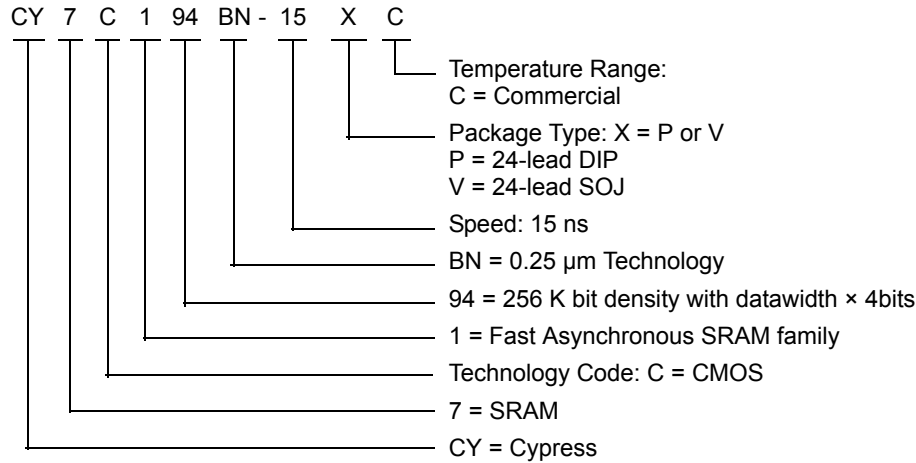
Write Cycle No. 2 ($\overline{CE}$ Controlled)[12, 13]

Notes
12. This cycle is $\overline{CE}$ controlled.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Power Option	Operating Range
15	CY7C194BN-15PC	51-85013	24 DIP (6.6 x 31.8 x 3.5 mm)	Standard	Commercial
	CY7C194BN-15VC	51-85030	24 SOJ (8 x 15 x 3.5 mm)	Standard	Commercial

Ordering Code Definitions

CY 7 C 1 94 BN - 15 X C

Temperature Range:
C = Commercial

Package Type: X = P or V
P = 24-lead DIP
V = 24-lead SOJ

Speed: 15 ns

BN = 0.25 µm Technology

94 = 256 K bit density with datawidth × 4bits

1 = Fast Asynchronous SRAM family

Technology Code: C = CMOS

7 = SRAM

CY = Cypress

Please contact local sales representative regarding availability of these parts.

Package Diagrams

Figure 1. 24-pin (300-mil) SOJ (51-85030)
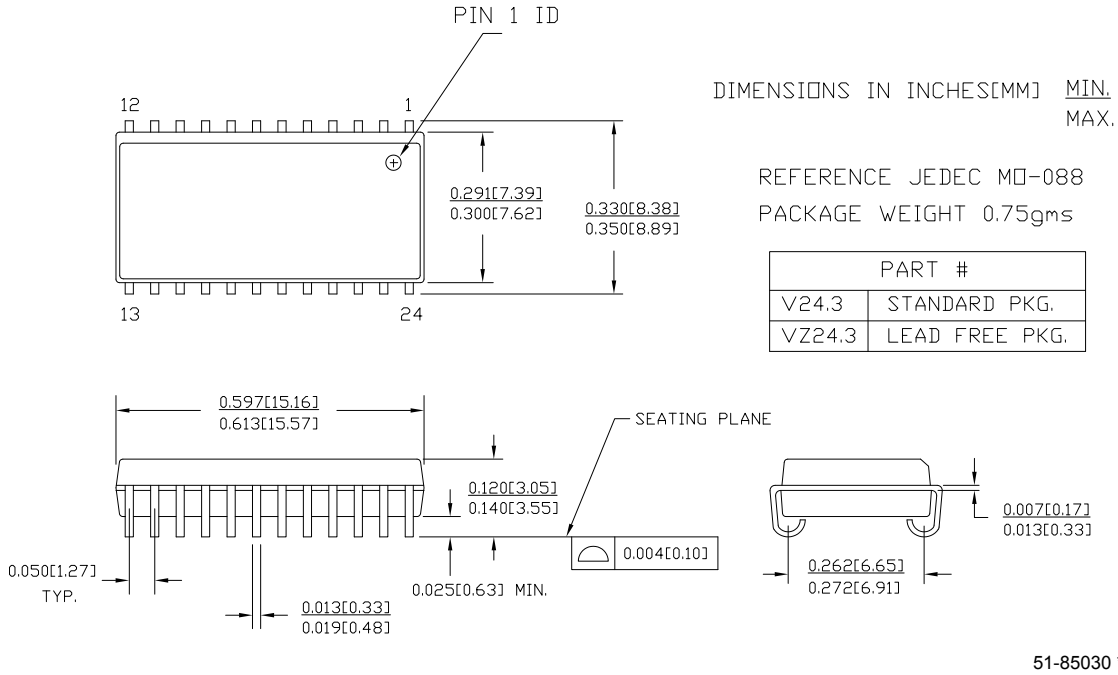
Figure 2. 24 DIP (6.6 x 31.8 x 3.5 mm) (51-85013)

[+] Feedback
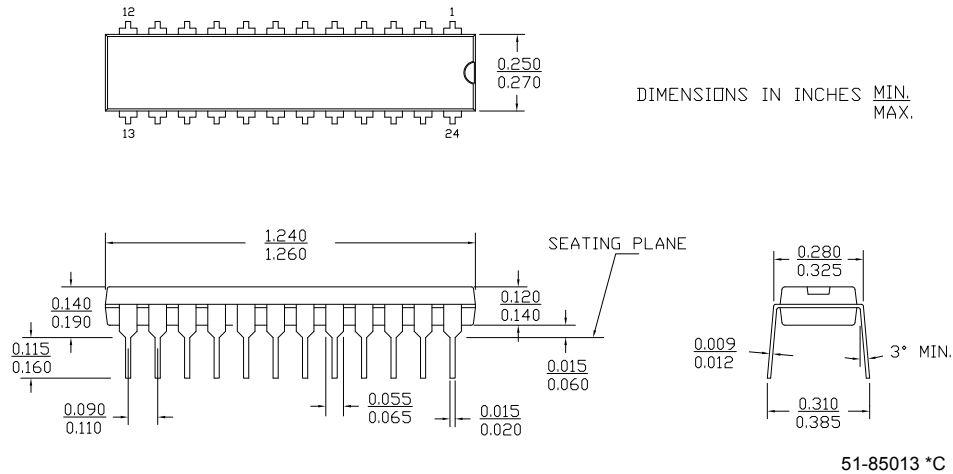
Document History Page

Document Title: CY7C194BN 256 Kb (64 K × 4) Static RAM Document Number: 001-06446				
REV.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	424111	See ECN	NXR	New Data Sheet
*A	2892510	03/18/2010	VKN	Removed 25ns speed bin Updated Ordering Information table Updated Package Diagram Added Sales, Solutions, and Legal Information
*B	3108898	12/13/2010	AJU	Added Ordering Code Definitions.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive	
Clocks & Buffers	cypress.com/go/clocks	
Interface	cypress.com/go/interface	
Lighting & Power Control	cypress.com/go/powerpsoc	
	cypress.com/go/plc	
Memory	cypress.com/go/memory	
Optical & Image Sensing	cypress.com/go/image	
PSoC	cypress.com/go/psoc	
Touch Sensing	cypress.com/go/touch	
USB Controllers	cypress.com/go/USB	
Wireless/RF	cypress.com/go/wireless	

PSoC Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 5

All products and company names mentioned in this document may be the trademarks of their respective holders.