

**Features**

- Very high speed: 45 ns
- Wide voltage range: 2.2 V to 3.6 V and 4.5 V to 5.5 V
- Ultra low standby power
  - Typical standby current: 1  $\mu$ A
  - Maximum standby current: 7  $\mu$ A
- Ultra low active power
  - Typical active current: 2 mA at f = 1 MHz
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 44-pin thin small outline package (TSOP) II package

**Functional Description**

The CY62136ESL is a high performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL<sup>®</sup>) in portable

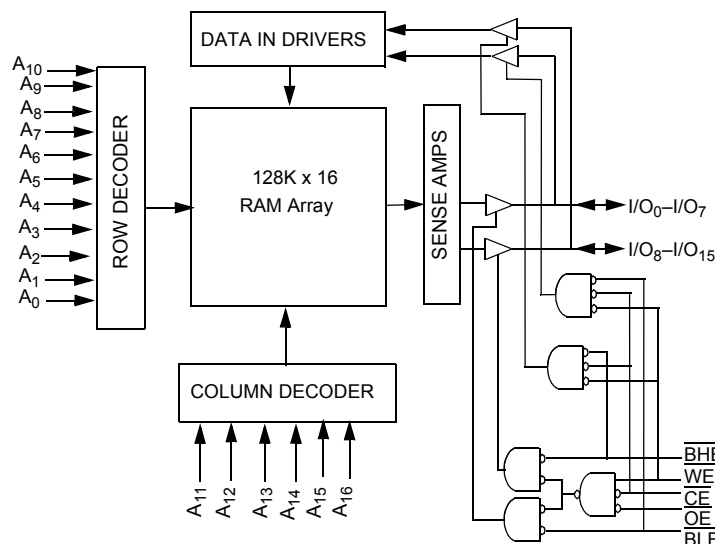
applications such as cellular telephones. The device also has an automatic power down feature that reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected ( $\overline{CE}$  HIGH). The input and output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), both Byte High Enable and Byte Low Enable are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH) or during a write operation ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW).

To write to the device, take Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>).

To read from the device, take Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins appears on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory appears on I/O<sub>8</sub> to I/O<sub>15</sub>. See the "Truth Table" on page 11 for a complete description of read and write modes.

For best practice recommendations, refer to the Cypress application note [AN1064, SRAM System Guidelines](#).

**Logic Block Diagram**

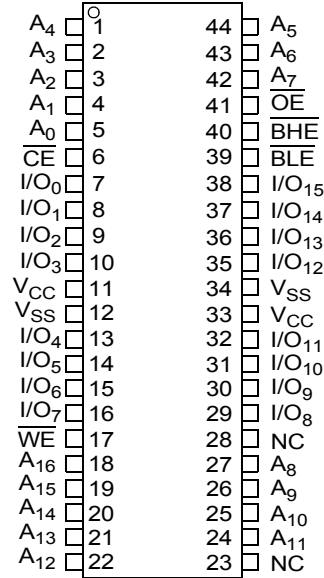


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## Pin Configuration

Figure 1. 44-Pin TSOP II (Top View) <sup>[1]</sup>



## Product Portfolio

Product	Range	V <sub>CC</sub> Range (V) <sup>[2]</sup>	Speed (ns)	Power Dissipation					
				Operating I <sub>CC</sub> , (mA)				Standby, I <sub>SB2</sub> (μA)	
				f = 1MHz		f = f <sub>max</sub>			
				Typ <sup>[3]</sup>	Max	Typ <sup>[3]</sup>	Max	Typ <sup>[3]</sup>	Max
CY62136ESL	Industrial	2.2 V to 3.6 V and 4.5 V to 5.5 V	45	2	2.5	15	20	1	7

### Notes

1. NC pins are not connected on the die.
2. Datasheet specifications are not guaranteed for V<sub>CC</sub> in the range of 3.6 V to 4.5 V
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = 3V, and V<sub>CC</sub> = 5V, T<sub>A</sub> = 25 °C

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature..... -65 °C to +150 °C

Ambient temperature with power applied ..... -55 °C to +125 °C

Supply voltage to ground potential ..... -0.5 V to 6.0 V

DC voltage applied to outputs in High-Z State<sup>[4, 5]</sup>..... -0.5 V to 6.0 V

DC input voltage<sup>[4, 5]</sup>..... -0.5 V to 6.0 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage..... >2001 V (MIL-STD-883, Method 3015) Latch up current ..... >200 mA

## Operating Range

Device	Range	Ambient Temperature	V <sub>CC</sub> <sup>[6]</sup>
CY62136ESL	Industrial	-40 °C to +8 5°C	2.2 V–3.6 V, and 4.5 V–5.5 V

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	45 ns			Unit	
			Min	Typ <sup>[7]</sup>	Max		
V <sub>OH</sub>	Output HIGH voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7	I <sub>OH</sub> = -0.1 mA	2.0	-	-	V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6	I <sub>OH</sub> = -1.0 mA	2.4	-	-	
		4.5 ≤ V <sub>CC</sub> ≤ 5.5	I <sub>OH</sub> = -1.0 mA	2.4	-	-	
V <sub>OL</sub>	Output LOW voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7	I <sub>OL</sub> = 0.1 mA	-	-	0.4	V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6	I <sub>OL</sub> = 2.1 mA	-	-	0.4	
		4.5 ≤ V <sub>CC</sub> ≤ 5.5	I <sub>OL</sub> = 2.1 mA	-	-	0.4	
V <sub>IH</sub>	Input HIGH voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7		1.8	-	V <sub>CC</sub> + 0.3	V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6		2.2	-	V <sub>CC</sub> + 0.3	
		4.5 ≤ V <sub>CC</sub> ≤ 5.5		2.2	-	V <sub>CC</sub> + 0.5	
V <sub>IL</sub>	Input LOW voltage	2.2 ≤ V <sub>CC</sub> ≤ 2.7		-0.3	-	0.6	V
		2.7 ≤ V <sub>CC</sub> ≤ 3.6		-0.3	-	0.8	
		4.5 ≤ V <sub>CC</sub> ≤ 5.5		-0.5	-	0.8	
I <sub>IX</sub>	Input leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>		-1	-	+1	μA
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output disabled		-1	-	+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating supply current	f = f <sub>max</sub> = 1/t <sub>RC</sub>	V <sub>CC</sub> = V <sub>CCmax</sub>	-	15	20	mA
		f = 1 MHz	I <sub>OUT</sub> = 0 mA, CMOS levels	-	2	2.5	
I <sub>SB1</sub> <sup>[8]</sup>	Automatic CE power-down current — CMOS inputs	$\overline{CE} \geq V_{CC} - 0.2 \text{ V}$ , $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$ , $f = f_{max}$ (Address and data only), $f = 0$ ( $\overline{OE}$ , $\overline{BHE}$ , $\overline{BLE}$ and $\overline{WE}$ ), $V_{CC} = V_{CC(max)}$		-	1	7	μA
I <sub>SB2</sub> <sup>[8]</sup>	Automatic CE power-down current — CMOS inputs	$\overline{CE} \geq V_{CC} - 0.2 \text{ V}$ , $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$ , $f = 0$ , $V_{CC} = V_{CC(max)}$		-	1	7	μA

### Notes

- V<sub>IL</sub>(min) = -2.0 V for pulse durations less than 20 ns.
- V<sub>IH</sub>(max) = V<sub>CC</sub> + 0.75 V for pulse durations less than 20 ns
- Full Device AC operation assumes a 100 μs ramp time from 0 to V<sub>CC</sub> (min) and 200 μs wait time after V<sub>CC</sub> stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = 3 V, and V<sub>CC</sub> = 5V, T<sub>A</sub> = 25 °C.
- Chip enable (CE) and byte enables (BHE and BLE) need to be tied to CMOS levels to meet the I<sub>SB1</sub> / I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can be left floating.

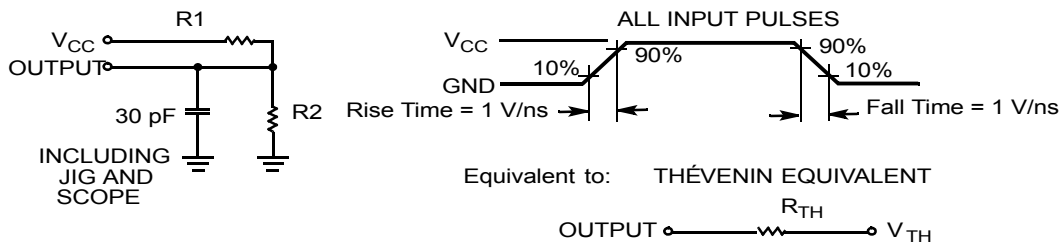
### Capacitance.

Parameter <sup>[9]</sup>	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub>	10	pF
C <sub>OUT</sub>	Output capacitance		10	pF

### Thermal Resistance

Parameter <sup>[9]</sup>	Description	Test Conditions	TSOP II	Unit
Θ <sub>JA</sub>	Thermal resistance (Junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	77	°C / W
Θ <sub>JC</sub>	Thermal resistance (Junction to case)		13	°C / W

Figure 2. AC Test Loads and Waveforms



Parameters	2.5 V	3.0 V	5.0 V	Unit
R1	16667	1103	1800	Ω
R2	15385	1554	990	Ω
R <sub>TH</sub>	8000	645	639	Ω
V <sub>TH</sub>	1.20	1.75	1.77	V

**Note**  
9. Tested initially and after any design or process changes that may affect these parameters

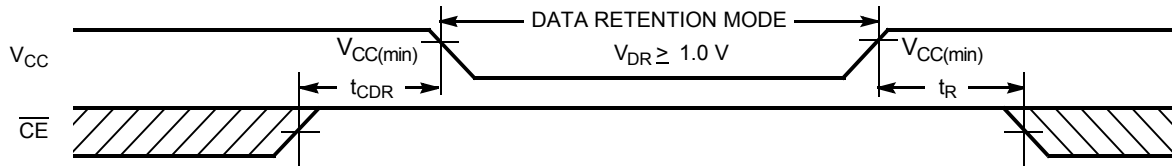
### Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ <sup>[10]</sup>	Max	Unit
V <sub>DR</sub>	V <sub>CC</sub> for data retention		1.0	–	–	V
I <sub>CCDR</sub> <sup>[11]</sup>	Data retention current	$\overline{CE} \geq V_{CC} - 0.2 \text{ V}$ , $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$	–	0.8	3	μA
t <sub>CDR</sub> <sup>[12]</sup>	Chip deselect to data retention time		0	–	–	ns
t <sub>R</sub> <sup>[13]</sup>	Operation recovery time		45	–	–	ns

### Data Retention Waveform

Figure 3. Data Retention Waveform



**Notes**

- 10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(typ), T<sub>A</sub> = 25 °C
- 11. Chip enable ( $\overline{CE}$ ) and byte enables (BHE and BLE) need to be tied to CMOS levels to meet the I<sub>SB1</sub> / I<sub>SB2</sub> / I<sub>CCDR</sub> specification. Other inputs can be left floating
- 12. Tested initially and after any design or process changes that may affect these parameters
- 13. Full device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC(min)</sub> ≥ 100 μs or stable at V<sub>CC(min)</sub> ≥ 100 μs

## Switching Characteristics

Over the Operating Range

Parameter <sup>[14,15]</sup>	Description	45 ns		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{RC}$	Read cycle time	45	–	ns
$t_{AA}$	Address to data valid	–	45	ns
$t_{OHA}$	Data hold from address change	10	–	ns
$t_{ACE}$	$\overline{CE}$ LOW to data valid	–	45	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid	–	22	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z <sup>[16]</sup>	5	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[16, 17]</sup>	–	18	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[16]</sup>	10	–	ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[16, 17]</sup>	–	18	ns
$t_{PU}$	$\overline{CE}$ LOW to power-up	0	–	ns
$t_{PD}$	$\overline{CE}$ HIGH to ower-down	–	45	ns
$t_{DBE}$	$\overline{BLE/BHE}$ LOW to data valid	–	22	ns
$t_{LZBE}$	$\overline{BLE/BHE}$ LOW to Low Z <sup>[16]</sup>	5	–	ns
$t_{HZBE}$	$\overline{BLE/BHE}$ HIGH to High Z <sup>[16, 17]</sup>	–	18	ns
<b>Write Cycle<sup>[18]</sup></b>				
$t_{WC}$	Write cycle time	45	–	ns
$t_{SCE}$	$\overline{CE}$ LOW to write end	35	–	ns
$t_{AW}$	Address setup to write end	35	–	ns
$t_{HA}$	Address hold from write end	0	–	ns
$t_{SA}$	Address setup to write start	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	35	–	ns
$t_{BW}$	$\overline{BLE/BHE}$ LOW to write end	35	–	ns
$t_{SD}$	Data setup to write end	25	–	ns
$t_{HD}$	Data hold from write end	0	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[16, 17]</sup>	–	18	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[16]</sup>	10	–	ns

### Notes

14. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3 V, and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the [AC Test Loads and Waveforms on page 5](#)
15. AC timing parameters are subject to byte enable signals (BHE or BLE) not switching when chip is disabled. See [application note AN13842](#) for further clarification
16. At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any device
17.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high-impedance state.
18. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ , BHE, BLE or both =  $V_{IL}$ . All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

## Switching Waveforms

Figure 4. Read Cycle No.1: Address Transition Controlled [19, 20]

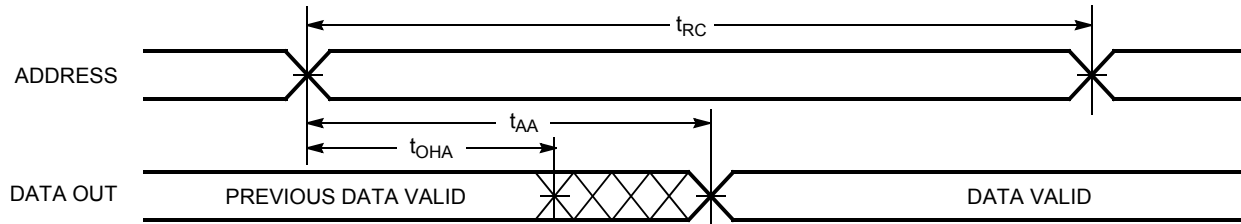
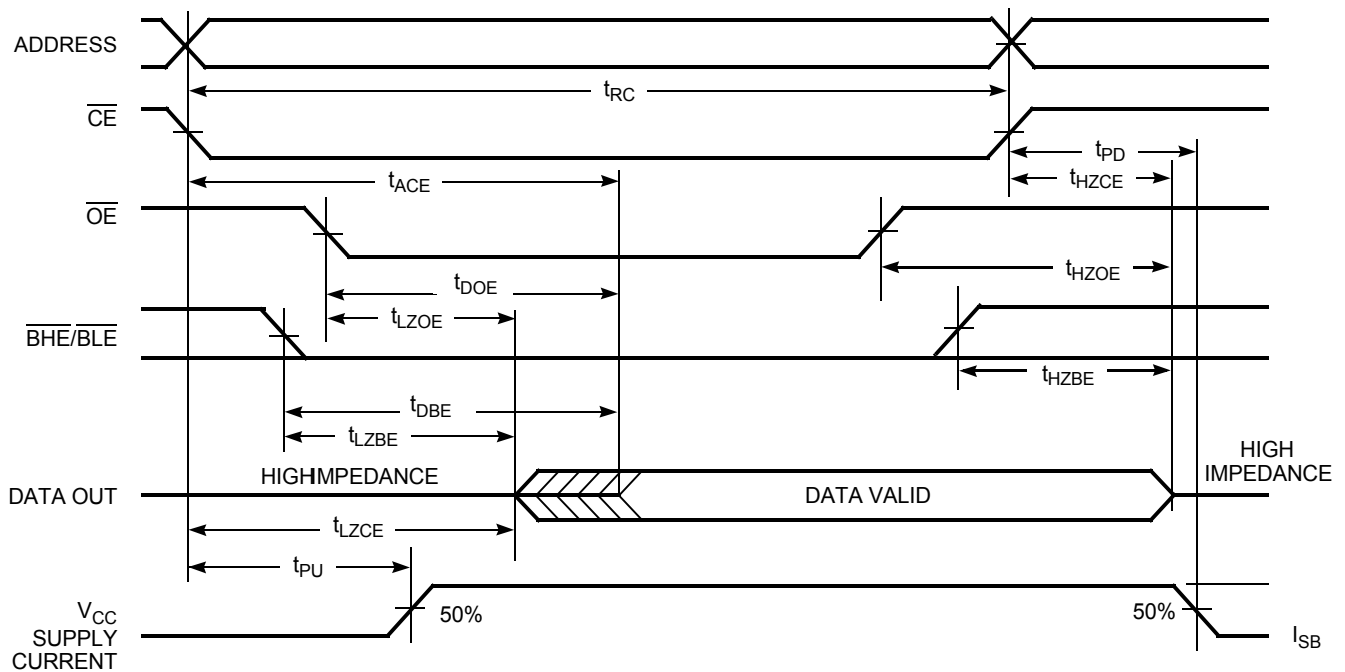


Figure 5. Read Cycle No. 2:  $\overline{OE}$  Controlled [20, 21]



### Notes

19. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$  =  $V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$ , or both =  $V_{IL}$ .
20.  $\overline{WE}$  is HIGH for read cycle.
21. Address valid before or similar to  $\overline{CE}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW.



Switching Waveforms (continued)

Figure 6. Write Cycle No 1:  $\overline{WE}$  Controlled [22, 23, 24]

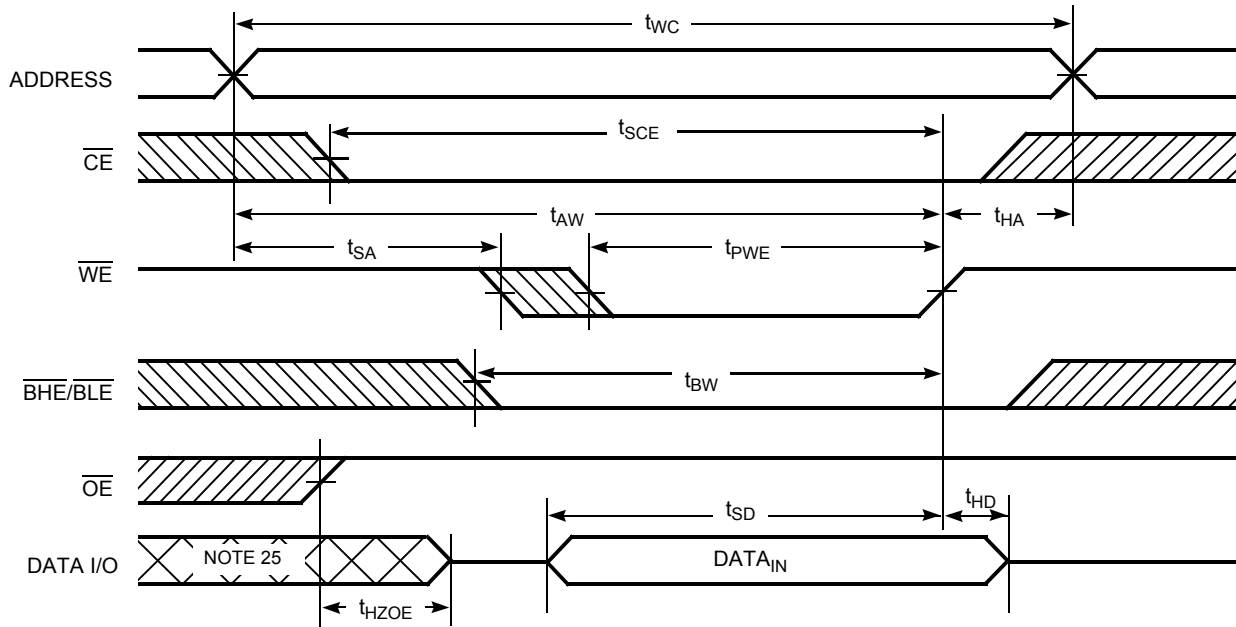
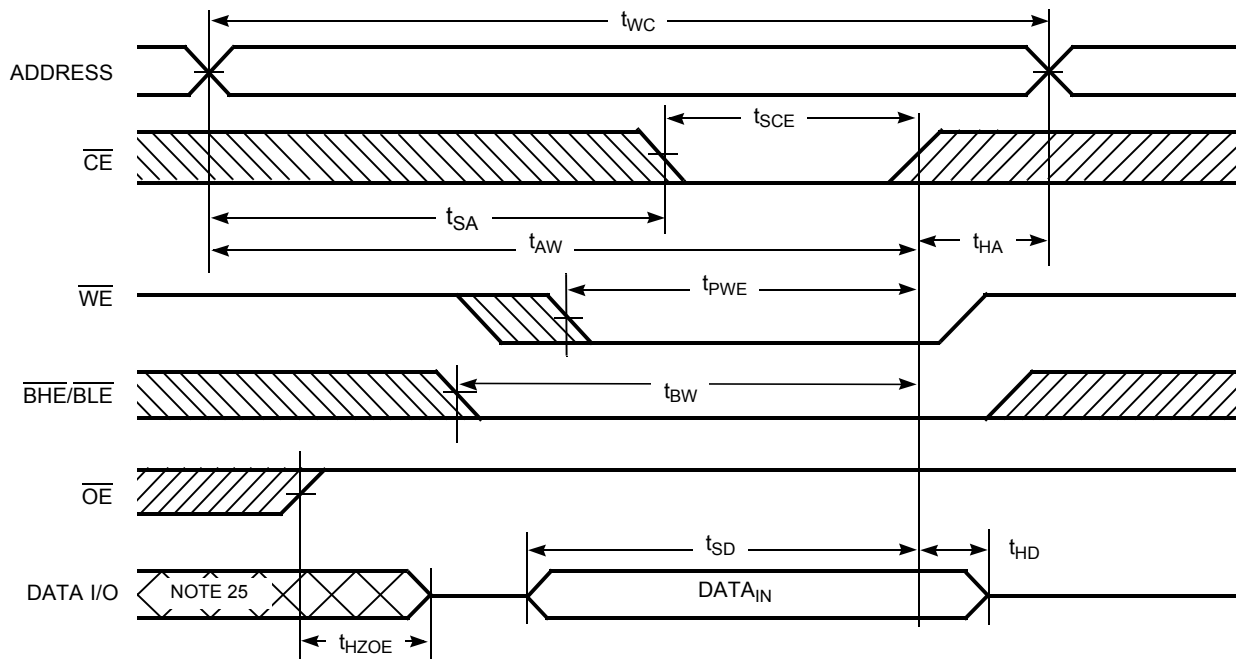


Figure 7. Write Cycle No 2:  $\overline{CE}$  Controlled [22, 23, 24]



Notes

22. The internal write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ . All signals are ACTIVE to initiate a write and any of these signals terminate a write by going INACTIVE. The data input setup and hold timing are referenced to the edge of the signal that terminates the write.

23. Data I/O is high impedance if  $OE = V_{IH}$ .

24. If  $\overline{CE}$  goes HIGH simultaneously with  $WE = V_{IH}$ , the output remains in a high impedance state.

25. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 8. Write Cycle 3:  $\overline{WE}$  Controlled,  $\overline{OE}$  LOW <sup>[26]</sup>

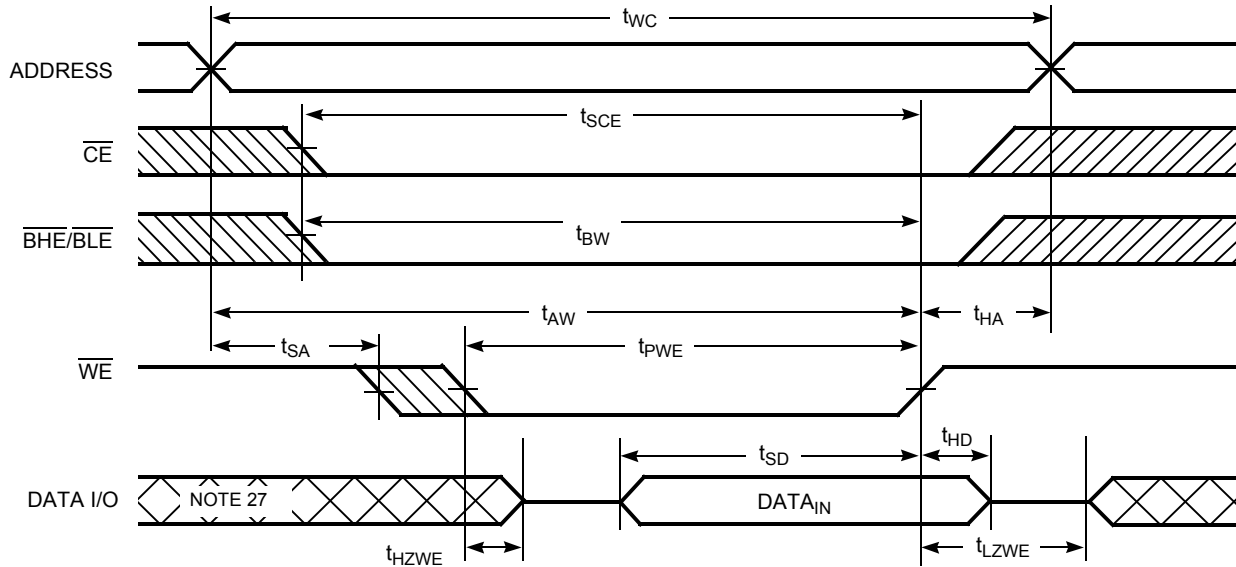
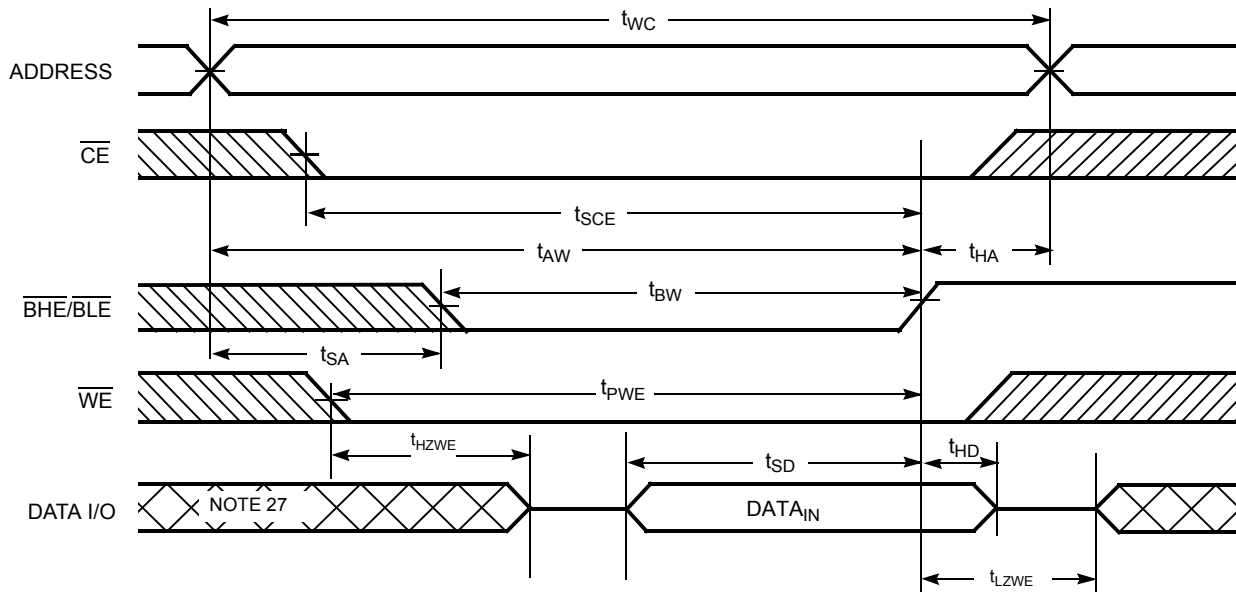


Figure 9. Write Cycle 4:  $\overline{BHE}/\overline{BLE}$  Controlled,  $\overline{OE}$  LOW <sup>[26]</sup>



Notes

- 26. If CE goes HIGH simultaneously with  $\overline{WE} = VIH$ , the output remains in a high impedance state.
- 27. During this period, the I/Os are in output state. Do not apply input signals.

**Truth Table**

$\overline{\text{CE}}^{[28]}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{BHE}}$	$\overline{\text{BLE}}$	Inputs/Outputs	Mode	Power
H	X	X	X <sup>[28]</sup>	X <sup>[28]</sup>	High Z	Deselect/power-down	Standby ( $I_{\text{SB}}$ )
L	X	X	H	H	High Z	Output disabled	Active ( $I_{\text{CC}}$ )
L	H	L	L	L	Data out ( $I/O_0$ – $I/O_{15}$ )	Read	Active ( $I_{\text{CC}}$ )
L	H	L	H	L	Data out ( $I/O_0$ – $I/O_7$ ); $I/O_8$ – $I/O_{15}$ in High-Z	Read	Active ( $I_{\text{CC}}$ )
L	H	L	L	H	Data out ( $I/O_8$ – $I/O_{15}$ ); $I/O_0$ – $I/O_7$ in High-Z	Read	Active ( $I_{\text{CC}}$ )
L	H	H	L	L	High-Z	Output disabled	Active ( $I_{\text{CC}}$ )
L	H	H	H	L	High-Z	Output disabled	Active ( $I_{\text{CC}}$ )
L	H	H	L	H	High-Z	Output disabled	Active ( $I_{\text{CC}}$ )
L	L	X	L	L	Data in ( $I/O_0$ – $I/O_{15}$ )	Write	Active ( $I_{\text{CC}}$ )
L	L	X	H	L	Data in ( $I/O_0$ – $I/O_7$ ); $I/O_8$ – $I/O_{15}$ in High-Z	Write	Active ( $I_{\text{CC}}$ )
L	L	X	L	H	Data in ( $I/O_8$ – $I/O_{15}$ ); $I/O_0$ – $I/O_7$ in High-Z	Write	Active ( $I_{\text{CC}}$ )

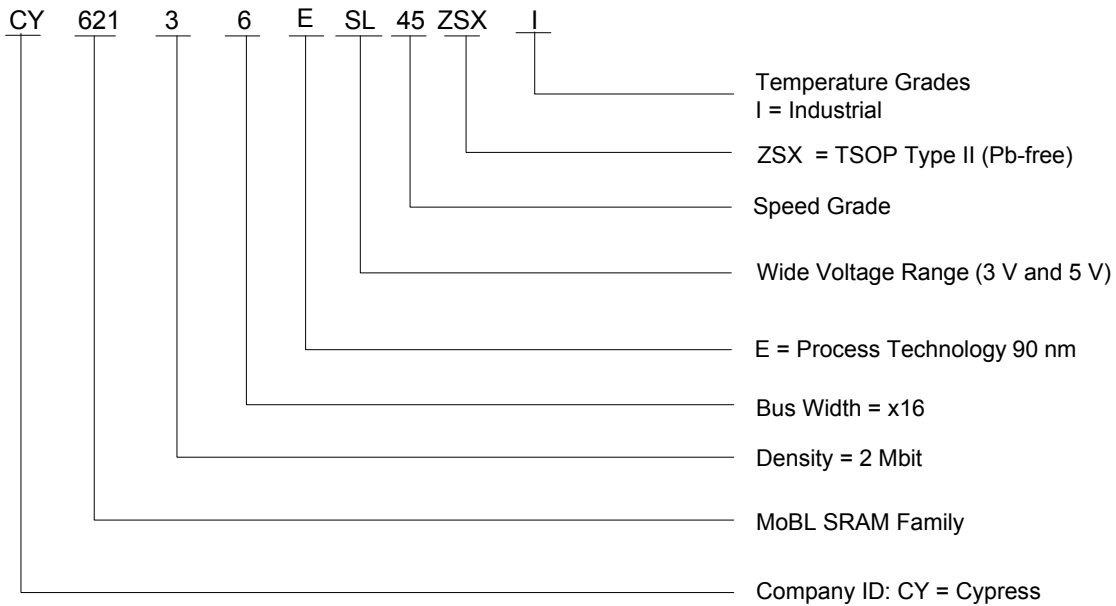
**Note**

28. The 'X' (Don't care) state for the Chip enable (CE) and Byte enables ( $\overline{\text{BHE}}$  and  $\overline{\text{BLE}}$ ) in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

### Ordering Information

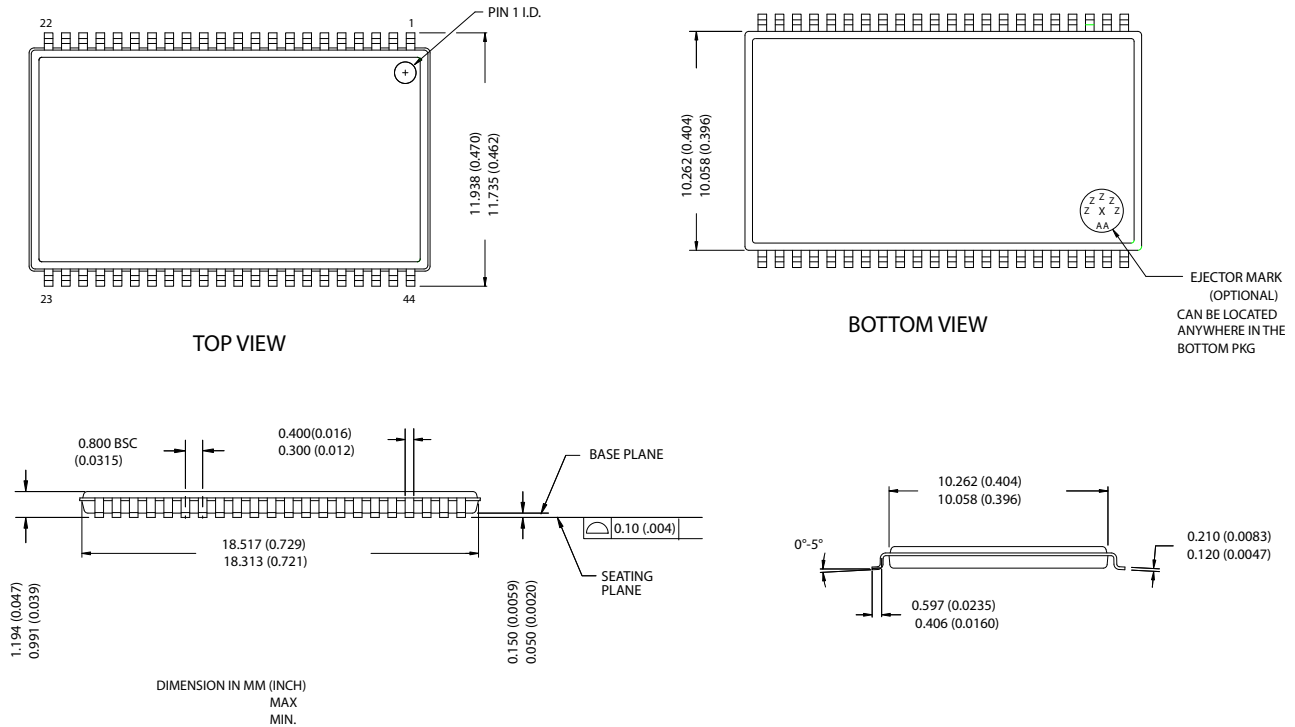
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62136ESL-45ZSXI	51-85087	44-Pin TSOP Type II (Pb-free)	Industrial

### Ordering Code Definition



## Package Diagram

Figure 10. 44-Pin TSOP II, 51-85087



51-85087-°C

## Acronyms

Acronym	Description
$\overline{\text{BHE}}$	byte high enable
$\overline{\text{BLE}}$	byte low enable
CMOS	complementary metal oxide semiconductor
$\overline{\text{CE}}$	chip enable
I/O	input/output
$\overline{\text{OE}}$	output enable
SRAM	static random access memory
TSOP	thin small outline package
VFBGA	very fine ball gird array
$\overline{\text{WE}}$	write enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
μA	microamperes
mA	milliamperes
MHz	megahertz
ns	nanoseconds
pF	picofarads
V	volts
Ω	ohms
W	watts

## Document History Page

Document Title: CY62136ESL MoBL <sup>®</sup> 2 Mbit (128K x 16) Static RAM Document Number: 001-48147				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	2615537	VKN/PYRS	12/03/08	New Data Sheet
*A	2718906	VKN	06/15/2009	Post to external web
*B	2944332	VKN	06/04/2010	Added <a href="#">Contents</a> Added footnote for I <sub>SB2</sub> parameter in <a href="#">Electrical Characteristics</a> Added Footnote 2 in <a href="#">Switching Characteristics</a> Added footnote related to Chip enable and Byte enables in <a href="#">Truth Table</a> Updated <a href="#">Package Diagram</a> Updated links in <a href="#">Sales, Solutions, and Legal Information</a>
*C	3126445	RAME	01/03/2011	Updated datasheet as per new template Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> Table Added <a href="#">Ordering Code Definition</a> Converted all tablenote to footnote.

## Sales, Solutions, and Legal Information

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