

64-Kbit (8 K × 8) Static RAM

Features

- High speed

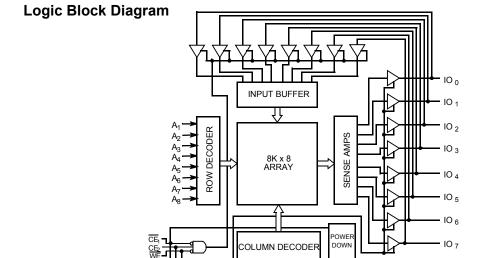
 □ 15 ns
- Fast t_{DOE}
- Low active power ☐ 715 mW
- Low standby power □ 85 mW
- CMOS for optimum speed/power
- Easy memory expansion with \overline{CE}_1 , CE_2 and \overline{OE} features
- TTL-compatible inputs and outputs
- Automatic power down when deselected
- Available in non Pb-free 28-pin (300-Mil) Molded SOJ, 28-pin (300-Mil) Molded SOIC and Pb-free 28-pin (300-Mil) Molded DIP

Functional Description

The CY7C185^[1] is a high-performance CMOS static RAM organized as 8192 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{\text{CE}}_1$), an active HIGH chip enable ($\overline{\text{CE}}_2$), and active LOW output enable ($\overline{\text{OE}}$) and tri-state drivers. This device has an automatic power down feature ($\overline{\text{CE}}_1$ or $\overline{\text{CE}}_2$), reducing the power consumption by 70% when deselected. The CY7C185 is in a standard 300-mil-wide DIP, SOJ, or SOIC package.

An active LOW write enable signal (\overline{WE}) controls the writing/reading operation of the memory. When \overline{CE}_1 and \overline{WE} inputs are both LOW and CE_2 is HIGH, data on the eight data input/output pins (IO_0 through IO_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{12}). Reading the device is accomplished by selecting the device and enabling the outputs, \overline{CE}_1 and \overline{OE} active LOW, \overline{CE}_2 active HIGH, while \overline{WE} remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input or output pins.

The input or output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable (WE) is HIGH. A die coat is used to insure alpha immunity.



Pin Configurations

DID/SO I

	DIL	130	J	
	То	p Vi	ew	
NC A ₄ A ₅ A ₆ A ₇ A ₈ A ₉ A ₁₀ O ₀ IO ₁ IO ₂ GND	1 2 3 4 5 6 7 8 9 10 11 12 13		28 27 26 25 24 23 22 21 20 19 18 17 16 15	Vcc WE CE ₂ A ₃ A ₁ OE DO 6 DO 6 DO 6 DO 6

Selection Guide

Description	-15	-20	-35
Maximum Access Time (ns)	15	20	35
Maximum Operating Current (mA)	130	110	100
Maximum CMOS Standby Current (mA)	15	15	15

Note

^{1.} For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com.



Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature-65°C to +150°C

Ambient Temperature with

Power Applied –55°C to +125°C

Supply Voltage to Ground Potential.....-0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State $^{[2]}$-0.5V to +7.0V

DC Input Voltage^[2]-0.5V to +7.0V

Output Current into Outputs (LOW)......20 mA

Static Discharge Voltage	>2001V
(per MIL-STD-883, Method 3015)	
Latch-Up Current	>200 mA

Operating Range

Range	Ambient Temperature	V _{cc}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%

Electrical Characteristics

Over the Operating Range

			-	-15		-20		– 35	
Parameter	Description	Test Conditions	Min	Max	Min	Max	Min	Max	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.3V	2.2	V _{CC} + 0.3V	2.2	V _{CC} + 0.3V	V
V_{IL}	Input LOW Voltage ^[2]		-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I _{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	– 5	+5	– 5	+5	– 5	+5	μΑ
I _{OZ}	Output Leakage Current	$\begin{aligned} &\text{GND} \leq V_I \leq V_{CC}, \\ &\text{Output Disabled} \end{aligned}$	– 5	+5	– 5	+5	– 5	+5	μА
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA		130		110		100	mA
I _{SB1}	Automatic Power Down Current	$\begin{array}{l} \underline{\text{Ma}}\text{x. } V_{CC}, \\ CE_1 \geq V_{\text{IH}} \text{ or } CE_2 \leq V_{\text{IL}} \\ Min. \text{ Duty Cycle = 100\%} \end{array}$		40		20		20	mA
I _{SB2}	Automatic Power Down Current	$\begin{array}{l} \underline{\text{Max}}. \ V_{\text{CC}}, \\ \overline{\text{CE}}_1 \geq V_{\text{CC}} - 0.3\text{V}, \\ \text{or } \overline{\text{CE}}_2 \leq 0.3\text{V} \\ V_{\text{IN}} \geq V_{\text{CC}} - 0.3\text{V or} \\ V_{\text{IN}} \leq 0.3\text{V} \end{array}$		15		15		15	mA

Capacitance

Tested initially and after any design or process changes that may affect these parameters.

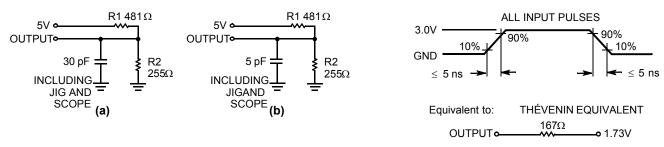
Parameter	Description	Test Conditions	Max	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz,	7	pF
C _{OUT}	Output Capacitance	$V_{CC} = 5.0V$	7	pF

Notes

- 2. Minimum voltage is equal to -3.0V for pulse durations less than 30 ns.
- 3. Tested initially and after any design or process changes that may affect these parameters.



Figure 1. AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range^[4]

		-	15	-2	20	-35		
Parameter	Description	Min	Max	Min	Max	Min	Max	Unit
Read Cycle								
t _{RC}	Read Cycle Time	15		20		35		ns
t _{AA}	Address to Data Valid		15		20		35	ns
t _{OHA}	Data Hold from Address Change	3		5		5		ns
t _{ACE1}	CE ₁ LOW to Data Valid		15		20		35	ns
t _{ACE2}	CE ₂ HIGH to Data Valid		15		20		35	ns
t _{DOE}	OE LOW to Data Valid		8		9		15	ns
t _{LZOE}	OE LOW to Low Z	3		3		3		ns
t _{HZOE}	OE HIGH to High Z ^[5]		7		8		10	ns
t _{LZCE1}	CE ₁ LOW to Low Z ^[6]	3		5		5		ns
t _{LZCE2}	CE ₂ HIGH to Low Z	3		3		3		ns
t _{HZCE}	CE ₁ HIGH to High Z ^[5, 6] CE ₂ LOW to High Z		7		8		10	ns
t _{PU}	CE ₁ LOW to Power Up CE ₂ to HIGH to Power Up	0		0		0		ns
t _{PD}	CE ₁ HIGH to Power Down CE ₂ LOW to Power Down		15		20		20	ns
Write Cycle ^[7]								
t _{WC}	Write Cycle Time	15		20		35		ns
t _{SCE1}	CE ₁ LOW to Write End	12		15		20		ns
t _{SCE2}	CE ₂ HIGH to Write End	12		15		20		ns
t _{AW}	Address Setup to Write End	12		15		25		ns
t _{HA}	Address Hold from Write End	0		0		0		ns
t _{SA}	Address Setup to Write Start	0		0		0		ns
t _{PWE}	WE Pulse Width	12		15		20		ns
t _{SD}	Data Setup to Write End	8		10		12		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t _{HZWE}	WE LOW to High Z ^[5]		7		7		8	ns
t _{LZWE}	WE HIGH to Low Z	3		5		5		ns

Notes

A. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified lo_L/_{IOH} and 30-pF load capacitance.
 t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
 At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE1} and t_{LZCE2} for any given device.
 The internal write time of the memory is defined by the overlap of CE₁ LOW, CE₂ HIGH, and WE LOW. All 3 signals must be active to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing must be referenced to the rising edge of the signal that terminates the write.



Switching Waveforms

Figure 2. Read Cycle No.1^[8,9]

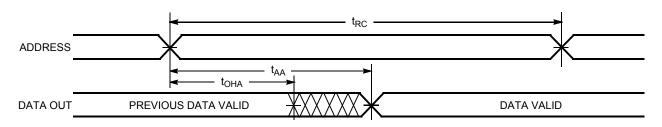
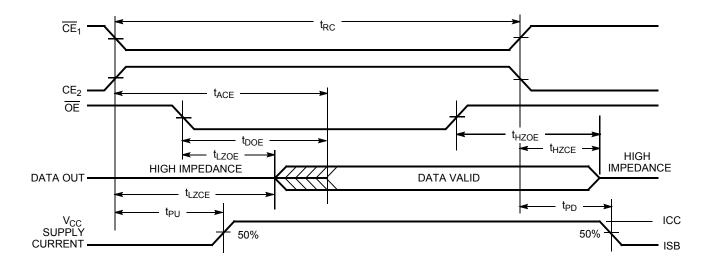


Figure 3. Read Cycle No.2^[10,11]



Document #: 38-05043 Rev. *D

<sup>Notes
8. Device is continuously selected. OE, CE₁ = V_{IL}. CE₂ = V_{IH}.
9. WE is HIGH for read cycle.
10. Data IO is High Z if OE = V_{II}, CE₁ = V_{IH}, WE = V_{IL}, or CE₂=V_{IL}.
11. The internal write time of the memory is defined by the overlap of CE₁ LOW, CE₂ HIGH and WE LOW. CE₁ and WE must be LOW and CE₂ must be HIGH to initiate write. A write can be terminated by CE₁ or WE going HIGH or CE₂ going LOW. The data input setup and hold timing must be referenced to the rising edge of the signal that terminates the write.</sup>



Switching Waveforms (continued)

Figure 4. Write Cycle No. 1 (WE Controlled)[9,11]

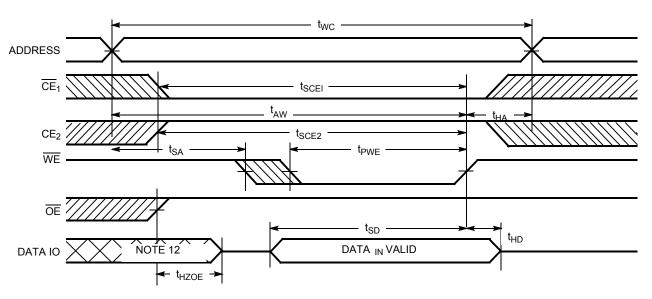
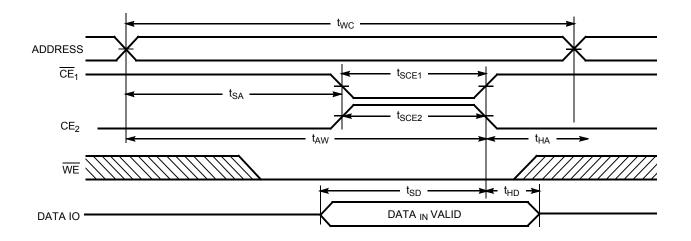


Figure 5. Write Cycle No. 2 (CE Controlled)[11,12,13]



Notes

Document #: 38-05043 Rev. *D

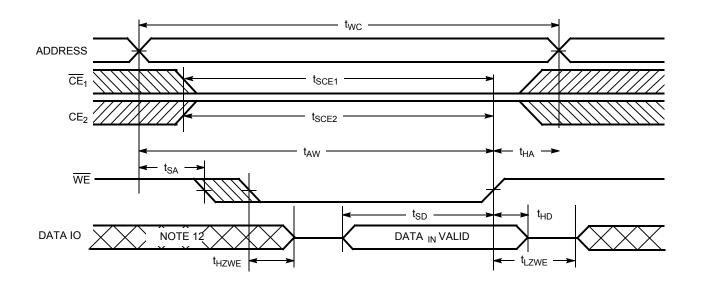
^{12.} During this period, the IOs are in the output state <u>and</u> input sign<u>als must</u> not be applied.

13. The minimum write cycle time for write cycle #3 (WE controlled, OE LOW) is the sum of t_{HZWE} and t_{SD}.



Switching Waveforms (continued)

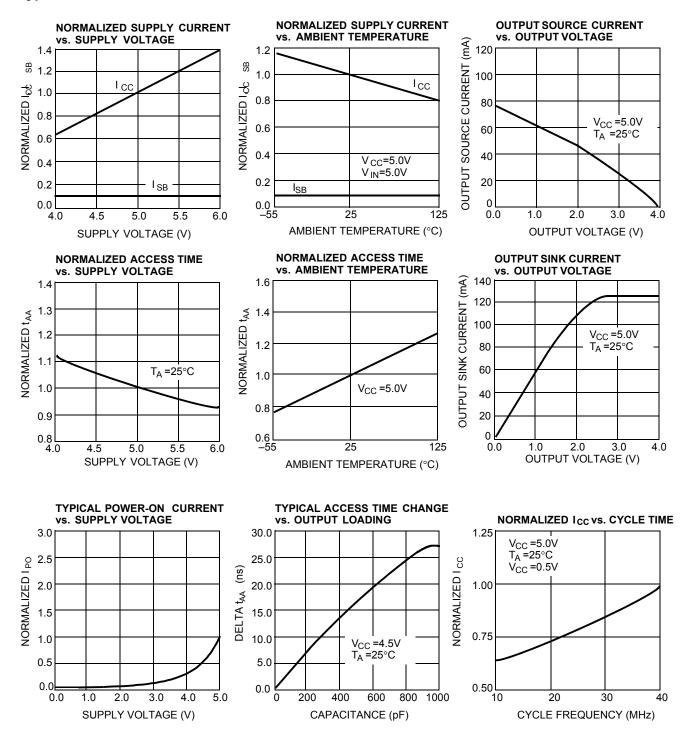
Figure 6. Write Cycle No. $3(\overline{WE} \text{ Controlled}, \overline{OE} \text{ LOW})^{[11,12,13,14]}$



 $[\]label{eq:Note_note} \begin{tabular}{l} \textbf{Note} \\ \textbf{14. If } \overline{\text{CE}}_1 \ \text{goes HIGH or CE}_2 \ \text{goes LOW simultaneously with } \overline{\text{WE HIGH, the output remains in a high-impedance state.} \\ \end{tabular}$



Typical DC and AC Characteristics





Truth Table

CE ₁	CE ₂	WE	OE	Input/Out- put	Mode
Н	Х	X	Х	High Z	Deselect/Power Down
Х	L	Х	Х	High Z	Deselect/Power Down
L	Н	Н	L	Data Out	Read
L	Н	L	Х	Data In	Write
L	Н	Н	Н	High Z	Deselect

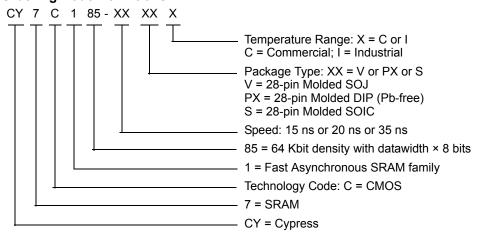
Address Designators

Address Name	Address Function	Pin Number
A4	X3	2
A5	X4	3
A6	X5	4
A7	X6	5
A8	X7	6
A9	Y1	7
A10	Y4	8
A11	Y3	9
A12	Y0	10
A0	Y2	21
A1	X0	23
A2	X1	24
A3	X2	25

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C185-15VI	51-85031	28-pin (300-Mil) Molded SOJ	Industrial
20	CY7C185-20PXC	51-85014	28-pin (300-Mil) Molded DIP (Pb-free)	Commercial
35	CY7C185-35SC	51-85026	28-pin (300-Mil) Molded SOIC	Commercial

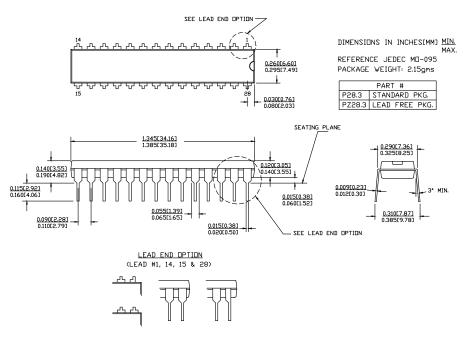
Ordering Code Definitions





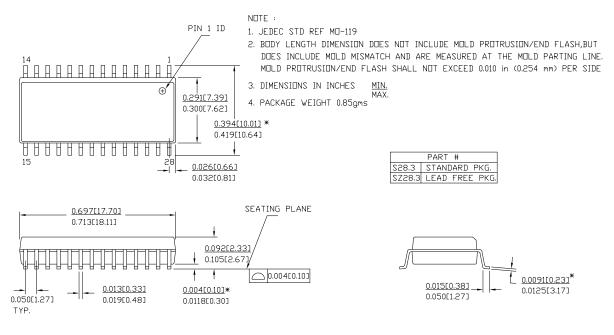
Package Diagrams

Figure 7. 28-pin (300-Mil) PDIP (51-85014)



51-85014 *E

Figure 8. 28-pin (300-Mil) Molded SOIC (51-85026)



51-85026 *E

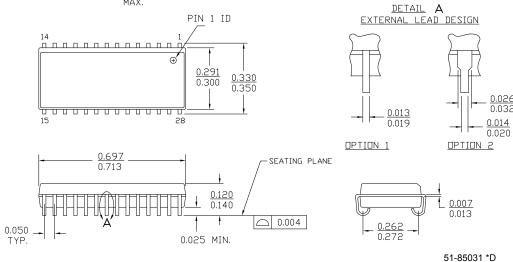


Package Diagrams (continued)

Figure 9. 28-pin (300-Mil) Molded SOJ (51-85031)

NOTE :

- 1. JEDEC STD REF MO088
- 2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.006 in (0.152 mm) PER SIDE
- 3. DIMENSIONS IN INCHES MIN. MAX.





Document History Page

	Document Title: CY7C185, 64-Kbit (8 K × 8) Static RAM Document Number: 38-05043						
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change			
**	107145	09/10/01	SZV	Change from Spec number: 38-00037 to 38-05043			
*A	116470	09/16/02	CEA	Add applications foot note to data sheet			
*B	486744	See ECN	NXR	Changed Low standby power from 220mW to 85mW Changed the description of I _{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed I _{OS} parameter from DC Electrical Characteristics table Updated the Ordering Information table			
*C	2263686	See ECN	VKN/AESA	Removed 25 ns speed bin Updated the Ordering Information table as per the current product offerings			
*D	3105329	12/09/2010	AJU	Added Ordering Code Definitions. Updated Package Diagrams.			



Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive cypress.com/go/automotive Clocks & Buffers cypress.com/go/clocks Interface cypress.com/go/interface Lighting & Power Control cypress.com/go/powerpsoc

cypress.com/go/plc
Memory cypress.com/go/memory
Optical & Image Sensing cypress.com/go/image
PSoC cypress.com/go/psoc
Touch Sensing cypress.com/go/touch
USB Controllers cypress.com/go/USB
Wireless/RF cypress.com/go/wireless

PSoC Solutions

psoc.cypress.com/solutions PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2001-2010. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

Document #: 38-05043 Rev. *D

Revised December 9, 2010

Page 12 of 12

All products and company names mentioned in this document may be the trademarks of their respective holders.