

# Double Data Rate (DDR) SDRAM

**MT46V32M4 – 8 Meg x 4 x 4 banks**
**MT46V16M8 – 4 Meg x 8 x 4 banks**
**MT46V8M16 – 2 Meg x 16 x 4 banks**

 For the latest data sheet revisions, please refer to the Micron® Web site: [www.micron.com/ddr2](http://www.micron.com/ddr2)

## Features

- VDD = +2.5V ±0.2V, VDDQ = +2.5V ±0.2V
- VDD = +2.6V ±0.1V, VDDQ = +2.6V ±0.1V (DDR 400)
- Bidirectional data strobe (DQS) transmitted/received with data, i.e., source-synchronous data capture (x16 has two – one per byte)
- Internal, pipelined double-data-rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- DLL to align DQ and DQS transitions with CK
- Four internal banks for concurrent operation
- Data mask (DM) for masking write data (x16 has two – one per byte)
- Programmable burst lengths: 2, 4, or 8
- Auto Refresh and Self Refresh Modes
- Longer lead TSOP for improved reliability (OCPL)
- 2.5V I/O (SSTL<sub>2</sub> compatible)
- Concurrent auto precharge option is supported
- <sup>t</sup>RAS lockout supported (<sup>t</sup>RAP = <sup>t</sup>RCD)

## Options

- Configuration
 

32 Meg x 4 (8 Meg x 4 x 4 banks)	32M4
16 Meg x 8 (4 Meg x 8 x 4 banks)	16M8
8 Meg x 16 (2 Meg x 16 x 4 banks)	8M16
- Plastic Package – OCPL
 

66-pin TSOP	TG
66-pin TSOP (lead-free) <sup>1</sup>	P
- Timing – Cycle Time
 

5ns @ CL = 3 (DDR400)	-5B
6ns @ CL = 2.5 (DDR333) <sup>2</sup>	-6T
7.5ns @ CL = 2 (DDR266)	-75E
7.5ns @ CL = 2 (DDR266A)	-75Z
7.5ns @ CL = 2.5 (DDR266B)	-75
- Self Refresh
 

Standard	None
Low Power Self Refresh	L
- Temperature Rating
 

Commercial (0°C to +70°C)	None
Industrial (-40°C to +85°C)	IT
- Revision
 

	:A
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## Marking

Notes: 1. Contact Micron for availability of lead-free products.  
2. Not available in x16 configuration.

**Table 1: Configuration Addressing**

	32 Meg x 4	16 Meg x 8	8 Meg x 16
Configuration	8 Meg x 4 x 4 banks	4 Meg x 8 x 4 banks	2 Meg x 16 x 4 banks
Refresh Count	4K	4K	4K
Row Addressing	4K (A0–A11)	4K (A0–A11)	4K (A0–A11)
Bank Addressing	4(BA0,BA1)	4(BA0,BA1)	4(BA0,BA1)
Column Addressing	2K(A0–A9,A11)	1K(A0–A9)	512(A0–A8)

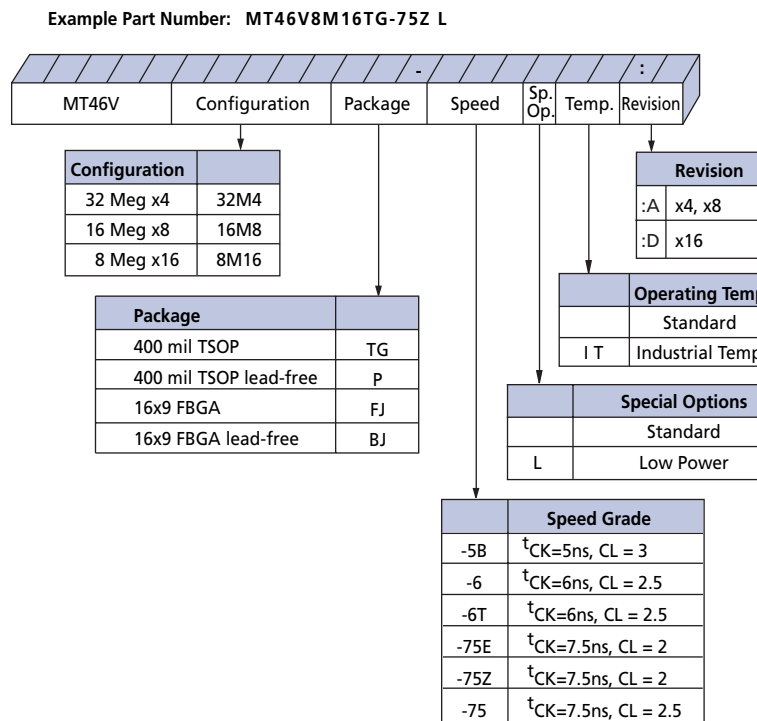
**Table 2: Key Timing Parameters**

CL = CAS (READ) latency; minimum clock rate @ CL = 2 (-75E, -75Z), CL = 2.5 (-6, -6T, -75), and CL = 3 (-5B).

Speed Grade	Clock Rate			Data-Out Window	Access Window	DQS–DQ Skew
	CL = 2	CL = 2.5	CL = 3			
-5B	133 MHz	167 MHz	200 MHz	1.6ns	±0.70ns	+0.40ns
-6	133 MHz	167 MHz	N/A	2.1ns	±0.70ns	+0.40ns
6T	133 MHz	167 MHz	N/A	2.0ns	±0.70ns	+0.45ns
-75E/75Z	133 MHz	133 MHz	N/A	2.5ns	±0.75ns	+0.50ns
-75	100 MHz	133 MHz	N/A	2.5ns	±0.75ns	+0.50ns

**Table 3: Speed Grade Compatibility**

Marking	PC3200 (3-3-3)	PC2700 (2.5-3-3)	PC2100 (2-2-2)	PC2100 (2-3-3)	PC2100 (2.5-3-3)	PC1600 (2-2-2)
-5B	Yes	Yes	Yes	Yes	Yes	Yes
-6		Yes	Yes	Yes	Yes	Yes
-6T		Yes	Yes	Yes	Yes	Yes
-75E			Yes	Yes	Yes	Yes
-75Z				Yes	Yes	Yes
-75					Yes	Yes
	<b>-5B</b>	<b>-6/-6T</b>	<b>-75E</b>	<b>-75Z</b>	<b>-75</b>	<b>-75</b>

**Figure 1: 128Mb DDR SDRAM Part Numbers**


Note: Not all speeds and all configurations are available in all packages.

## General Description

The 128Mb DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 134,217,728 bits. It is internally configured as a quad-bank DRAM.

The 128Mb DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a  $2n$ -prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 128Mb DDR SDRAM effectively consists of a single  $2n$ -bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding  $n$ -bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs. The x16 offering has two data strobes, one for the lower byte and one for the upper byte.

The 128Mb DDR SDRAM operates from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The DDR SDRAM provides for programmable READ or WRITE burst lengths of 2, 4, or 8 locations. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

As with standard SDR SDRAMs, the pipelined, multibank architecture of DDR SDRAMs allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL\_2. All full drive option outputs are SSTL\_2, Class II compatible.

- Notes:
1. The functionality and the timing specifications discussed in this data sheet are for the DLL-enabled mode of operation.
  2. Throughout the data sheet, the various figures and text refer to DQs as "DQ." The DQ term is to be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, the x16 is divided into two bytes, the lower byte and upper byte. For the lower byte (DQ0 through DQ7) DM refers to LDM and DQS refers to LDQS. For the upper byte (DQ8 through DQ15) DM refers to UDM and DQS refers to UDQS.
  3. Complete functionality is described throughout the document and any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
  4. Any specific requirement takes precedence over a general statement.

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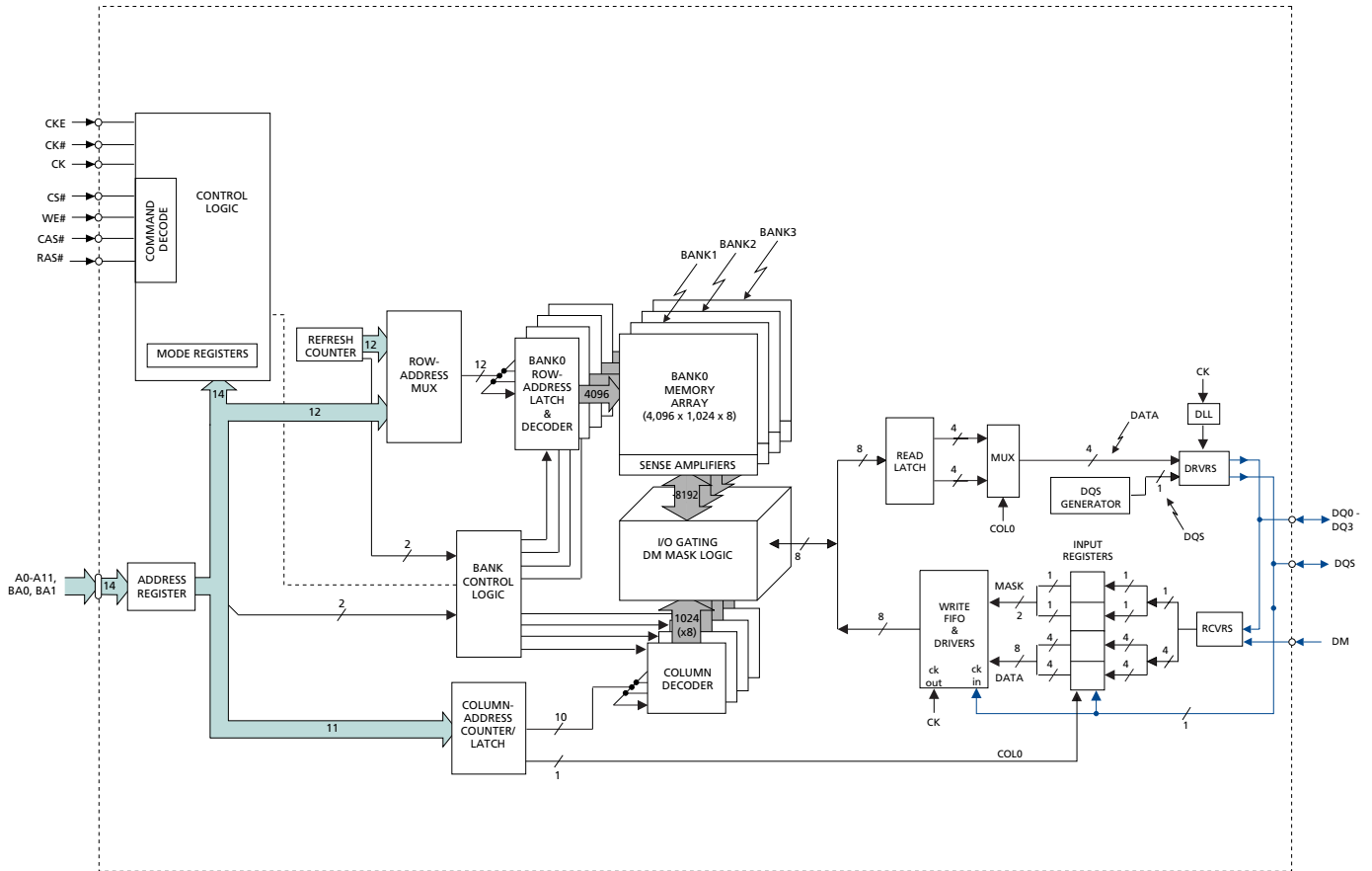
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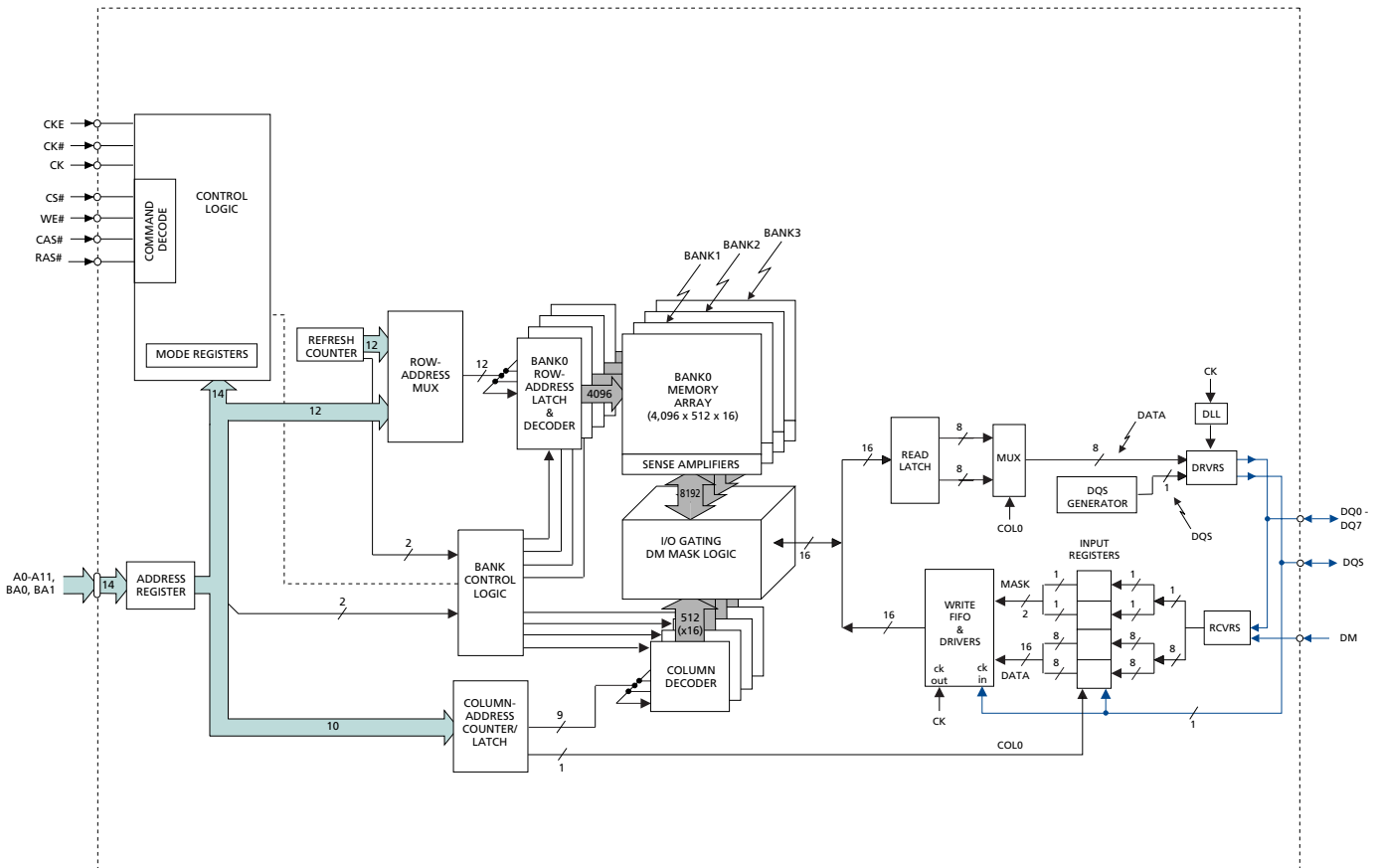
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## Functional Block Diagrams

Figure 2: Functional Block Diagram 32 Meg x 4

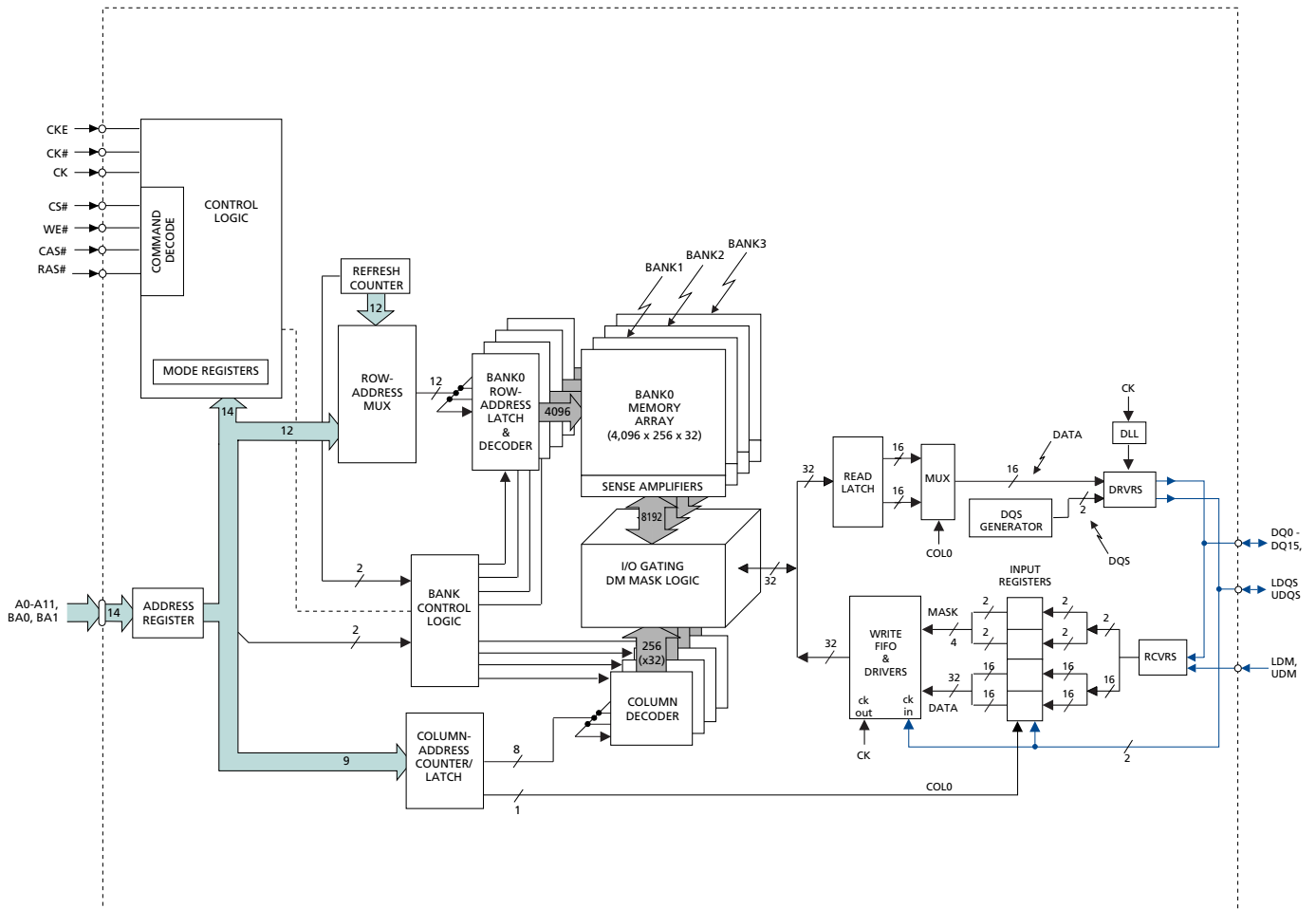


**Figure 3: Functional Block Diagram 16 Meg x 8**





**Figure 4: Functional Block Diagram 8 Meg x 16**



## Ball/Pin Descriptions and Assignments

**Table 4: Ball/Pin Descriptions**

FBGA Numbers	TSOP Numbers	Symbol	Type	Description
G2, G3	45, 46	CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQ and DQS) is referenced to the crossings of CK and CK#.
H3	44	CKE	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any bank). CKE is synchronous for POWER-DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, CK# and CKE) are disabled during POWER-DOWN. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after V <sub>DD</sub> is applied and until CKE is first brought HIGH, after which it becomes a SSTL_2 input only.
H8	24	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
H7, G8, G7	23, 22, 21	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS#, and WE# (along with CS#) define the command being entered.
3F	47 20, 47	DM LDM, UDM	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins. For the x16, LDM is DM for DQ0–DQ7 and UDM is DM for DQ8–DQ15. Pin 20 is a NC on x4 and x8.
J8, J7	26, 27	BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
K7, L8, L7, M8, M2, L3, L2, K3, K2, J3, K8, J2	29, 30, 31, 32, 35, 36, 37, 38, 39, 40, 28 41	A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/ WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command. BA0 and BA1 define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.

**Table 4: Ball/Pin Descriptions (Continued)**

FBGA Numbers	TSOP Numbers	Symbol	Type	Description
	2, 4, 5, 7, 8, 10, 11, 13, 54, 56, 57, 59, 60, 62, 63, 65	DQ0–DQ2 DQ3–DQ5 DQ6–DQ8 DQ9–DQ11 DQ12–DQ14 DQ15	I/O	Data Input/Output: Data bus for <b>x16</b>
	14, 17, 25, 42, 43, 53	NC	–	No Connect for <b>x16</b> These pins should be left unconnected.
A8, B7, C7, D7, D3, C3, B3, A2	2, 5, 8, 11, 56, 59, 62, 65	DQ0–DQ2 DQ3–DQ5 DQ6, DQ7	I/O	Data Input/Output: Data bus for <b>x8</b>
B1, B9, C1, C9, D1, D9, E1, E7, E9, F7, H2	4, 7, 10, 13, 14, 16, 17, 20, 25, 42, 43, 53, 54, 57, 60, 63,	NC	–	No Connect for <b>x8</b> These pins should be left unconnected.
B7, D7, D3, B3	5, 11, 56, 62	DQ0–DQ2 DQ3	I/O	Data Input/Output: Data bus for <b>x4</b>
A2, A8, B1, B9, C1, C3, C7, C9, D1, D9, E1, E7, E9, F7, H2	2, 4, 7, 8, 10, 13, 14, 16, 17, 20, 25, 42, 43, 53, 54, 57, 59, 60, 63, 65	NC	–	No Connect for <b>x4</b> These pins should be left unconnected.
E3	51 16 51	DQS LDQS UDQS	I/O	Data Strobe: Output with read data, input with write data. DQS is edge-aligned with read data, centered in write data. It is used to capture data. For the x16, LDQS is DQS for DQ0–DQ7 and UDQS is DQS for DQ8–DQ15. Pin 16 (E7) is NC on x4 and x8.
F9	19, 50	DNU	–	Do Not Use: Must float to minimize noise on VREF.
B2, D2, C8, E8, A9	3, 9, 15, 55, 61	VDDQ	Supply	DQ Power Supply: +2.5 ±0.2V (+2.6V ±0.1V for DDR400). Isolated on the die for improved noise immunity.
A1, C2, E2, B8, D8	6, 12, 52, 58, 64	VSSQ	Supply	DQ Ground. Isolated on the die for improved noise immunity.
F8, M7, A7	1, 18, 33	VDD	Supply	Power Supply: +2.5V ±0.2V (+2.6V ±0.1V for DDR400).
A3, F2, M3	34, 48, 66	VSS	Supply	Ground.
F1	49	VREF	Supply	SSTL_2 reference voltage.

**Table 5: Reserved NC Balls and Pins**

NC pins not listed may also be reserved for other uses; this table defines NC pins of importance

FBGA NUMBERS	TSOP NUMBERS	SYMBOL	TYPE	DESCRIPTION
H2, F9	42, 17	A12, A13	I	Address inputs A12 and A13 for 256Mb, 512Mb and 1Gb devices. DNU for FBGA.

**Figure 5: Pin Assignment (Top View) 66-pin TSOP**

x4	x8	x16				x16	x8	x4
VDD	VDD	VDD	1	•	66	Vss	Vss	Vss
NC	DQ0	DQ0	2		65	DQ15	DQ7	NC
VDDQ	VDDQ	VDDQ	3		64	VssQ	VssQ	VssQ
NC	NC	DQ1	4		63	DQ14	NC	NC
DQ0	DQ1	DQ2	5		62	DQ13	DQ6	DQ3
VssQ	VssQ	VssQ	6		61	VDDQ	VDDQ	VDDQ
NC	NC	DQ3	7		60	DQ12	NC	NC
NC	DQ2	DQ4	8		59	DQ11	DQ5	NC
VDDQ	VDDQ	VDDQ	9		58	VssQ	VssQ	VssQ
NC	NC	DQ5	10		57	DQ10	NC	NC
DQ1	DQ3	DQ6	11		56	DQ9	DQ4	DQ2
VssQ	VssQ	VssQ	12		55	VDDQ	VDDQ	VDDQ
NC	NC	DQ7	13		54	DQ8	NC	NC
NC	NC	NC	14		53	NC	NC	NC
VDDQ	VDDQ	VDDQ	15		52	VssQ	VssQ	VssQ
NC	NC	LDQS	16		51	UDQS	DQS	DQS
NC	NC	NC	17		50	DNU	DNU	DNU
VDD	VDD	VDD	18		49	VREF	VREF	VREF
DNU	DNU	DNU	19		48	Vss	Vss	Vss
NC	NC	LDM	20		47	UDM	DM	DM
WE#	WE#	WE#	21		46	CK#	CK#	CK#
CAS#	CAS#	CAS#	22		45	CK	CK	CK
RAS#	RAS#	RAS#	23		44	CKE	CKE	CKE
CS#	CS#	CS#	24		43	NC	NC	NC
NC	NC	NC	25		42	NC	NC	NC
BA0	BA0	BA0	26		41	A11	A11	A11
BA1	BA1	BA1	27		40	A9	A9	A9
A10/AP	A10/AP	A10/AP	28		39	A8	A8	A8
A0	A0	A0	29		38	A7	A7	A7
A1	A1	A1	30		37	A6	A6	A6
A2	A2	A2	31		36	A5	A5	A5
A3	A3	A3	32		35	A4	A4	A4
VDD	VDD	VDD	33		34	Vss	Vss	Vss

**Figure 6: Ball Assignment (Top View) 60-Ball FBGA**

x4 (Top View)

1	2	3	4	5	6	7	8	9
V <sub>SSQ</sub>	NC	V <sub>SS</sub>	● A ●			V <sub>DD</sub>	NC	V <sub>DDQ</sub>
NC	V <sub>DDQ</sub>	DQ3	● B ●			DQ0	V <sub>SSQ</sub>	NC
NC	V <sub>SSQ</sub>	NC	● C ●			NC	V <sub>DDQ</sub>	NC
NC	V <sub>DDQ</sub>	DQ2	● D ●			DQ1	V <sub>SSQ</sub>	NC
NC	V <sub>SSQ</sub>	DQS	● E ●			NC	V <sub>DDQ</sub>	NC
V <sub>REF</sub>	V <sub>SS</sub>	DM	● F ●			NC	V <sub>DD</sub>	DNU
	CK	CK#	● G ●			WE#	CAS#	
	NC	CKE	● H ●			RAS#	CS#	
	A11	A9	● J ●			BA1	BA0	
	A8	A7	● K ●			A0	A10	
	A6	A5	● L ●			A2	A1	
	A4	V <sub>SS</sub>	● M ●			V <sub>DD</sub>	A3	

x8 (Top View)

1	2	3	4	5	6	7	8	9
V <sub>SSQ</sub>	DQ7	V <sub>SS</sub>	● A ●			V <sub>DD</sub>	DQ0	V <sub>DDQ</sub>
NC	V <sub>DDQ</sub>	DQ6	● B ●			DQ1	V <sub>SSQ</sub>	NC
NC	V <sub>SSQ</sub>	DQ5	● C ●			DQ2	V <sub>DDQ</sub>	NC
NC	V <sub>DDQ</sub>	DQ4	● D ●			DQ3	V <sub>SSQ</sub>	NC
NC	V <sub>SSQ</sub>	DQS	● E ●			NC	V <sub>DDQ</sub>	NC
V <sub>REF</sub>	V <sub>SS</sub>	DM	● F ●			NC	V <sub>DD</sub>	DNU
	CK	CK#	● G ●			WE#	CAS#	
	NC	CKE	● H ●			RAS#	CS#	
	A11	A9	● J ●			BA1	BA0	
	A8	A7	● K ●			A0	A10	
	A6	A5	● L ●			A2	A1	
	A4	V <sub>SS</sub>	● M ●			V <sub>DD</sub>	A3	

## Functional Description

The 128Mb DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 134,217,728 bits. The 128Mb DDR SDRAM is internally configured as a quad-bank DRAM.

The 128Mb DDR SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a  $2n$ -prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the 128Mb DDR SDRAM consists of a single  $2n$ -bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding  $n$ -bit wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses to the DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A11 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the DDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions, and device operation.

## Initialization

DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power must first be applied to VDD and VDDQ simultaneously, and then to VREF (and to the system VTT). VTT must be applied after VDDQ to avoid device latch-up, which may cause permanent damage to the device. VREF can be applied any time after VDDQ but is expected to be nominally coincident with VTT. Except for CKE, inputs are not recognized as valid until after VREF is applied. CKE is an SSTL\_2 input but will detect an LVCMOS LOW level after VDD is applied. After CKE passes through VIH, it will transition to a SSTL 2 signal and remain as such until power is cycled. Maintaining an LVCMOS LOW level on CKE during power-up is required to ensure that the DQ and DQS outputs will be in the High-Z state, where they will remain until driven in normal operation (by a read access). After all power supply and reference voltages are stable, and the clock is stable, the DDR SDRAM requires a 200 $\mu$ s delay prior to applying an executable command.

Once the 200 $\mu$ s delay has been satisfied, a DESELECT or NOP command should be applied, and CKE should be brought HIGH. Following the NOP command, a PRE-CHARGE ALL command should be applied. Next a LOAD MODE REGISTER command should be issued for the extended mode register (BA1 LOW and BA0 HIGH) to enable the DLL, followed by another LOAD MODE REGISTER command to the mode register (BA0/BA1 both LOW) to reset the DLL and to program the operating parameters. Two-hundred clock cycles are required between the DLL reset and any READ command. A PRE-CHARGE ALL command should then be applied, placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed (<sup>4</sup>RFC must be satisfied.) Additionally, a LOAD MODE REGISTER command for the mode register with the reset DLL bit deactivated (i.e., to program operating parameters without resetting the DLL) is required. Following these requirements, the DDR SDRAM is ready for normal operation.

## Register Definition

### Mode Register

The mode register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency and an operating mode, as shown in Figure 7 on page 16. The mode register is programmed via the MODE REGISTER SET command (with BA0 = 0 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

Reprogramming the mode register will not alter the contents of the memory, provided it is performed correctly. The mode register must be loaded (reloaded) when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Mode register bits A0-A2 specify the burst length, A3 specifies the type of burst (sequential or interleaved), A4-A6 specify the CAS latency, and A7-A11 specify the operating mode.

### Burst Length

Read and write accesses to the DDR SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 7. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

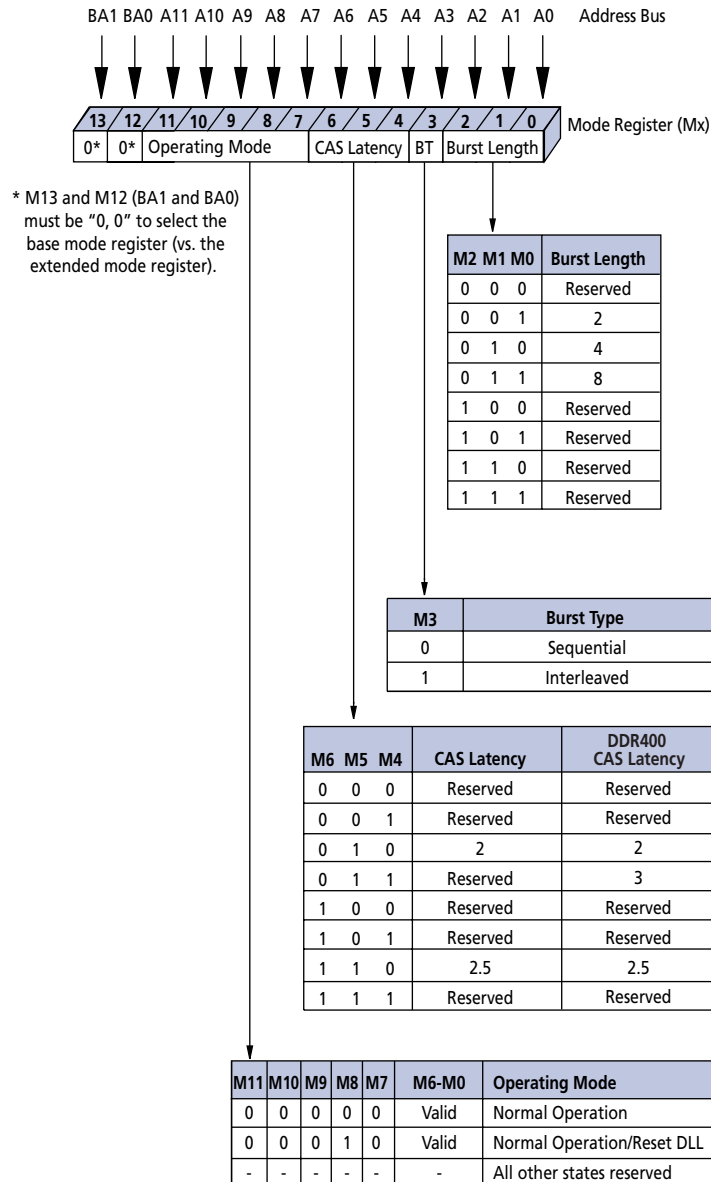
When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1-A<sub>i</sub> when the burst length is set to two, by A2-A<sub>i</sub> when the burst length is set to four and by A3-A<sub>i</sub> when the burst length is set to eight (where A<sub>i</sub> is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

### Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 6, Burst Definition, on page 17.

**Figure 7: Mode Register Definition**





**Table 6: Burst Definition**

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2	<b>A0</b>				
	0			0-1	0-1
	1			1-0	1-0
4	<b>A1</b>		<b>A0</b>		
	0		0	0-1-2-3	0-1-2-3
	0		1	1-2-3-0	1-0-3-2
	1		0	2-3-0-1	2-3-0-1
	1		1	3-0-1-2	3-2-1-0
8	<b>A2</b>	<b>A1</b>	<b>A0</b>		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

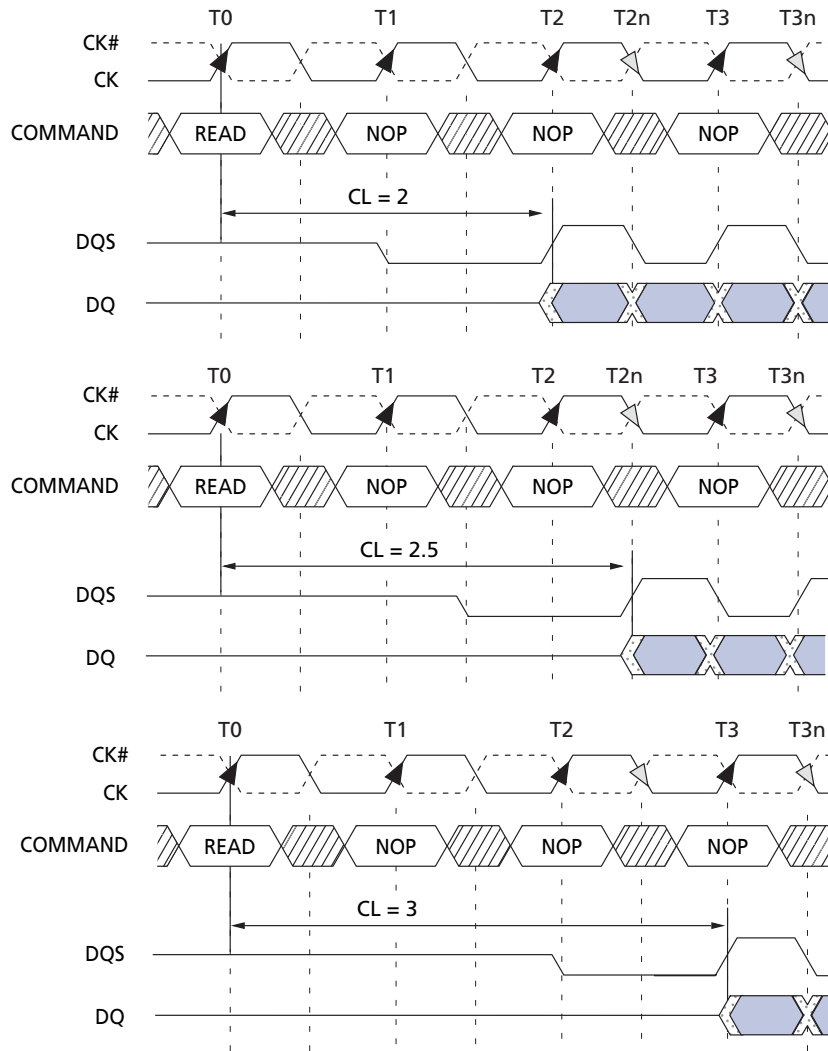
- Notes:
- Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
  - For a burst length of two, A1-A<sub>i</sub> select the two- data-element block; A0 selects the first access within the block.
  - For a burst length of four, A2-A<sub>i</sub> select the four- data-element block; A0-A1 select the first access within the block.
  - For a burst length of eight, A3-A<sub>i</sub> select the eight- data-element block; A0-A2 select the first access within the block.

## Read Latency

The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 2, 2.5, or 3 (DDR400 only) clocks, as shown in Figure 8.

If a READ command is registered at clock edge  $n$ , and the latency is  $m$  clocks, the data will be available nominally coincident with clock edge  $n + m$ . Table 7, CAS Latency (CL), on page 18 indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

**Figure 8: CAS Latency**


Burst Length = 4 in the cases shown  
Shown with nominal  $t_{AC}$ ,  $t_{DQSK}$ , and  $t_{DQSQ}$

TRANSITIONING DATA    DON'T CARE

**Table 7: CAS Latency (CL)**

Speed	Allowable Operating Clock Frequency (MHz)		
	CL = 2	CL = 2.5	CL = 3
-5B	$75 \leq f \leq 133$	$75 \leq f \leq 167$	$133 \leq f \leq 200$
-6/-6T	$75 \leq f \leq 133$	$75 \leq f \leq 167$	–
-75E	$75 \leq f \leq 133$	$75 \leq f \leq 133$	–
-75Z	$75 \leq f \leq 133$	$75 \leq f \leq 133$	–
-75	$75 \leq f \leq 100$	$75 \leq f \leq 133$	–

## Operating Mode

The normal operating mode is selected by issuing a MODE REGISTER SET command with bits A7-A11 each set to zero, and bits A0-A6 set to the desired values. A DLL reset is initiated by issuing a MODE REGISTER SET command with bits A7 and A9-A11 each set to zero, bit A8 set to one, and bits A0-A6 set to the desired values. Although not required by the Micron device, JEDEC specifications recommend when a LOAD MODE REGISTER command is issued to reset the DLL, it should always be followed by a LOAD MODE REGISTER command to select normal operating mode.

All other combinations of values for A7-A11 are reserved for future use and/or test modes. Test modes and reserved states should not be used, as unknown operation or incompatibility with future versions may result.

## Extended Mode Register

The extended mode register controls functions beyond those controlled by the mode register; these additional functions are DLL enable/disable, and output drive strength. These functions are controlled via the bits shown in Figure 9. The extended mode register is programmed via the LOAD MODE REGISTER command to the mode register (with BA0 = 1 and BA1 = 0) and will retain the stored information until it is programmed again or the device loses power. The enabling of the DLL should always be followed by a LOAD MODE REGISTER command to the mode register (BA0/BA1 both LOW) to reset the DLL. The extended mode register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before initiating any subsequent operation. Violating either of these requirements could result in unspecified operation.

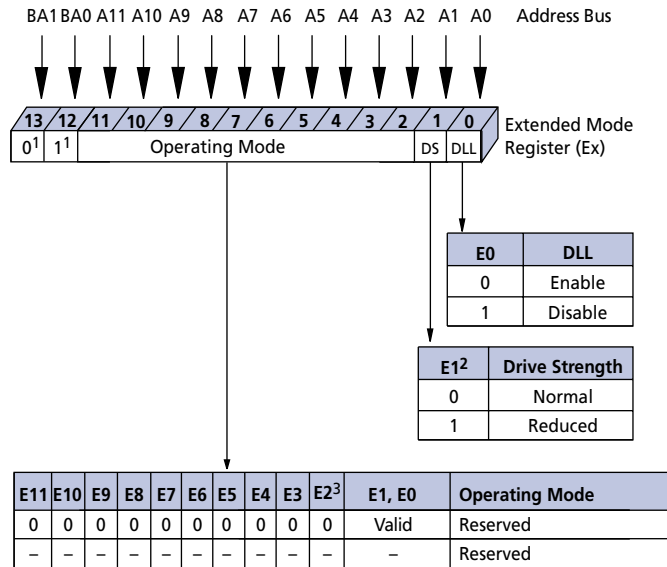
## Output Drive Strength

The normal drive strength for all outputs are specified to be SSTL2, Class II. The x16 supports a programmable option for reduced drive. This option is intended for the support of the lighter load and/or point-to-point environments. The selection of the reduced drive strength will alter the DQ pins and DQS pins from SSTL2, Class II drive strength to a reduced drive strength, which is approximately 54 percent of the SSTL2, Class II drive strength.

## DLL Enable/Disable

When the part is running without the DLL enabled, device functionality may be altered. The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disabled the DLL for the purpose of debug or evaluation. (When the device exits self refresh mode, the DLL is enabled automatically.) Any time the DLL is enabled, 200 clock cycles must occur before a READ command can be issued.

**Figure 9: Extended Mode Register Definition**



- Notes:
1. E13 and E12 (BA1 and BA0) must be “0, 1” to select the Extended Mode Register vs. the base Mode Register.
  2. The reduced drive strength option is not supported on the x4 and x8 versions, and is only available on the x16 version.
  3. The QFC# option is not supported.

## Commands

Table 8 and Table 9 provide a quick reference of available commands. This is followed by a verbal description of each command. Two additional Truth Tables, Table 11 on page 50, and Table 12 on page 52, appear following the Operation section, provide current state/next state information.

**Table 8: Truth Table – Commands**  
Notes 1 and 10 apply to all commands

Name (Function)	CS#	RAS#	CAS#	WE#	Addr	Notes
DESELECT (NOP)	H	X	X	X	X	9
NO OPERATION (NOP)	L	H	H	H	X	9
ACTIVE (Select bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
BURST TERMINATE	L	H	H	L	X	8
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	6, 7
LOAD MODE REGISTER	L	L	L	L	Op-Code	2

- Notes:
1. CKE is HIGH for all commands shown except SELF REFRESH.
  2. BA0-BA1 select either the mode register or the extended mode register (BA0 = 0, BA1 = 0 select the mode register; BA0 = 1, BA1 = 0 select extended mode register; other combinations of BA0-BA1 are reserved). A0-A11 provide the op-code to be written to the selected mode register.
  3. BA0-BA1 provide bank address and A0-A11 provide row address.
  4. BA0-BA1 provide bank address; A0-A<sub>i</sub> provide column address, (where  $i=8$  for x16,  $i=9$  for x8, and  $i=9, 11$  for x4) A10 HIGH enables the auto precharge feature (non persistent), and A10 LOW disables the auto precharge feature.
  5. A10 LOW: BA0-BA1 determine which bank is precharged.  
A10 HIGH: all banks are precharged and BA0-BA1 are "Don't Care."
  6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
  7. Internal refresh counter controls row addressing; for within the Self Refresh mode all inputs and I/Os are "Don't Care" except for CKE.
  8. Applies only to read bursts with auto precharge disabled; this command is undefined (and should not be used) for read bursts with auto precharge enabled and for write bursts.
  9. Deselect and NOP are functionally interchangeable.
  10. All states and sequences not shown are illegal or reserved.

**Table 9: Truth Table – DM Operation**  
Note 1 applies to all commands

Name (Function)	DM	DQ
Write Enable	L	Valid
Write Inhibit	H	X

- Notes:
1. Used to mask write data; provided coincident with the corresponding data.

## DESELECT

The Deselect function (CS# HIGH) prevents new commands from being executed by the DDR SDRAM. The DDR SDRAM is effectively deselected. Operations already in progress are not affected.

## NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct the selected DDR SDRAM to perform a NOP (CS# is LOW with RAS#, CAS#, and WE# are HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

## LOAD MODE REGISTER

The mode registers are loaded via inputs A0–A11. See mode register descriptions in the Register Definition section. The LOAD MODE REGISTER command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until  $t^{\text{MRD}}$  is met.

## ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A11 selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank. A precharge command must be issued before opening a different row in the same bank.

## READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A $i$  (where  $i = 8$  for x16, 9 for x8, or 9, 11 for x4) selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

## WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–A $i$  (where  $i = 8$  for x16, 9 for x8, or 9, 11 for x4) selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQ is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW, the corresponding data will be written to memory; if the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

## PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time ( $t^{\text{RP}}$ ) after the precharge command is issued. Except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate

any other timing parameters. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank (idle state), or if the previously open row is already in the process of precharging.

## Auto Precharge

Auto precharge is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. Auto precharge is nonpersistent in that it is either enabled or disabled for each individual Read or Write command. This device supports concurrent auto precharge if the command to the other bank does not interrupt the data transfer to the current bank.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. This “earliest valid stage” is determined as if an explicit PRECHARGE command was issued at the earliest possible time, without violating  $t^{\text{RAS}}$  (MIN), as described for each burst type in the Operation section of this data sheet. The user must not issue another command to the same bank until the precharge time ( $t^{\text{RP}}$ ) is completed.

## BURST TERMINATE

The BURST TERMINATE command is used to truncate read bursts (with auto precharge disabled). The most recently registered READ command prior to the BURST TERMINATE command will be truncated, as shown in the Operation section of this data sheet. The open page which the READ burst was terminated from remains open.

## AUTO REFRESH

AUTO REFRESH is used during normal operation of the DDR SDRAM and is analogous to CAS#-BEFORE-RAS# (CBR) refresh in FPM/EDO DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required. All banks must be idle before an AUTO REFRESH command is issued.

The addressing is generated by the internal refresh controller. This makes the address bits a “Don’t Care” during an AUTO REFRESH command. The 128Mb DDR SDRAM requires AUTO REFRESH cycles at an average interval of 15.625 $\mu$ s (maximum).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM, meaning that the maximum absolute interval between any AUTO REFRESH command and the next AUTO REFRESH command is 9 x 15.625 $\mu$ s (140.6 $\mu$ s). Note the JEDEC specifications only allows 8 x 15.625 $\mu$ s, thus the Micron specification exceeds the JEDEC requirement by one clock. This maximum absolute interval is to allow future support for DLL updates internal to the DDR SDRAM to be restricted to AUTO REFRESH cycles, without allowing excessive drift in  $t^{\text{AC}}$  between updates.

Although not a JEDEC requirement, to provide for future functionality features, CKE must be active (High) during the AUTO REFRESH period. The AUTO REFRESH period begins when the AUTO REFRESH command is registered and ends  $t^{\text{RFC}}$  later.

## SELF REFRESH

The SELF REFRESH command can be used to retain data in the DDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the DDR SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). The DLL is automatically disabled upon entering SELF REFRESH and is automatically enabled upon exiting SELF REFRESH (200 clock cycles must then occur before a READ command can be issued). Input signals except CKE are “Don’t Care” during SELF REFRESH. VREF voltage is also required for full duration of the SELF REFRESH cycle.

The procedure for exiting self refresh requires a sequence of commands. First, CK and CK# must be stable prior to CKE going back HIGH. Once CKE is HIGH, the DDR SDRAM must have NOP commands issued for  $t_{XSNR}$  because time is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh and DLL requirements is to apply NOPs for  $t_{XSNR}$  time, then a DLL Reset and NOPs for 200 additional clock cycles before applying any other command.



## Operations

### Bank/Row Activation

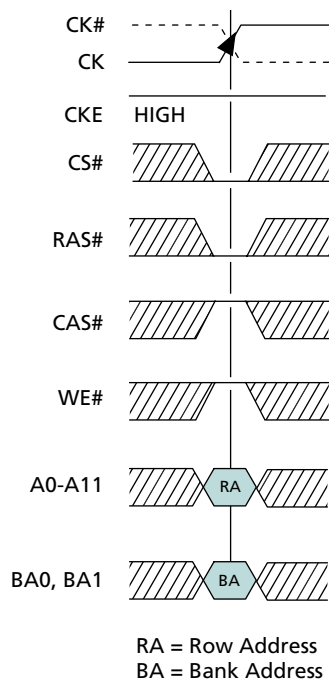
Before any READ or WRITE commands can be issued to a bank within the DDR SDRAM, a row in that bank must be “opened.” This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated, as shown in Figure 10.

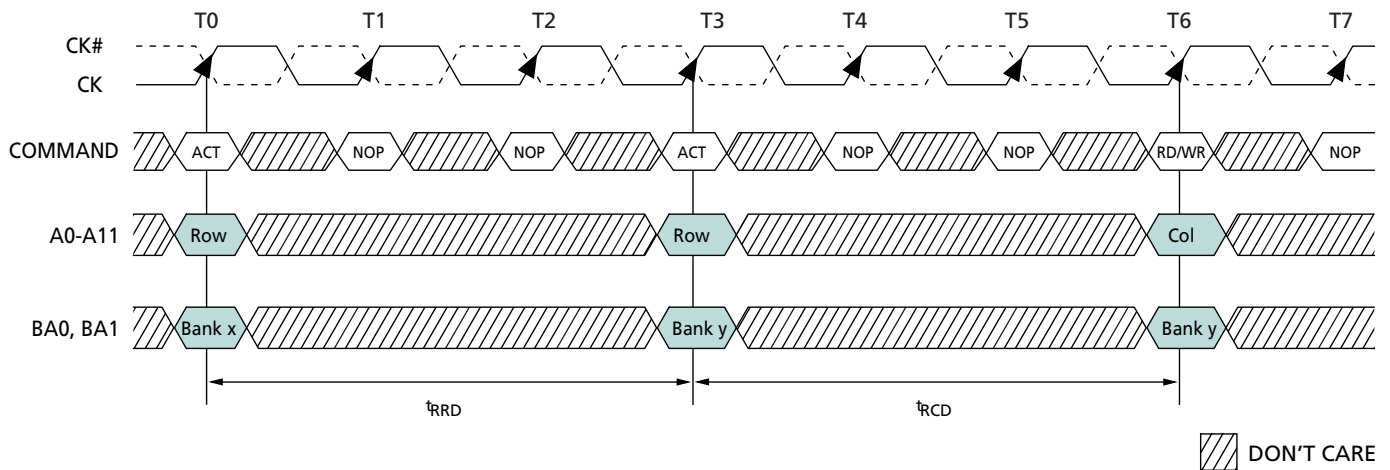
After a row is opened with an ACTIVE command, a READ or WRITE command may be issued to that row, subject to the  $t_{RCD}$  specification.  $t_{RCD} (MIN)$  should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a  $t_{RCD}$  specification of 20ns with a 133 MHz clock (7.5ns period) results in 2.7 clocks rounded to 3. This is reflected in Figure 11, which covers any case where  $2 < t_{RCD} (MIN) / t_{CK} \leq 3$ . (Figure 11 also shows the same case for  $t_{RCD}$ ; the same procedure is used to convert other specification limits from time units to clock cycles).

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been “closed” (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by  $t_{RC}$ .

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by  $t_{RRD}$ .

**Figure 10: Activating a Specific Row in a Specific Bank**



**Figure 11: Example: Meeting  $t_{RCD}$  ( $t_{RRD}$ ) MIN When  $2 < t_{RCD}$  ( $t_{RRD}$ ) MIN/ $t_{CK} \leq 3$** 


## READs

READ bursts are initiated with a READ command, as shown in Figure 12 on page 27. The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst.

**Note:** For the READ commands used in the following illustrations, auto precharge is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge (i.e., at the next crossing of CK and CK#). Figure 13 on page 28 shows general timing for each possible CAS latency setting. DQS is driven by the DDR SDRAM along with output data. The initial LOW state on DQS is known as the read preamble; the LOW state coincident with the last data-out element is known as the read postamble.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z. A detailed explanation of  $t_{DQSQ}$  (valid data-out skew),  $t_{QH}$  (data-out window hold), the valid data window are depicted in Figure 40 on page 77 and Figure 41 on page 78. A detailed explanation of  $t_{DQSCK}$  (DQS transition skew to CK) and  $t_{AC}$  (data-out transition skew to CK) is depicted in Figure 42 on page 79.

Data from any READ burst may be concatenated with or truncated with data from a subsequent READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new READ command should be issued  $x$  cycles after the first READ command, where  $x$  equals the number of desired data element pairs (pairs are required by the 2n-prefetch architecture). This is shown in Figure 14 on page 29. A READ command can be initiated on any clock cycle following a previous READ command. Nonconsecutive read data is shown for illustration in Figure 15 on page 30. Full-speed random read accesses within a page (or pages) can be performed as shown in Figure 16 on page 31.

Data from any READ burst may be truncated with a BURST TERMINATE command, as shown in Figure 17 on page 32. The BURST TERMINATE latency is equal to the read (CAS) latency, i.e., the BURST TERMINATE command should be issued x cycles after the READ command, where x equals the number of desired data element pairs (pairs are required by the 2n-prefetch architecture).

Data from any READ burst must be completed or truncated before a subsequent WRITE command can be issued. If truncation is necessary, the BURST TERMINATE command must be used, as shown in Figure 18 on page 33. The <sup>t</sup>DQSS (NOM) case is shown; the <sup>t</sup>DQSS (MAX) case has a longer bus idle time. (<sup>t</sup>DQSS [MIN] and <sup>t</sup>DQSS [MAX] are defined in the section on WRITES.)

A READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank provided that auto precharge was not activated.

The PRECHARGE command should be issued x cycles after the READ command, where x equals the number of desired data element pairs (pairs are required by the 2n-prefetch architecture). This is shown in Figure 19 on page 34. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until both <sup>t</sup>RAS and <sup>t</sup>RP has been met. Note that part of the row precharge time is hidden during the access of the last data elements.

**Figure 12: READ Command**

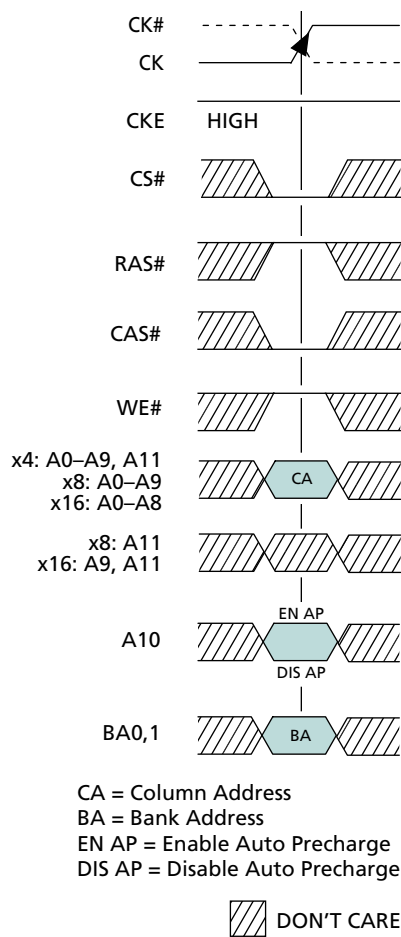
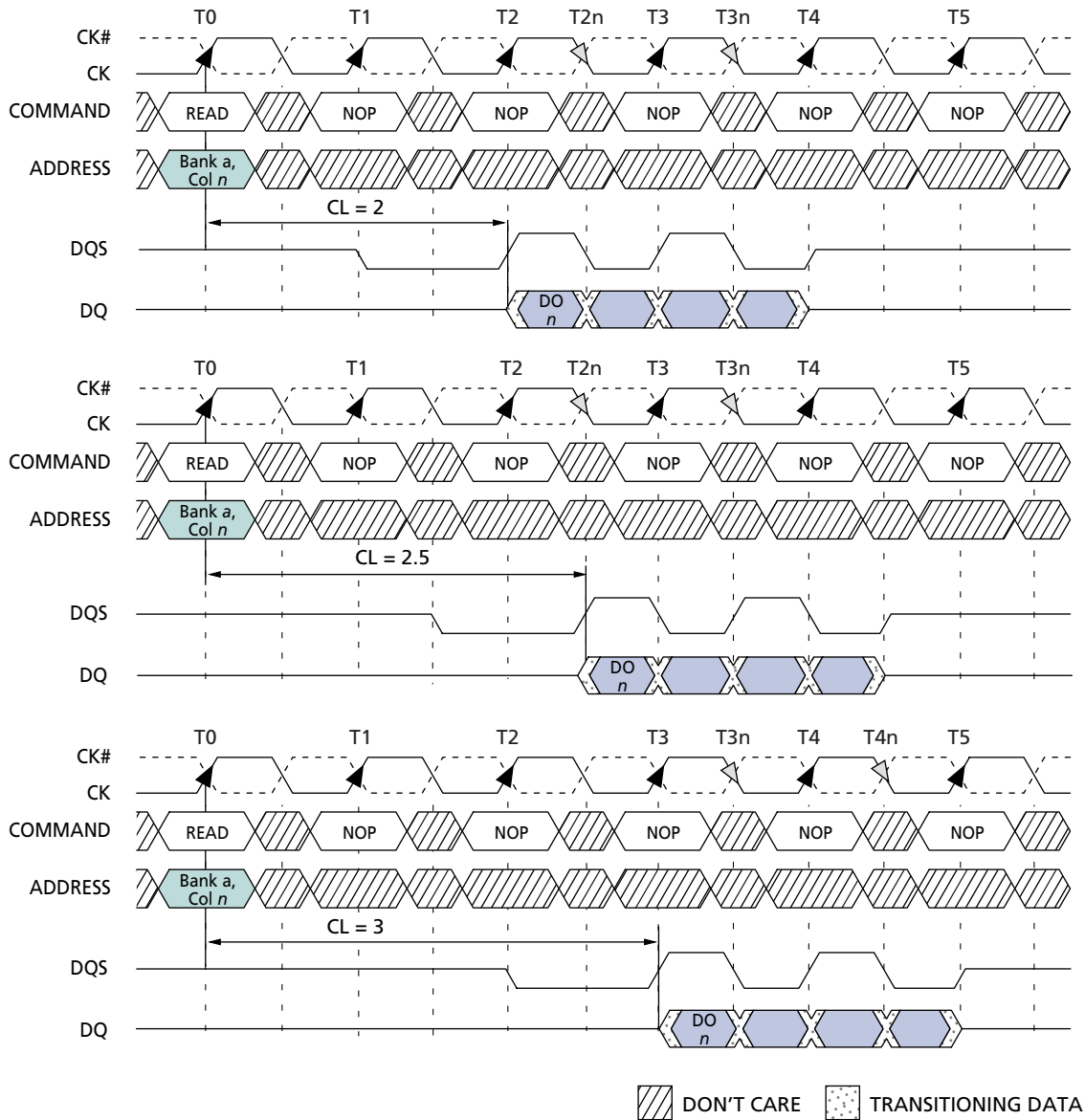
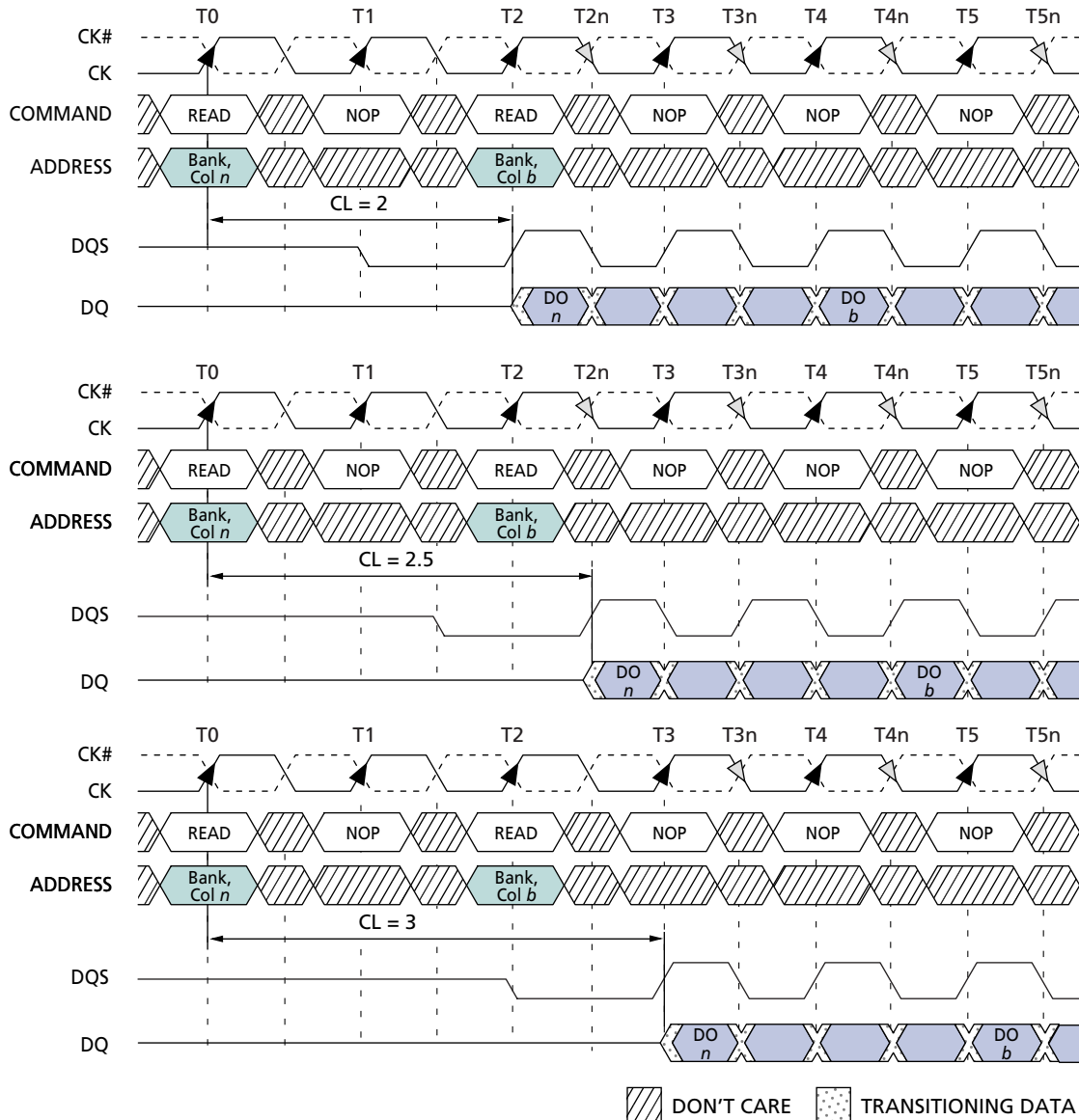


Figure 13: READ Burst

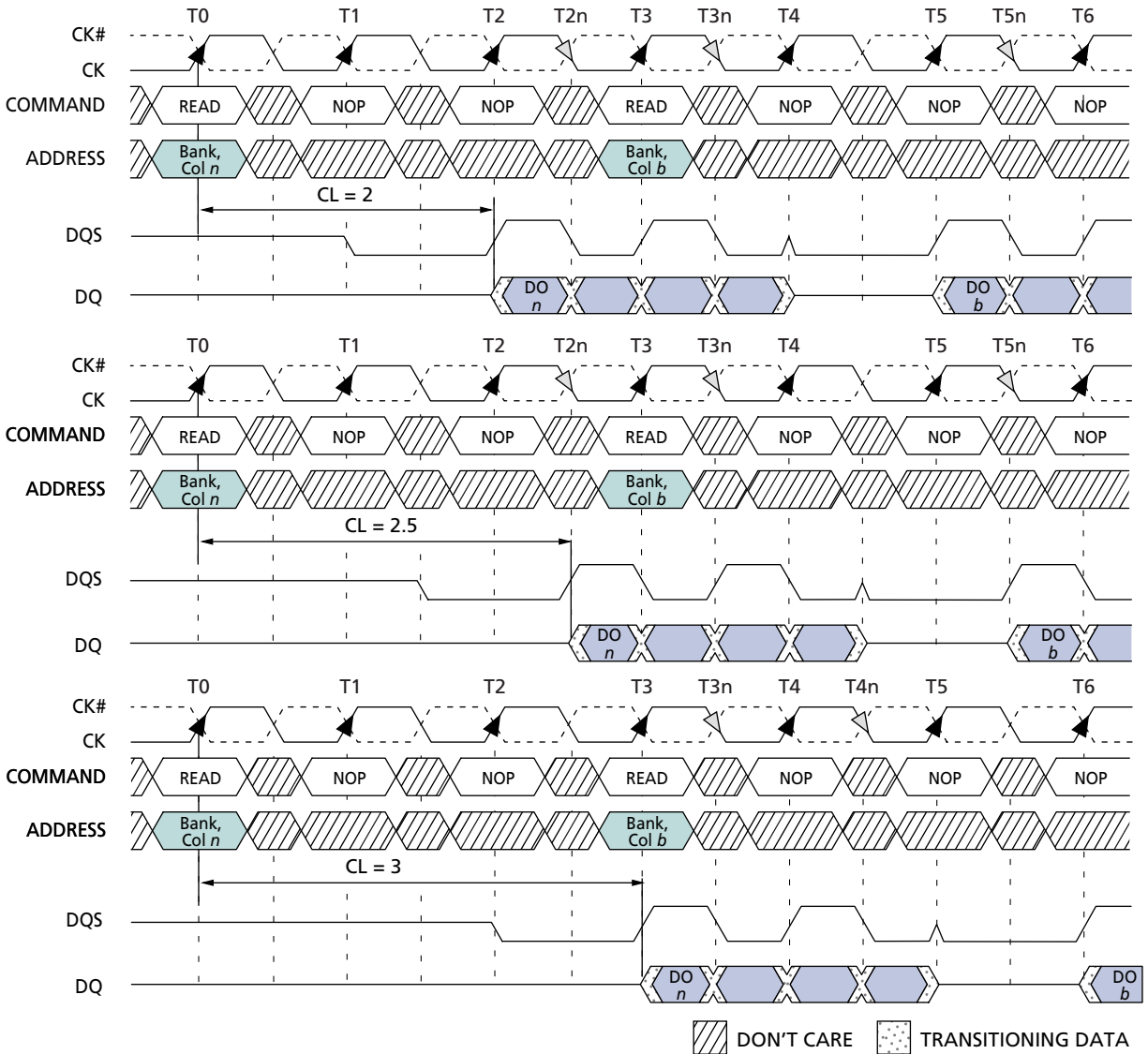


- Notes:
1. DO<sub>n</sub> = data-out from column *n*.
  2. Burst length = 4.
  3. Three subsequent elements of data-out appear in the programmed order following DO<sub>n</sub>.
  4. Shown with nominal <sup>t</sup>AC, <sup>t</sup>DQSK, and <sup>t</sup>DQSQ.

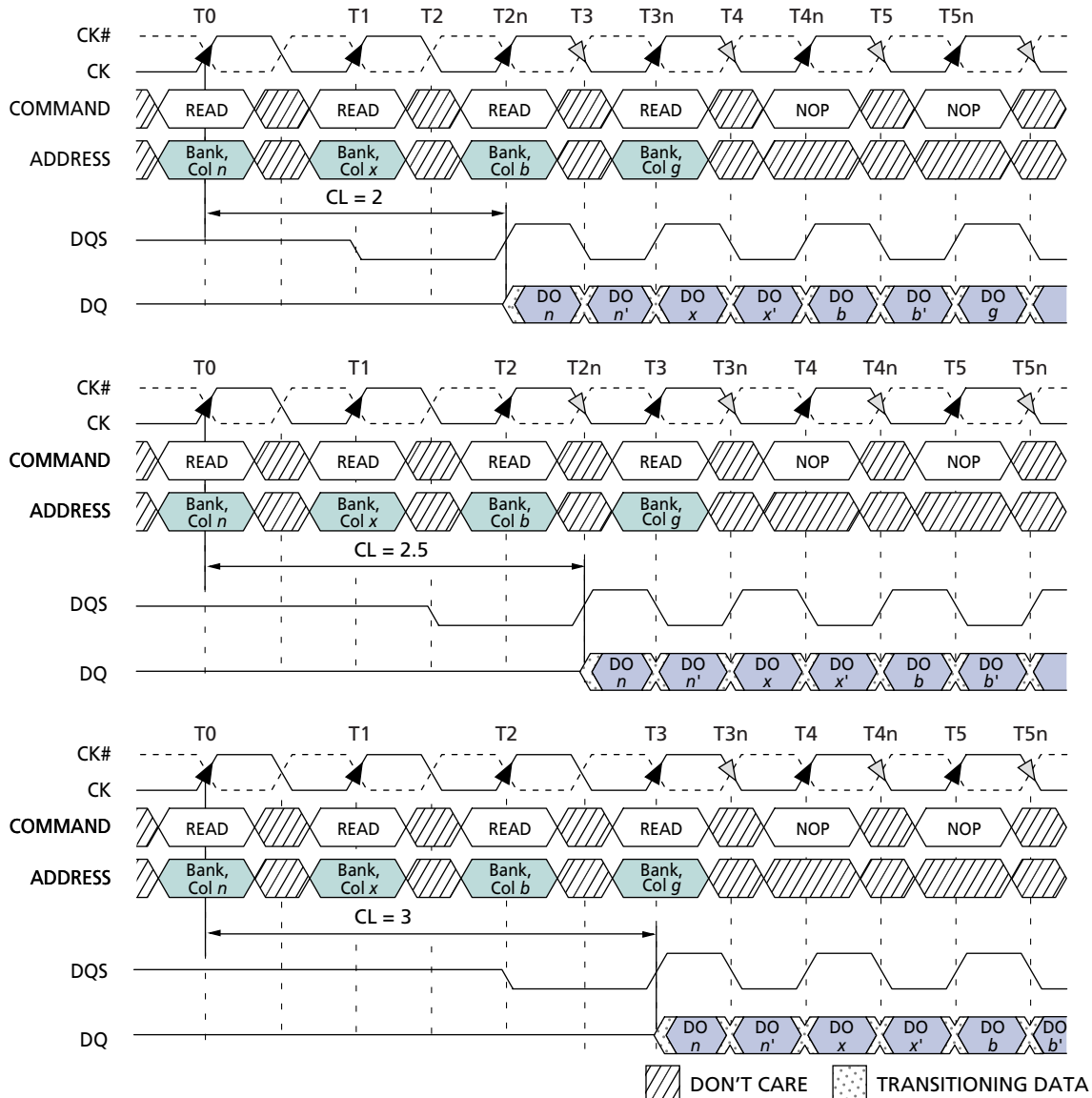
**Figure 14: Consecutive READ Bursts**


- Notes:
1. DO *n* (or *b*) = data-out from column *n* (or column *b*).
  2. Burst length = 4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first).
  3. Three subsequent elements of data-out appear in the programmed order following DO *n*.
  4. Three (or seven) subsequent elements of data-out appear in the programmed order following DO *b*.
  5. Shown with nominal <sup>t</sup>AC, <sup>t</sup>DQSCK, and <sup>t</sup>DQSQ.
  6. Example applies only when READ commands are issued to same device.

Figure 15: Nonconsecutive READ Bursts

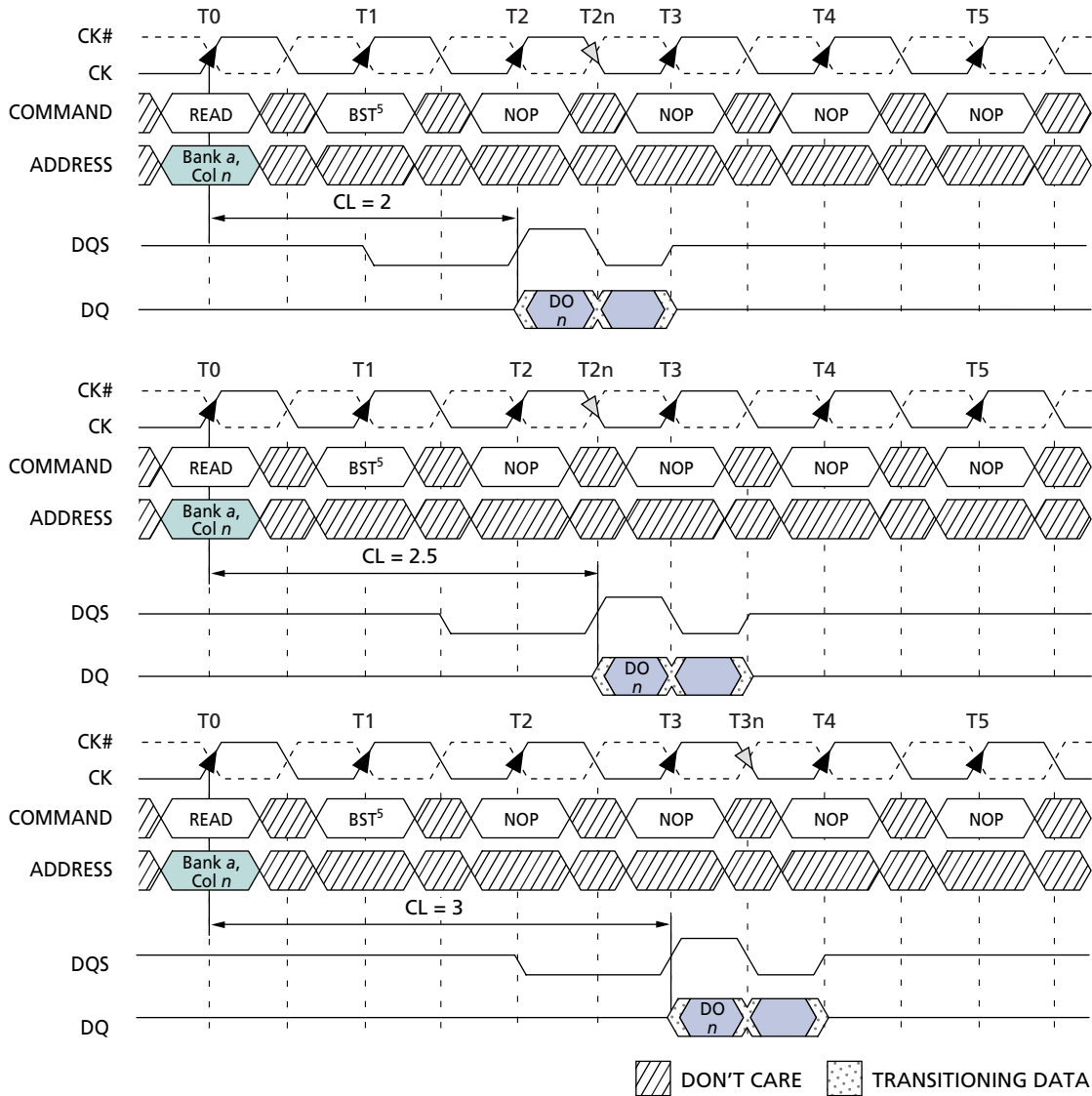


- Notes:
1. DO n (or b) = data-out from column n (or column b).
  2. Burst length = 4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first).
  3. Three subsequent elements of data-out appear in the programmed order following DO n.
  4. Three (or seven) subsequent elements of data-out appear in the programmed order following DO b.
  5. Shown with nominal  $t_{AC}$ ,  $t_{DQSK}$ , and  $t_{DQSQ}$ .

**Figure 16: Random READ Accesses**


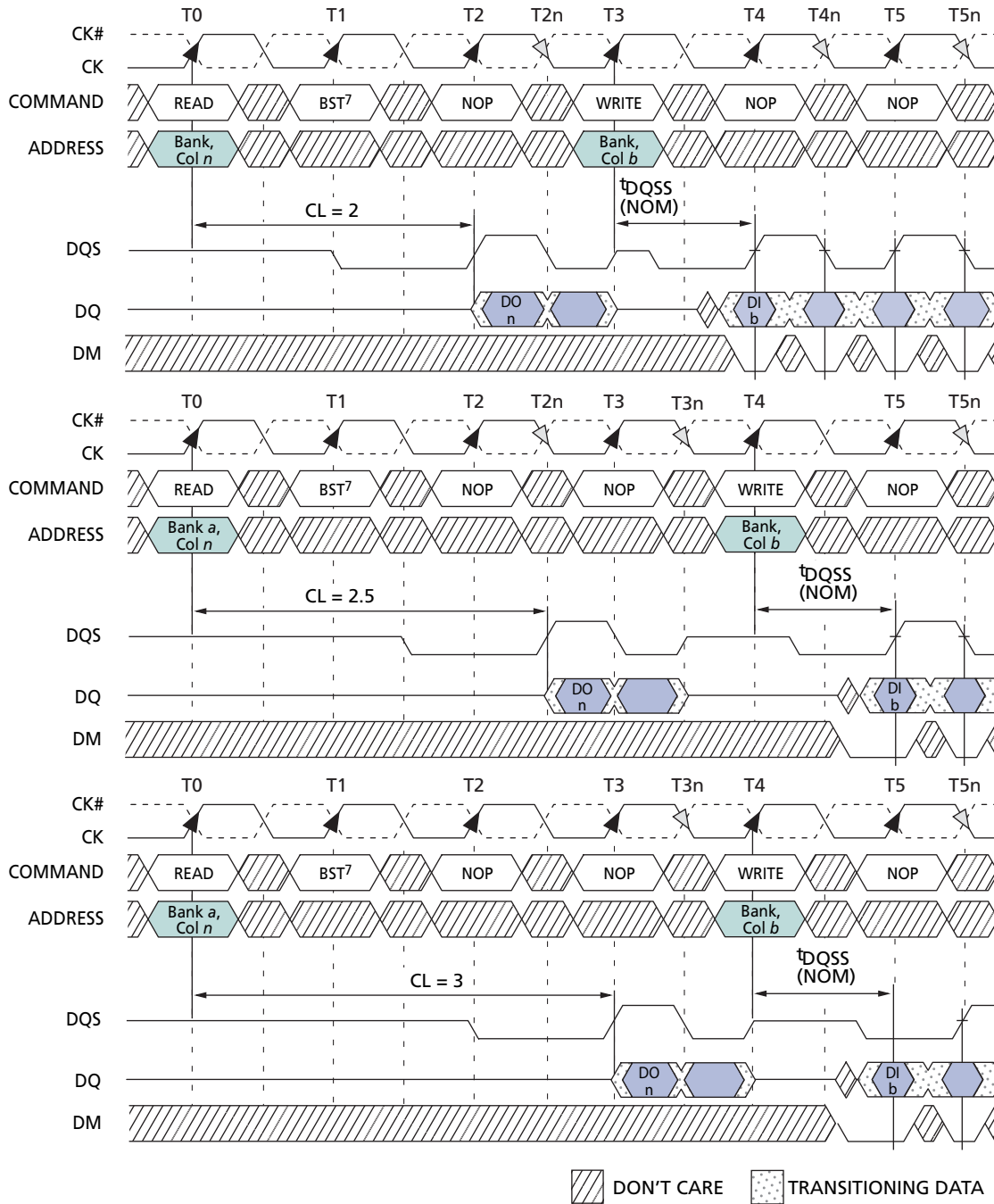
- Notes:
1. DO *n* (or *x* or *b* or *g*) = data-out from column *n* (or column *x* or column *b* or column *g*).
  2. Burst length = 2, 4 or 8 (if 4 or 8, the following burst interrupts the previous).
  3. *n'* or *x'* or *b'* or *g'* indicates the next data-out following DO *n* or DO *x* or DO *b* or DO *g*, respectively.
  4. READs are to an active row in any bank.
  5. Shown with nominal  $t_{AC}$ ,  $t_{DQSK}$ , and  $t_{DQSQ}$ .

Figure 17: Terminating a READ Burst

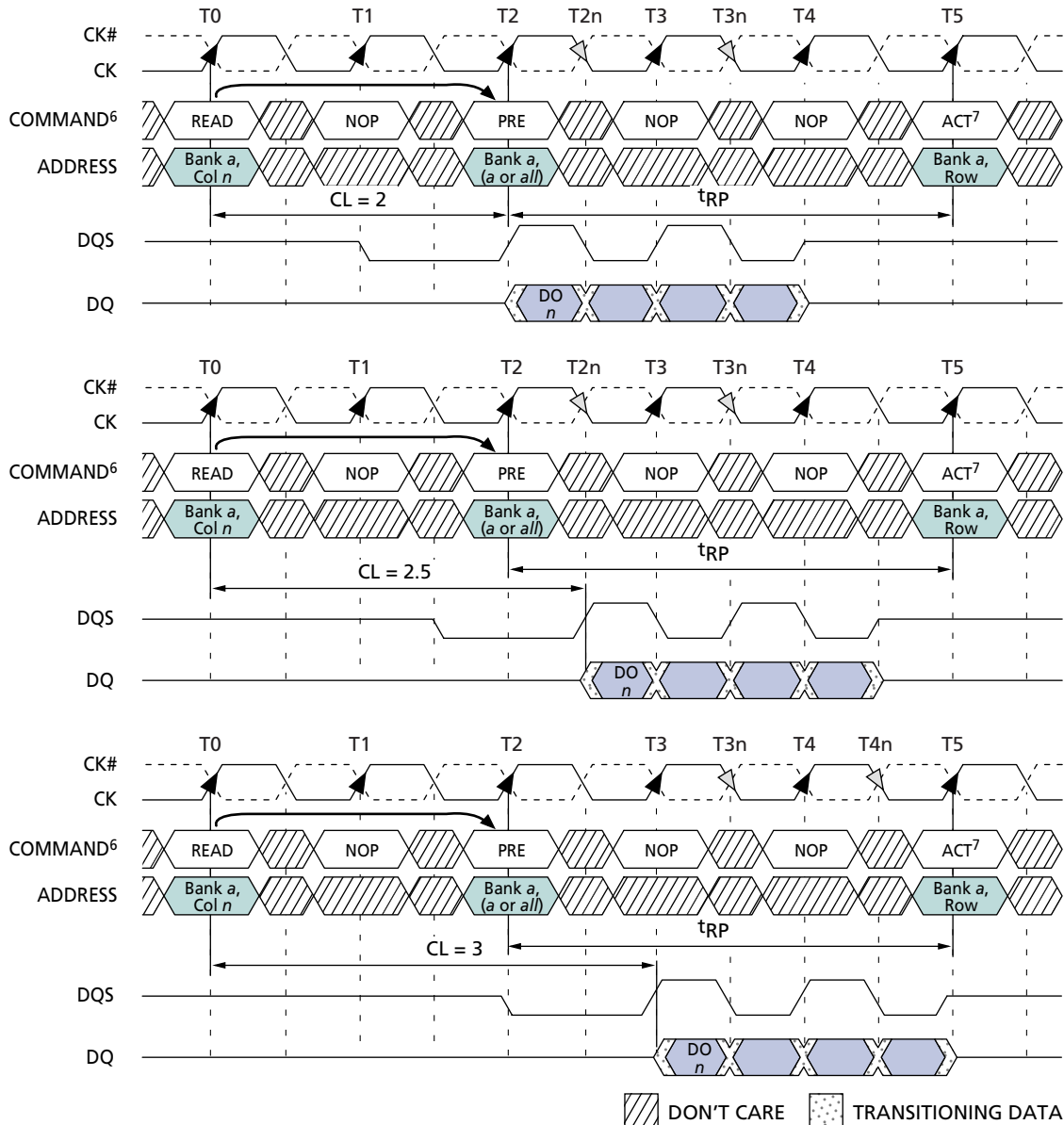


- Notes:
1.  $DO_n$  = data-out from column  $n$ .
  2. Burst length = 4 or 8.
  3. Subsequent element of data-out appears in the programmed order following  $DO_n$ .
  4. Shown with nominal  $t_{AC}$ ,  $t_{DQSK}$ , and  $t_{DQSQ}$ .
  5. BST = BURST TERMINATE command, page remains open.



**Figure 18: READ to WRITE**


- Notes:
1.  $DO_n$  = data-out from column  $n$ .
  2.  $DI_b$  = data-in from column  $b$ .
  3. Burst length = 4 in the cases shown (applies for bursts of 8 as well; if the burst length is 2, the BST command shown can be NOP).
  4. One subsequent element of data-out appears in the programmed order following  $DO_n$ .
  5. Data-in elements are applied following  $DI_b$  in the programmed order.
  6. Shown with nominal  $t_{AC}$ ,  $t_{DQSK}$ , and  $t_{DQSQ}$ .
  7. BST = BURST TERMINATE command, page remains open.

**Figure 19: READ to PRECHARGE**


- Notes:
1.  $DO_n$  = data-out from column  $n$ .
  2. Burst length = 4, or an interrupted burst of 8.
  3. Three subsequent elements of data-out appear in the programmed order following  $DO_n$ .
  4. Shown with nominal  $t_{AC}$ ,  $t_{DQSCK}$ , and  $t_{DQSQ}$ .
  5. READ to PRECHARGE equals two clocks, which allows two data pairs of data-out; it is also assumed that  $t_{RAS}$  (MIN) is met.
  6. A READ command with AUTO-PRECHARGE enabled, provided  $t_{RAS}$ (MIN) is met, would cause a precharge to be performed at  $x$  number of clock cycles after the READ command, where  $x = BL / 2$ .
  7. An active command to the same bank is only allowed if  $t_{RC}$  (MIN) has been satisfied.
  8. PRE = PRECHARGE command; ACT = ACTIVE command.

## WRITEs

WRITE bursts are initiated with a WRITE command, as shown in Figure 20.

The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst and after the  $t_{WR}$  time.

**Note:** For the WRITE commands used in the following illustrations, auto precharge is disabled.

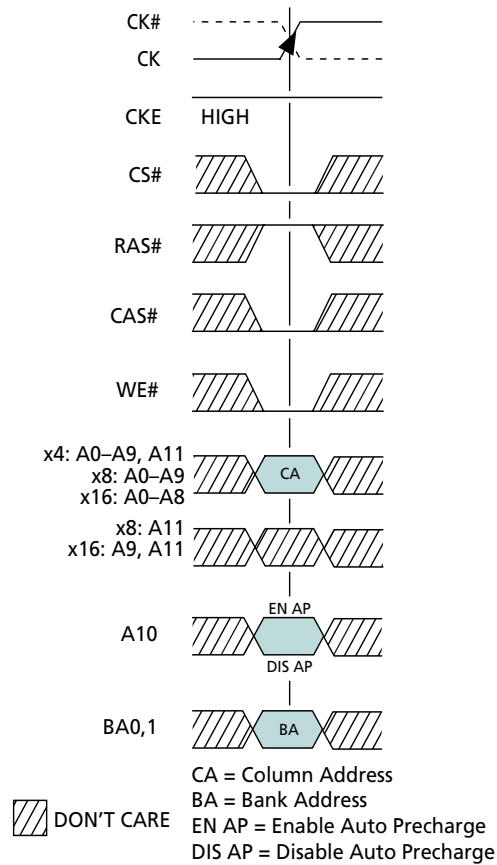
During WRITE bursts, the first valid data-in element will be registered on the first rising edge of DQS following the WRITE command, and subsequent data elements will be registered on successive edges of DQS. The LOW state on DQS between the WRITE command and the first rising edge is known as the write preamble; the LOW state on DQS following the last data-in element is known as the write postamble.

The time between the WRITE command and the first corresponding rising edge of DQS ( $t_{DQSS}$ ) is specified with a relatively wide range (from 75 percent to 125 percent of one clock cycle and 72

percent to 128 percent of one clock cycle for DDR400). All of the WRITE diagrams show the nominal case, and where the two extreme cases (i.e.,  $t_{DQSS}$  [MIN] and  $t_{DQSS}$  [MAX]) might not be intuitive, they have also been included. Figure 21 on page 37 shows the nominal case and the extremes of  $t_{DQSS}$  for a burst of 4. Upon completion of a burst, assuming no other commands have been initiated, the DQ will remain High-Z and any additional input data will be ignored.

Data for any WRITE burst may be concatenated with or truncated with a subsequent WRITE command. In either case, a continuous flow of input data can be maintained. The new WRITE command can be issued on any positive edge of clock following the previous WRITE command. The first data element from the new burst is applied after either the last element of a completed burst or the last desired data element of a longer burst which is being truncated. The new WRITE command should be issued  $x$  cycles after the first WRITE command, where  $x$  equals the number of desired data element pairs (pairs are required by the  $2n$ -prefetch architecture).

Figure 22 on page 38 shows concatenated bursts of 4. An example of nonconsecutive WRITEs is shown in Figure 23 on page 39. Full-speed random write accesses within a page or pages can be performed as shown in Figure 24 on page 40.

**Figure 20: WRITE Command**


Data for any WRITE burst may be followed by a subsequent READ command. To follow a WRITE without truncating the WRITE burst,  $t_{WTR}$  should be met as shown in Figure 25 on page 41.

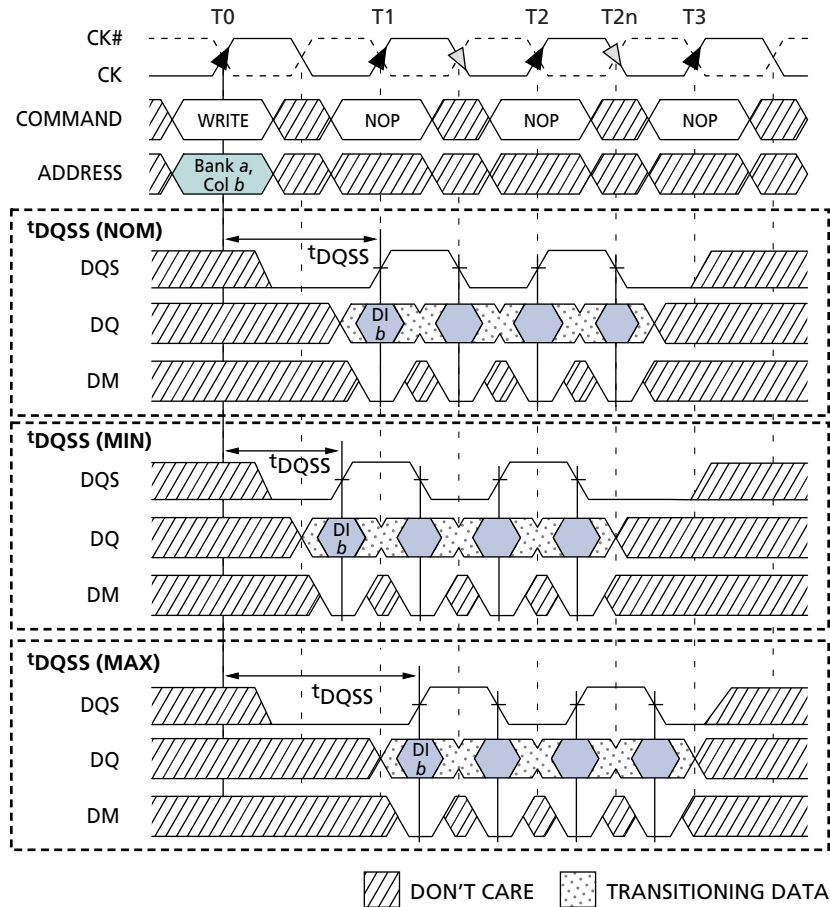
Data for any WRITE burst may be truncated by a subsequent READ command, as shown in Figure 26 on page 42.

Note that only the data-in pairs that are registered prior to the  $t_{WTR}$  period are written to the internal array, and any subsequent data-in should be masked with DM as shown in Figure 27 on page 43.

Data for any WRITE burst may be followed by a subsequent PRECHARGE command. To follow a WRITE without truncating the WRITE burst,  $t_{WR}$  should be met as shown in Figure 28 on page 44.

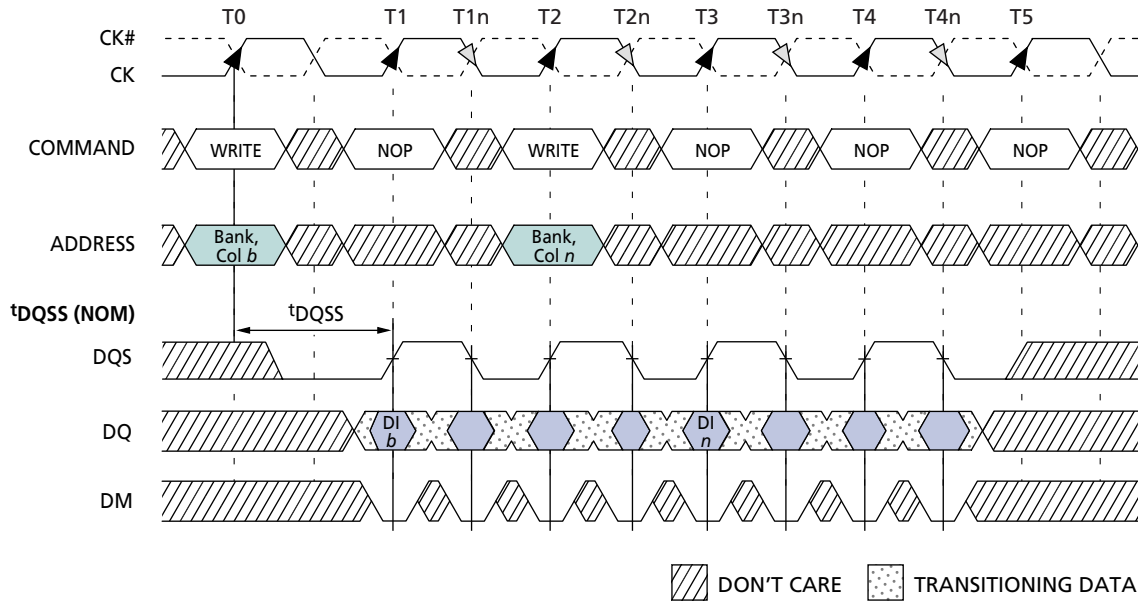
Data for any WRITE burst may be truncated by a subsequent PRECHARGE command, as shown in Figure 29 on page 45 and Figure 30 on page 46. Note that only the data-in pairs that are registered prior to the  $t_{WR}$  period are written to the internal array, and any subsequent data-in should be masked with DM as shown in Figures 29 and 30. After the PRECHARGE command, a subsequent command to the same bank cannot be issued until  $t_{RP}$  is met.

Figure 21: WRITE Burst



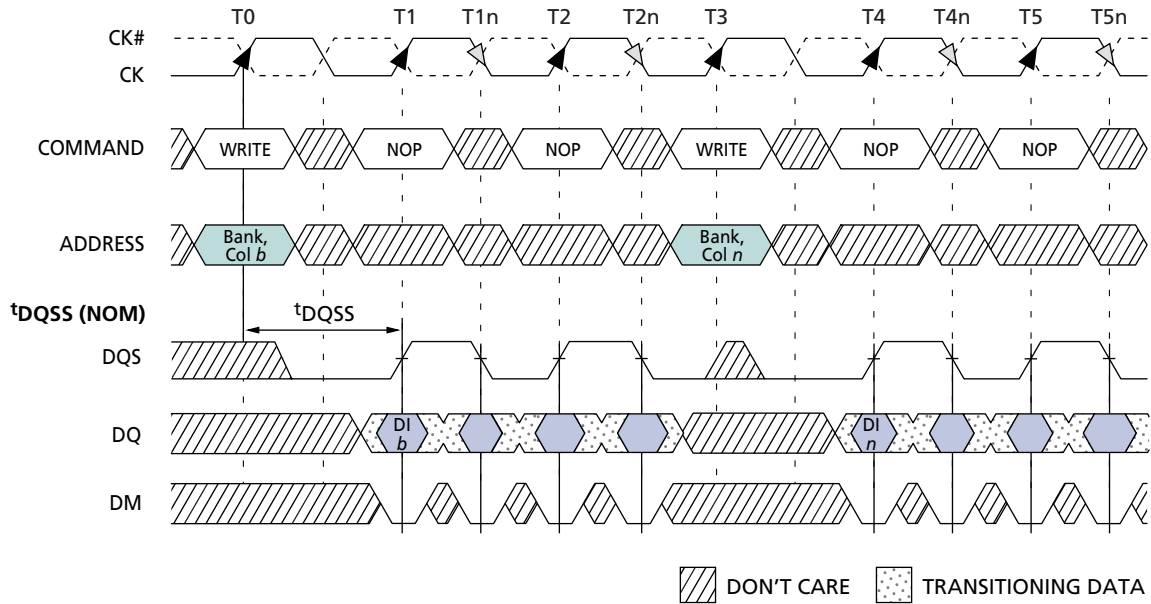
- Notes:
1. DI *b* = data-in for column *b*.
  2. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
  3. An uninterrupted burst of 4 is shown.
  4. A10 is LOW with the WRITE command (auto precharge is disabled).

**Figure 22: Consecutive WRITE to WRITE**



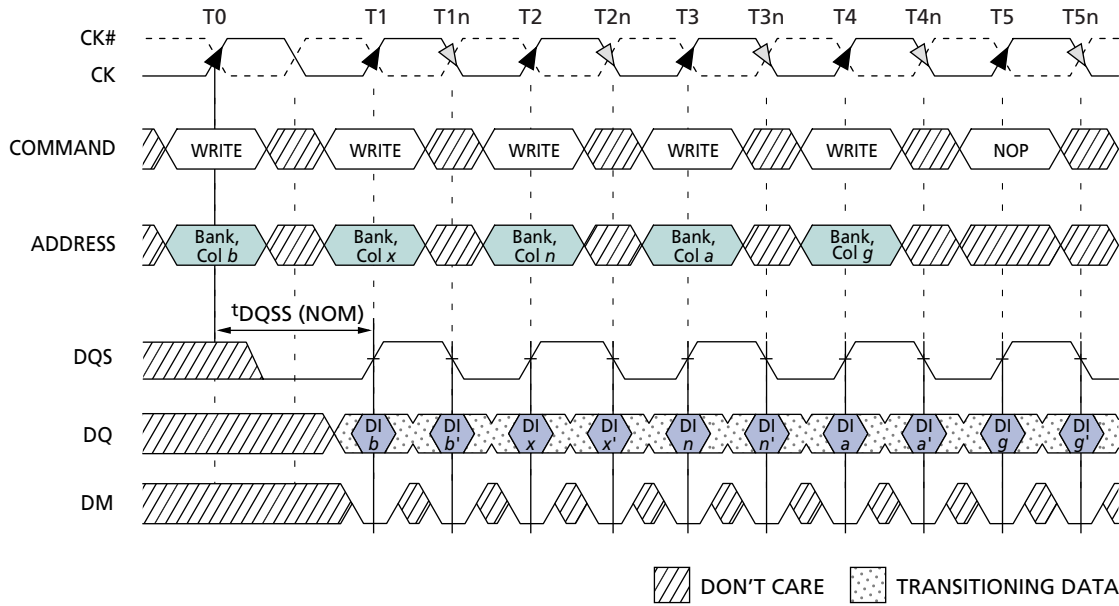
- Notes:
1. DI *b*, etc. = data-in for column *b*, etc.
  2. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
  3. Three subsequent elements of data-in are applied in the programmed order following DI *n*.
  4. An uninterrupted burst of 4 is shown.
  5. Each WRITE command may be to any bank.

**Figure 23: Nonconsecutive WRITE to WRITE**



- Notes:
1. DI *b*, etc. = data-in for column *b*, etc.
  2. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
  3. Three subsequent elements of data-in are applied in the programmed order following DI *n*.
  4. An uninterrupted burst of 4 is shown.
  5. Each WRITE command may be to any bank.

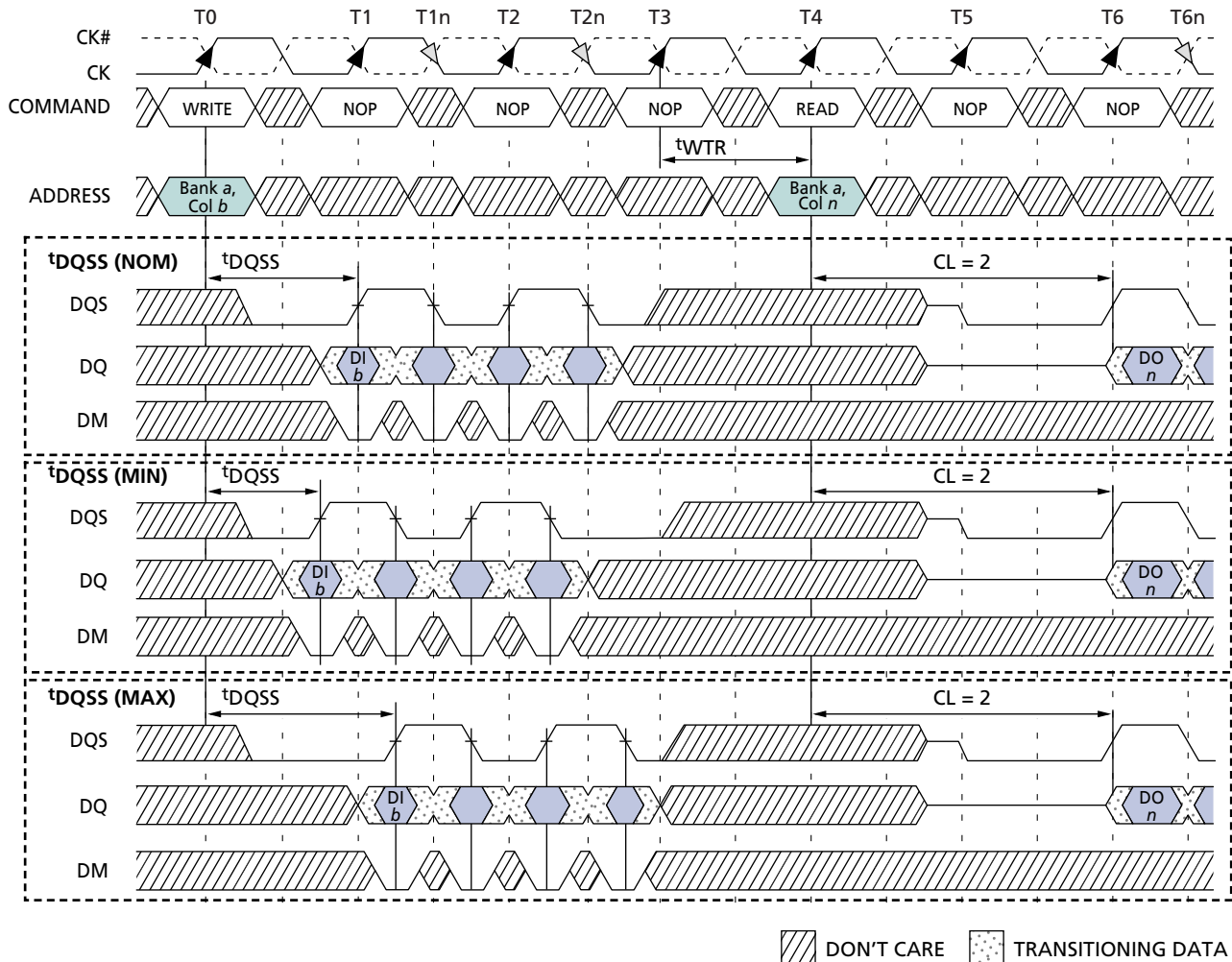
**Figure 24: Random WRITE Cycles**



- Notes:
1. DI *b*, etc. = data-in for column *b*, etc.
  2. *b'*, etc. = the next data-in following DI *b*, etc., according to the programmed burst order.
  3. Programmed burst length = 2, 4, or 8 in cases shown.
  4. Each WRITE command may be to any bank.

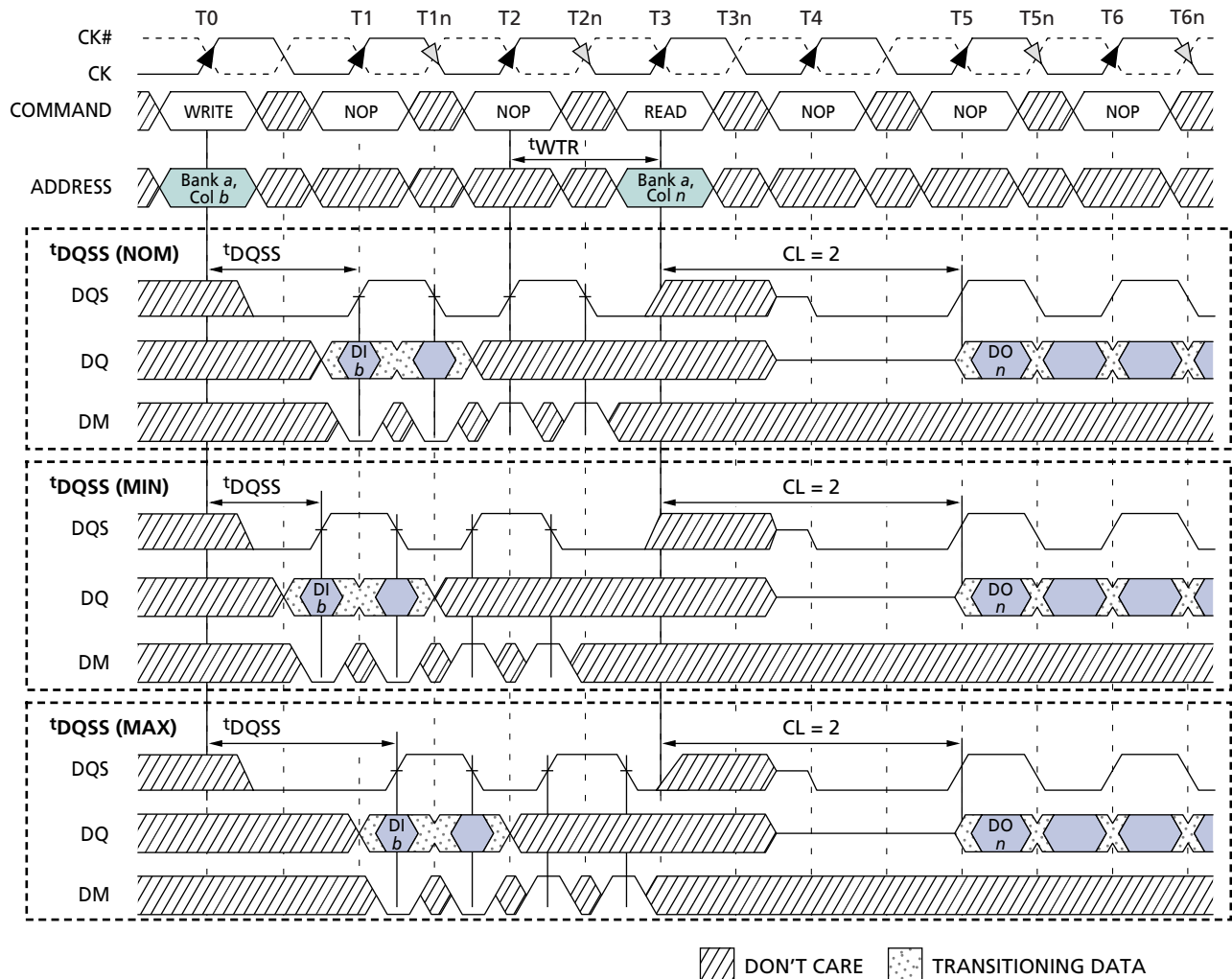


Figure 25: WRITE to READ - Uninterrupting



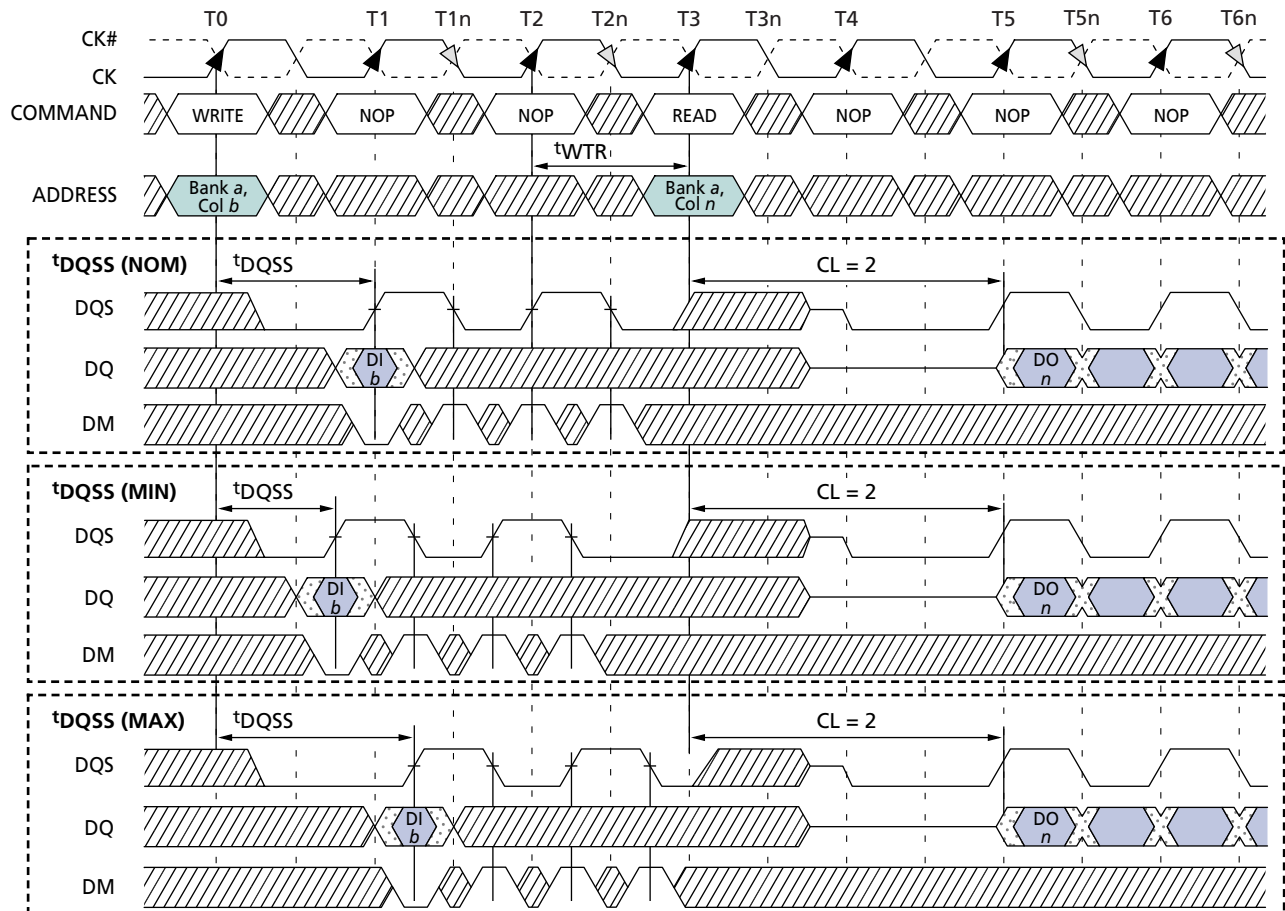
- Notes:
1.  $DI\ b$  = data-in for column  $b$ ,  $DO\ n$  = data-out for column  $n$ .
  2. Three subsequent elements of data-in are applied in the programmed order following  $DI\ b$ .
  3. An uninterrupted burst of 4 is shown.
  4.  $t_{WTR}$  is referenced from the first positive CK edge after the last data-in pair.
  5. The READ and WRITE commands are to same device. However, the READ and WRITE commands may be to different devices, in which case  $t_{WTR}$  is not required and the READ command could be applied earlier.
  6. A10 is LOW with the WRITE command (auto precharge is disabled).

Figure 26: WRITE to READ - Interrupting



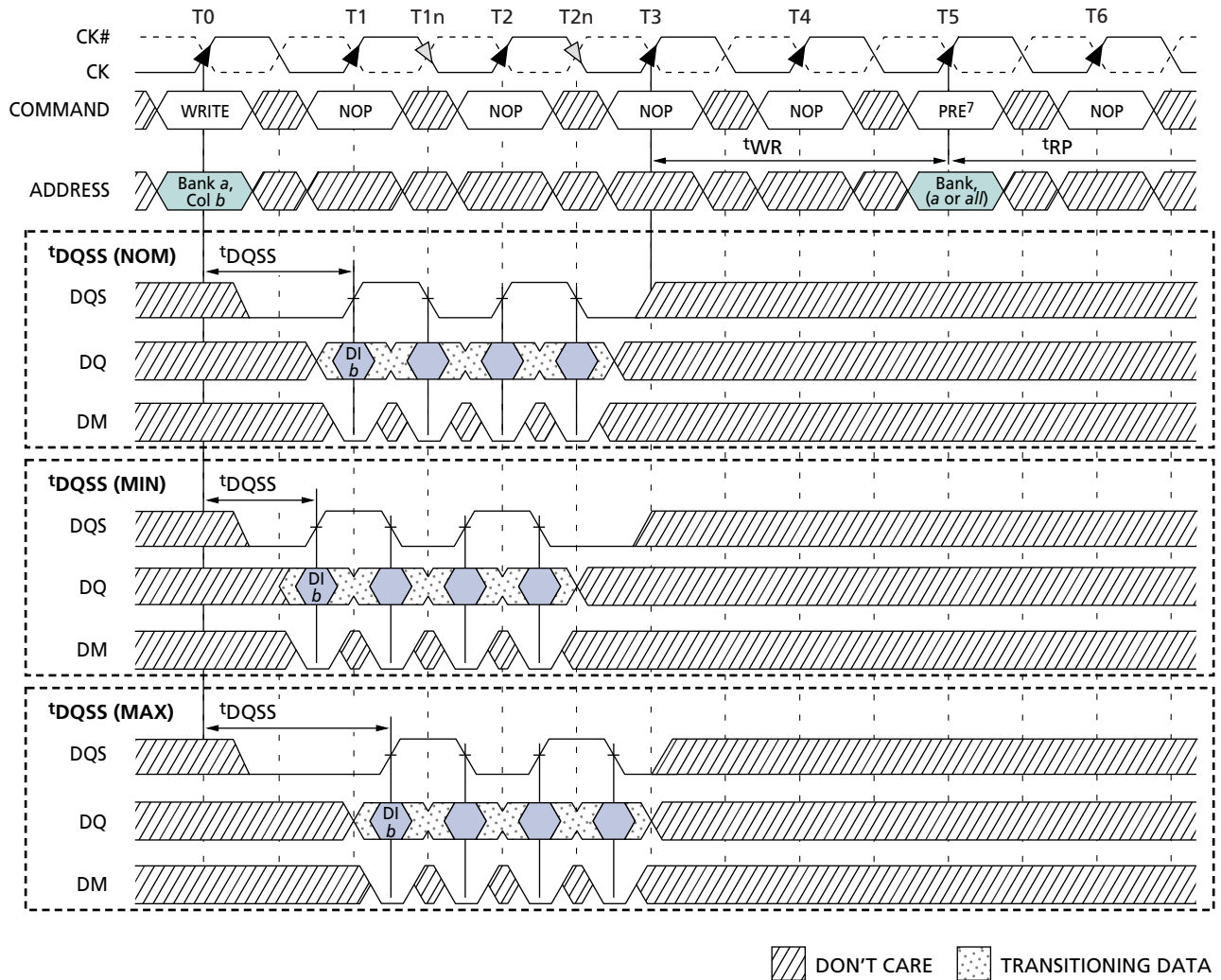
- Notes:
1. DI  $b$  = data-in for column  $b$ , DO  $n$  = data-out for column  $n$ .
  2. An interrupted burst of 4 is shown; two data elements are written.
  3. One subsequent element of data-in is applied in the programmed order following DI  $b$ .
  4.  $t_{WTR}$  is referenced from the first positive CK edge after the last data-in pair.
  5. A10 is LOW with the WRITE command (auto precharge is disabled).
  6. DQS is required at T2 and T2n (nominal case) to register DM.
  7. If the burst of 8 was used, DM and DQS would be required at T3 and T3n because the READ command would not mask these two data elements.

Figure 27: WRITE to READ - Odd Number of Data, Interrupting



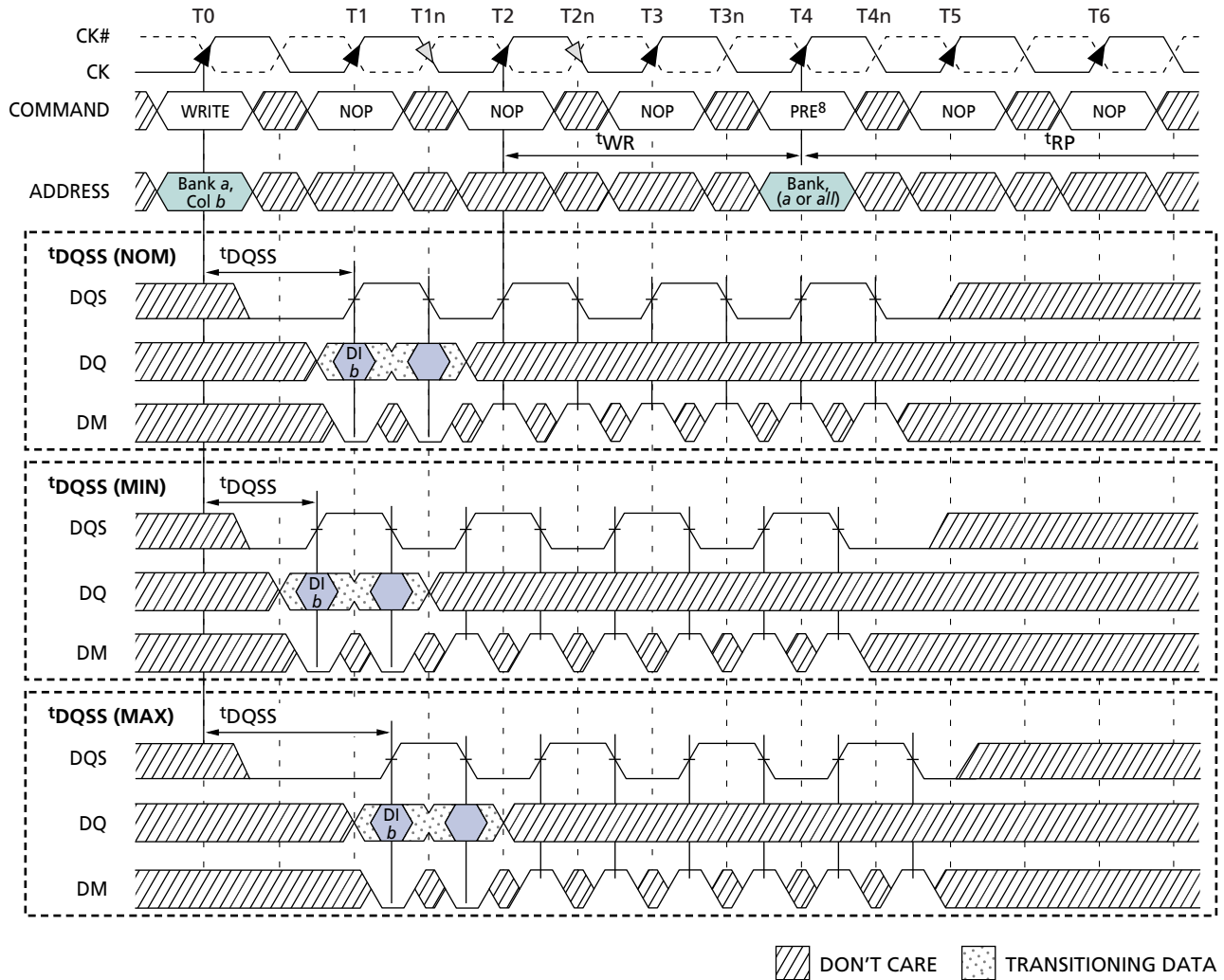
- Notes:
1.  $DI\ b$  = data-in for column  $b$ ,  $DO\ n$  = data-out for column  $n$ .
  2. An interrupted burst of 4 is shown; one data element is written.
  3.  $t_{WTR}$  is referenced from the first positive CK edge after the last desired data-in pair (not the last two data elements).
  4. A10 is LOW with the WRITE command (auto precharge is disabled).
  5. DQS is required at T1n, T2, and T2n (nominal case) to register DM.
  6. If the burst of 8 was used, DM and DQS would be required at T3 - T3n because the READ command would not mask these data elements.

Figure 28: WRITE to PRECHARGE - Uninterrupting



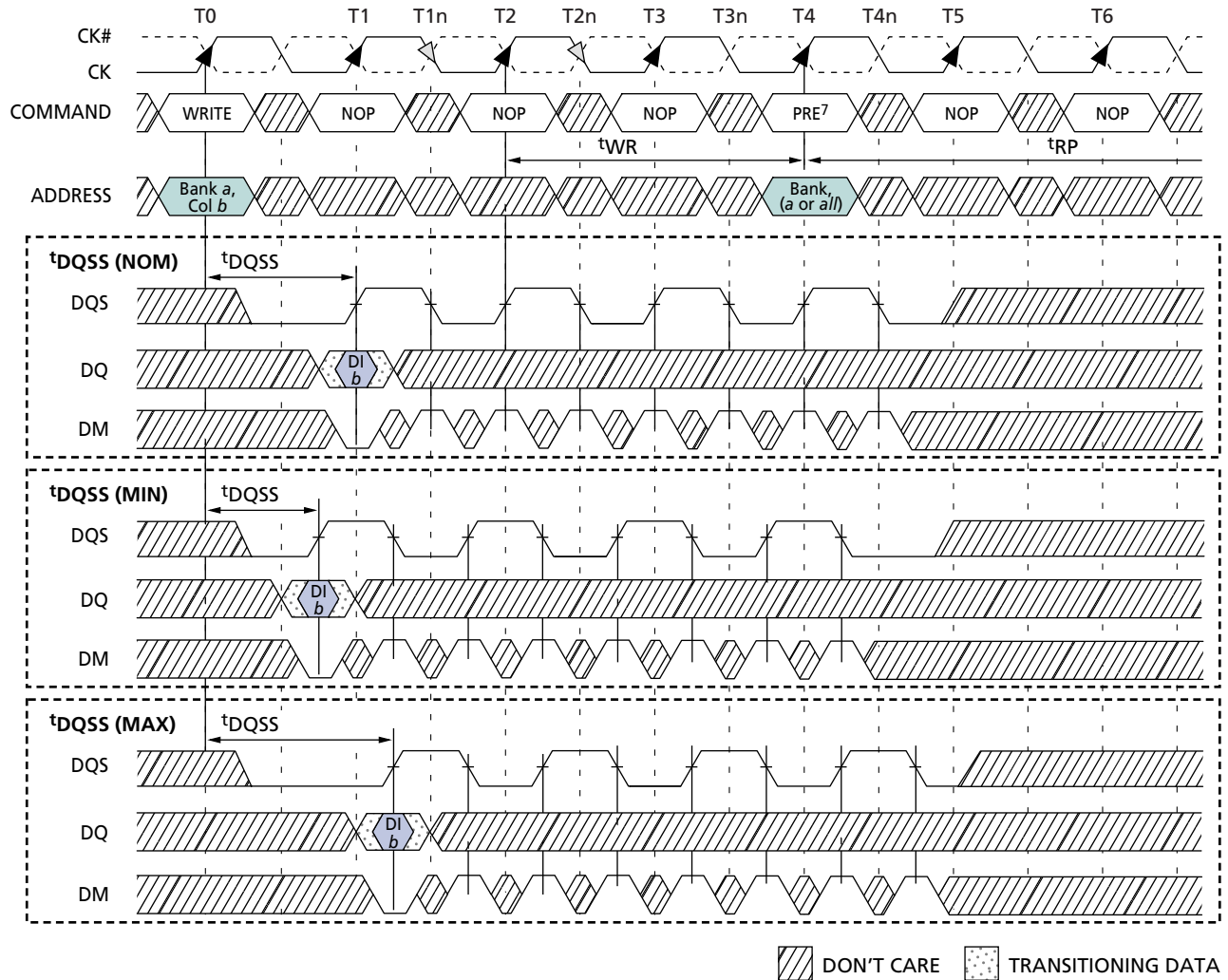
- Notes:
1. DI b = data-in for column b.
  2. Three subsequent elements of data-in are applied in the programmed order following DI b.
  3. An uninterrupted burst of 4 is shown.
  4.  $t_{WR}$  is referenced from the first positive CK edge after the last data-in pair.
  5. The PRECHARGE and WRITE commands are to the same device. However, the PRECHARGE and WRITE commands may be to different devices, in which case  $t_{WR}$  is not required and the PRECHARGE command could be applied earlier.
  6. A10 is LOW with the WRITE command (auto precharge is disabled).
  7. PRE = PRECHARGE command.

Figure 29: WRITE to Precharge – Interrupting



- Notes:
1. DI *b* = data-in for column *b*.
  2. Subsequent element of data-in is applied in the programmed order following DI *b*.
  3. An interrupted burst of 8 is shown; two data elements are written.
  4.  $t_{WR}$  is referenced from the first positive CK edge after the last data-in pair.
  5. A10 is LOW with the WRITE command (auto precharge is disabled).
  6. DQS is required at T4 and T4n (nominal case) to register DM.
  7. If the burst of 4 was used, DQS and DM would not be required at T3, T3n, T4 and T4n.
  8. PRE = PRECHARGE command.

Figure 30: WRITE to PRECHARGE Odd Number of Data, Interrupting

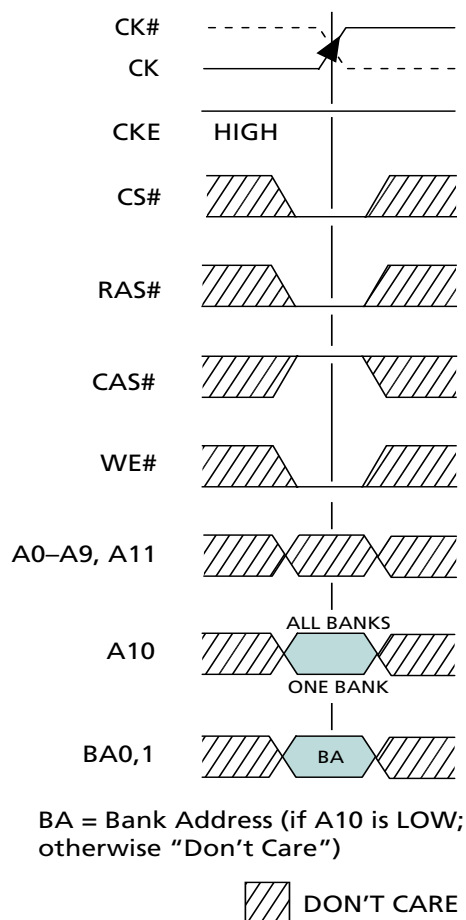


- Notes:
1. DI *b* = data-in for column *b*.
  2. An interrupted burst of 8 is shown; one data element is written.
  3.  $t_{WR}$  is referenced from the first positive CK edge after the last data-in pair.
  4. A10 is LOW with the WRITE command (auto precharge is disabled).
  5. DQS is required at T4 and T4n (nominal case) to register DM.
  6. If the burst of 4 was used, DQS and DM would not be required at T3, T3n, T4 and T4n.
  7. PRE = PRECHARGE command.

## PRECHARGE

The PRECHARGE command, as shown in Figure 31, is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time ( $t^1RP$ ) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

**Figure 31: PRECHARGE Command**



## Power-Down (CKE Not Active)

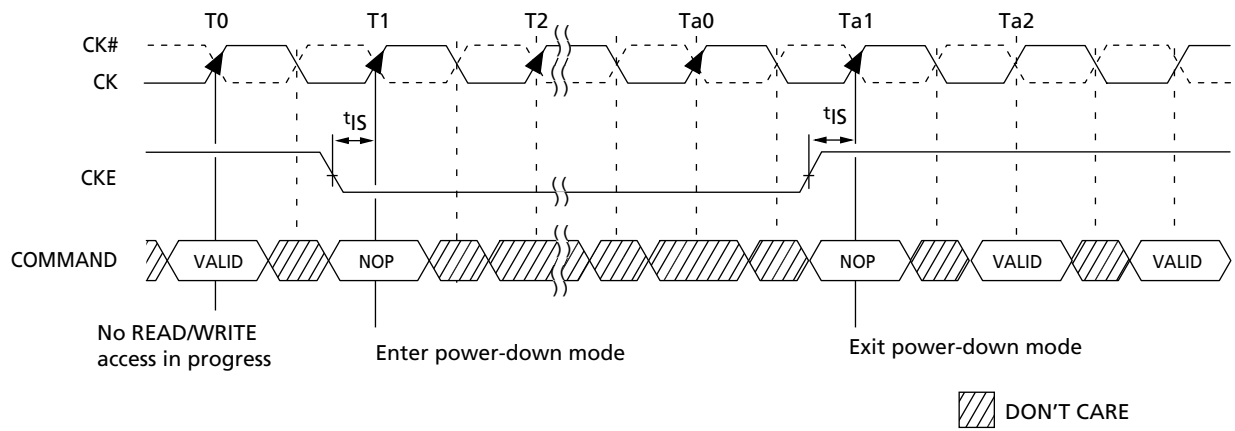
Unlike SDR SDRAMs, DDR SDRAMs require CKE to be active at all times an access is in progress, from the issuing of a READ or WRITE command until completion of the access. Thus a clock suspend is not supported. For READs, an access completion is defined when the Read Postamble is satisfied; for WRITEs, an access completion is defined when the Write Recovery time ( $t^1WR$ ) is satisfied.

Power-down as shown in Figure 32 on page 48, is entered when CKE is registered LOW and all Table 10 (page 49) criteria are met. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-

down deactivates the input and output buffers, excluding CK, CK#, and CKE. For maximum power savings, the DLL is frozen during precharge power-down mode. Exiting power-down requires the device to be at the same voltage and frequency as when it entered power-down. However, power-down duration is limited by the refresh requirements of the device ( $t^{REFC}$ ).

While in power-down, CKE LOW and a stable clock signal must be maintained at the inputs of the DDR SDRAM, while all other input signals are “Don’t Care.” The power-down state is synchronously exited when CKE is registered HIGH (in conjunction with a NOP or DESELECT command). A valid executable command may be applied one clock cycle later.

**Figure 32: Power-Down**





**Table 10: Truth Table – CKE**

Notes: 1-6

CKE <sub>n-1</sub>	CKE <sub>n</sub>	Current State	Command <sub>n</sub>	Action <sub>n</sub>	Notes
L	L	Power-Down	X	Maintain Power-Down	
		Self Refresh	X	Maintain Self Refresh	
L	H	Power-Down	DESELECT or NOP	Exit Power-Down	
		Self Refresh	DESELECT or NOP	Exit Self Refresh	7
H	L	All Banks Idle	DESELECT or NOP	Precharge Power-Down Entry	
		Bank(s) Active	DESELECT or NOP	Active Power-Down Entry	
		All Banks Idle	AUTO REFRESH	Self Refresh Entry	
H	H		See Table 11 on page 50		

- Notes:
1. CKE<sub>n</sub> is the logic state of CKE at clock edge n; CKE<sub>n-1</sub> was the state of CKE at the previous clock edge.
  2. Current state is the state of the DDR SDRAM immediately prior to clock edge n.
  3. COMMAND<sub>n</sub> is the command registered at clock edge n, and ACTION<sub>n</sub> is a result of COMMAND<sub>n</sub>.
  4. All states and sequences not shown are illegal or reserved.
  5. CKE must not drop low during a column access. For a READ, this means CKE must stay high until after the Read Postamble time; for a WRITE, CKE must stay high until the WRITE Recovery Time (<sup>t</sup>WR) has been met.
  6. Once initialized, including during self refresh mode, VREF must be powered with in the specified range.
  7. Upon exit of the Self Refresh mode the DLL is automatically enabled. A minimum of 200 clock cycles with CKE HIGH is needed before applying a READ command for the DLL to lock. DESELECT or NOP commands should be issued on any clock edges occurring during the <sup>t</sup>XSNR period.

**Table 11: Truth Table – Current State Bank  $n$  - Command to Bank  $n$** 

(Notes: 1-6; notes appear below and on next page)

Current State	CS#	RAS#	CAS#	WE#	Command/Action	Notes
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	L	L	H	H	ACTIVE (select and activate row)	
	L	L	L	H	AUTO REFRESH	7
	L	L	L	L	LOAD MODE REGISTER	7
Row Active	L	H	L	H	READ (select column and start READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (deactivate row in bank or banks)	8
Read (Auto-Precharge Disabled)	L	H	L	H	READ (select column and start new READ burst)	10
	L	H	L	L	WRITE (select column and start WRITE burst)	10, 12
	L	L	H	L	PRECHARGE (truncate READ burst, start PRECHARGE)	8
	L	H	H	L	BURST TERMINATE	9
Write (Auto-Precharge Disabled)	L	H	L	H	READ (select column and start READ burst)	10, 11
	L	H	L	L	WRITE (select column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (truncate WRITE burst, start PRECHARGE)	8, 11

Notes: 1. This table applies when  $CKE_{n-1}$  was HIGH and  $CKE_n$  is HIGH (see Table 10 on page 49) and after  $t_{XSNR}$  has been met (if the previous state was self refresh).

2. This table is bank-specific, except where noted (i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state). Exceptions are covered in the notes below.

3. Current state definitions:

- Idle: The bank has been precharged, and  $t_{RP}$  has been met.
- Row Active: A row in the bank has been activated, and  $t_{RCD}$  has been met. No data bursts/accesses and no register accesses are in progress.
- Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
- Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.

4. The following states must not be interrupted by a command issued to the same bank. DESELECT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Table 11, Truth Table – Current State Bank  $n$  - Command to Bank  $n$ , on page 50 and according to Table 12, Truth Table – Current State Bank  $n$  - Command to Bank  $m$ , on page 52.

- Precharging: Starts with registration of a PRECHARGE command and ends when  $t_{RP}$  is met. Once  $t_{RP}$  is met, the bank will be in the idle state.
- Row Activating: Starts with registration of an ACTIVE command and ends when  $t_{RCD}$  is met. Once  $t_{RCD}$  is met, the bank will be in the “row active” state.
- Read w/Auto-Precharge Enabled: Starts with registration of a READ command with auto precharge enabled and ends when  $t_{RP}$  has been met. Once  $t_{RP}$  is met, the bank will be in the idle state.
- Write w/Auto-Precharge Enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when  $t_{RP}$  has been met. Once  $t_{RP}$  is met, the bank will be in the idle state.

5. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.

- Refreshing: Starts with registration of an AUTO REFRESH command and ends when  $t_{RFC}$  is met. Once  $t_{RFC}$  is met, the DDR SDRAM will be in the all banks idle state.

- Accessing Mode Register: Starts with registration of a LOAD MODE REGISTER command and ends when  $t^{\text{MRD}}$  has been met. Once  $t^{\text{MRD}}$  is met, the DDR SDRAM will be in the all banks idle state.
- Precharging All: Starts with registration of a PRECHARGE ALL command and ends when  $t^{\text{RP}}$  is met. Once  $t^{\text{RP}}$  is met, all banks will be in the idle state.
  6. All states and sequences not shown are illegal or reserved.
  7. Not bank-specific; requires that all banks are idle, and bursts are not in progress.
  8. May or may not be bank-specific; if multiple banks are to be precharged, each must be in a valid state for precharging.
  9. Not bank-specific; BURST TERMINATE affects the most recent READ burst, regardless of bank.
  10. READs or WRITEs listed in the Command/Action column include Reads or Writes with auto precharge enabled and READs or WRITEs with auto precharge disabled.
  11. Requires appropriate DM masking.
  12. A WRITE command may be applied after the completion of the READ burst; otherwise, a BURST TERMINATE must be used to end the READ burst prior to asserting a WRITE command.

**Table 12: Truth Table – Current State Bank *n* - Command to Bank *m***

(Notes: 1-6; notes appear below and on next page)

Current State	CS#	RAS#	CAS#	WE#	Command/Action	Notes
Any	H	X	X	X	DESELECT (NOP/continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank <i>m</i>	
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (Auto-Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 9
	L	L	H	L	PRECHARGE	
Write (Auto-Precharge Disabled)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 8
	L	H	L	L	WRITE (select column and start new WRITE burst)	7
	L	L	H	L	PRECHARGE	
Read (With Auto-Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start new READ burst)	7, 3a
	L	H	L	L	WRITE (select column and start WRITE burst)	7, 9, 3a
	L	L	H	L	PRECHARGE	
Write (With Auto-Precharge)	L	L	H	H	ACTIVE (select and activate row)	
	L	H	L	H	READ (select column and start READ burst)	7, 3a
	L	H	L	L	WRITE (select column and start new WRITE burst)	7, 3a
	L	L	H	L	PRECHARGE	

Notes: 1. This table applies when  $CKE_{n-1}$  was HIGH and  $CKE_n$  is HIGH (see Truth Table 2) and after  $t^*_{XSNR}$  has been met (if the previous state was self refresh).

2. This table describes alternate bank operation, except where noted (i.e., the current state is for bank *n* and the commands shown are those allowed to be issued to bank *m*, assuming that bank *m* is in such a state that the given command is allowable). Exceptions are covered in the notes below.

3. Current state definitions:

- Idle: The bank has been precharged, and  $t^*_{RP}$  has been met.
- Row Active: A row in the bank has been activated, and  $t^*_{RCD}$  has been met. No data bursts/accesses and no register accesses are in progress.
- Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
- Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
- Read with Auto Precharge Enabled: See following text – 3a
- Write with Auto Precharge Enabled: See following text – 3a
  - a. The read with auto precharge enabled or write with auto precharge enabled states can each be broken into two parts: the access period and the precharge period. For read with auto precharge, the precharge period is defined as if the same burst was executed with auto precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all of the data in the burst. For write with auto precharge, the precharge period begins when  $t^*_{WR}$  ends, with  $t^*_{WR}$  measured as if auto precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or  $t^*_{RP}$ ) begins.

This device supports concurrent auto precharge such that when a read with auto precharge is enabled or a write with auto precharge is enabled any command to other banks is allowed, as long as that command does not interrupt the read or write data transfer already in process. In either case, all other related limitations apply (e.g., contention between read data and write data must be avoided).

- b. The minimum delay from a read or write command with auto precharge enabled, to a command to a different bank is summarized below.

**Table 13: Minimum Delay Summary**

$CL_{RU}$  = CAS Latency (CL) rounded up to the next integer BL = Bust Length

From Command	To Command	Minimum Delay (with Concurrent Auto Precharge)
WRITE w/AP	READ or READ w/AP	$[1 + (BL/2)] * t_{CK} + t_{WTR}$
	WRITE or WRITE w/AP	$(BL/2) * t_{CK}$
	PRECHARGE	$1 t_{CK}$
	ACTIVE	$1 t_{CK}$
READ w/AP	READ or READ w/AP	$(BL/2) * t_{CK}$
	WRITE or WRITE w/AP	$[CL_{RU} + (BL/2)] * t_{CK}$
	PRECHARGE	$1 t_{CK}$
	ACTIVE	$1 t_{CK}$

4. AUTO REFRESH and LOAD MODE REGISTER commands may only be issued when all banks are idle.
5. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. All states and sequences not shown are illegal or reserved.
7. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
8. Requires appropriate DM masking.
9. A WRITE command may be applied after the completion of the READ burst; otherwise, a BURST TERMINATE must be used to end the READ burst prior to asserting a WRITE command.

## Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

VDD Supply Voltage Relative to VSS	-1V to +3.6V
VDDQ Supply Voltage Relative to VSS	-1V to +3.6V
VREF and Inputs Voltage Relative to VSS	-1V to +3.6V
I/O Pins Voltage Relative to VSS	-0.5V to VDDQ +0.5V
Operating Temperature, T <sub>A</sub> (ambient, Commercial)	0°C to +70°C
Operating Temperature, T <sub>A</sub> (ambient, Industrial)	-40°C to +85°C
Storage Temperature (plastic)	-55°C to +150°C
Short Circuit Output Current	50mA

## Parameter Tables

**Table 14: DC Electrical Characteristics and Operating Conditions (-6, -6T, -75E, -75Z, -75)**  
0°C ≤ T<sub>A</sub> ≤ +70°C; VDDQ = +2.5V ±0.2V, VDD = +2.5V ±0.2V; notes: 1-5, 16, notes appear on page 69-74

Parameter/Condition	Symbol	Min	Max	Units	Notes
Supply Voltage	VDD	2.3	2.7	V	11, 9
I/O Supply Voltage	VDDQ	2.3	2.7	V	11, 9 12
I/O Reference Voltage	VREF	0.49 x VDDQ	0.51 x VDDQ	V	6, 12
I/O Termination Voltage (system)	VTT	VREF - 0.04	VREF + 0.04	V	7, 12
Input High (Logic 1) Voltage	V <sub>IH(DC)</sub>	VREF + 0.15	VDD + 0.3	V	28
Input Low (Logic 0) Voltage	V <sub>IL(DC)</sub>	-0.3	VREF - 0.15	V	28
INPUT LEAKAGE CURRENT Any input 0V ≤ V <sub>IN</sub> ≤ VDD, VREF PIN 0V ≤ V <sub>IN</sub> ≤ 1.35V (All other pins not under test = 0V)	I <sub>I</sub>	-2	2	μA	
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V ≤ V <sub>OUT</sub> ≤ VDDQ)	I <sub>OZ</sub>	-5	5	μA	
OUTPUT LEVELS: Full drive option - x4, x8, x16 High Current (V <sub>OUT</sub> = VDDQ - 0.373V, minimum VREF, minimum VTT)	I <sub>OH</sub>	-16.8	-	mA	12, 7
Low Current (V <sub>OUT</sub> = 0.373V, maximum VREF, maximum VTT)	I <sub>OL</sub>	16.8	-	mA	
OUTPUT LEVELS: Reduced drive option - x16 only High Current (V <sub>OUT</sub> = VDDQ - 0.763V, minimum VREF, minimum VTT)	I <sub>OHR</sub>	-9	-	mA	6, 7
Low Current (V <sub>OUT</sub> = 0.763V, maximum VREF, maximum VTT)	I <sub>OLR</sub>	9	-	mA	

**Table 15: DC Electrical Characteristics and Operating Conditions (-5B DDR400)**
 $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ ;  $V_{DDQ} = +2.6\text{V} \pm 0.1\text{V}$ ,  $V_{DD} = +2.6\text{V} \pm 0.1\text{V}$ ; notes: 1–5, 16, and 21; Notes appear on page 69-74

Parameter/Condition	Symbol	Min	Max	Units	Notes
Supply Voltage	$V_{DD}$	2.5	2.7	V	11, 9, 20
I/O Supply Voltage	$V_{DDQ}$	2.5	2.7	V	11, 9, 12, 20
I/O Reference Voltage	$V_{REF}$	$0.49 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	6, 12
I/O Termination Voltage (system)	$V_{TT}$	$V_{REF} - 0.04$	$V_{REF} + 0.04$	V	7, 12
Input High (Logic 1) Voltage	$V_{IH(DC)}$	$V_{REF} + 0.15$	$V_{DD} + 0.3$	V	28
Input Low (Logic 0) Voltage	$V_{IL(DC)}$	-0.3	$V_{REF} - 0.15$	V	28
INPUT LEAKAGE CURRENT Any input $0\text{V} \leq V_{IN} \leq V_{DD}$ , $V_{REF}$ PIN $0\text{V} \leq V_{IN} \leq 1.35\text{V}$ (All other pins not under test = 0V)	$I_i$	-2	2	$\mu\text{A}$	
OUTPUT LEAKAGE CURRENT (DQs are disabled; $0\text{V} \leq V_{OUT} \leq V_{DDQ}$ )	$I_{OZ}$	-5	5	$\mu\text{A}$	
OUTPUT LEVELS: Full drive option - x4, x8, x16 High Current ( $V_{OUT} = V_{DDQ} - 0.373\text{V}$ , minimum $V_{REF}$ , minimum $V_{TT}$ )	$I_{OH}$	-16.8	-	mA	12, 7
Low Current ( $V_{OUT} = 0.373\text{V}$ , maximum $V_{REF}$ , maximum $V_{TT}$ )	$I_{OL}$	16.8	-	mA	
OUTPUT LEVELS: Reduced drive option - x16 only High Current ( $V_{OUT} = V_{DDQ} - 0.763\text{V}$ , minimum $V_{REF}$ , minimum $V_{TT}$ )	$I_{OHR}$	-9	-	mA	6, 7
Low Current ( $V_{OUT} = 0.763\text{V}$ , maximum $V_{REF}$ , maximum $V_{TT}$ )	$I_{OLR}$	9	-	mA	

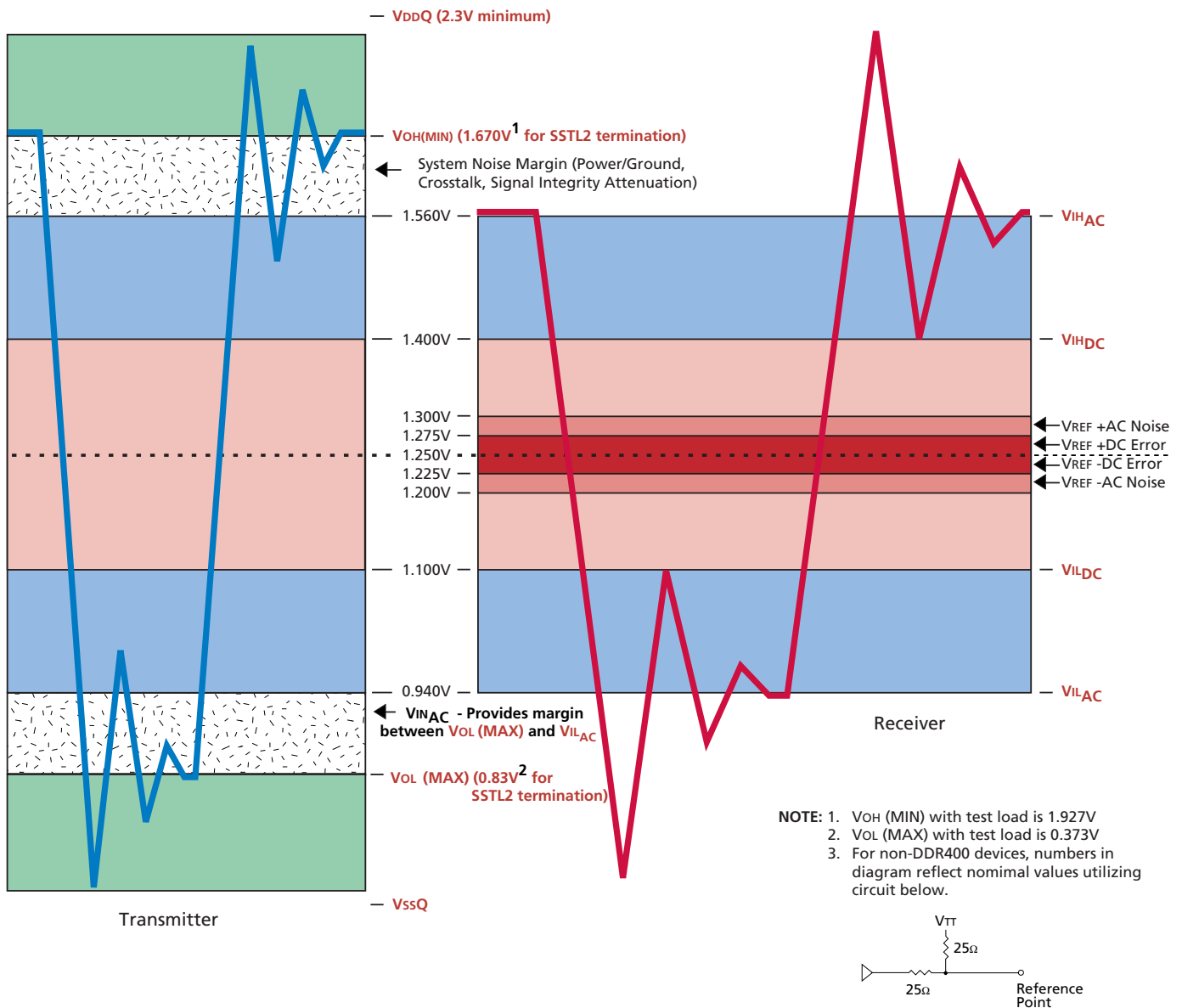
**Table 16: AC Input Operating Conditions**

$0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ ;  $V_{DDQ} = V_{DD} = +2.5\text{V} \pm 0.2\text{V}$  ( $V_{DDQ} = V_{DD} = +2.6\text{V} \pm 0.1\text{V}$  for DDR400); notes: 1–5, 16

Notes appear on page 69-74

Parameter/Condition	Symbol	Min	Max	Units	Notes
Input High (Logic 1) Voltage	$V_{IH(AC)}$	$V_{REF} + 0.310$	-	V	14, 28, 8
Input Low (Logic 0) Voltage	$V_{IL(AC)}$	-	$V_{REF} - 0.310$	V	14, 28, 8
I/O Reference Voltage	$V_{REF(AC)}$	$0.49 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	6

**Figure 33: Input Voltage Waveform**





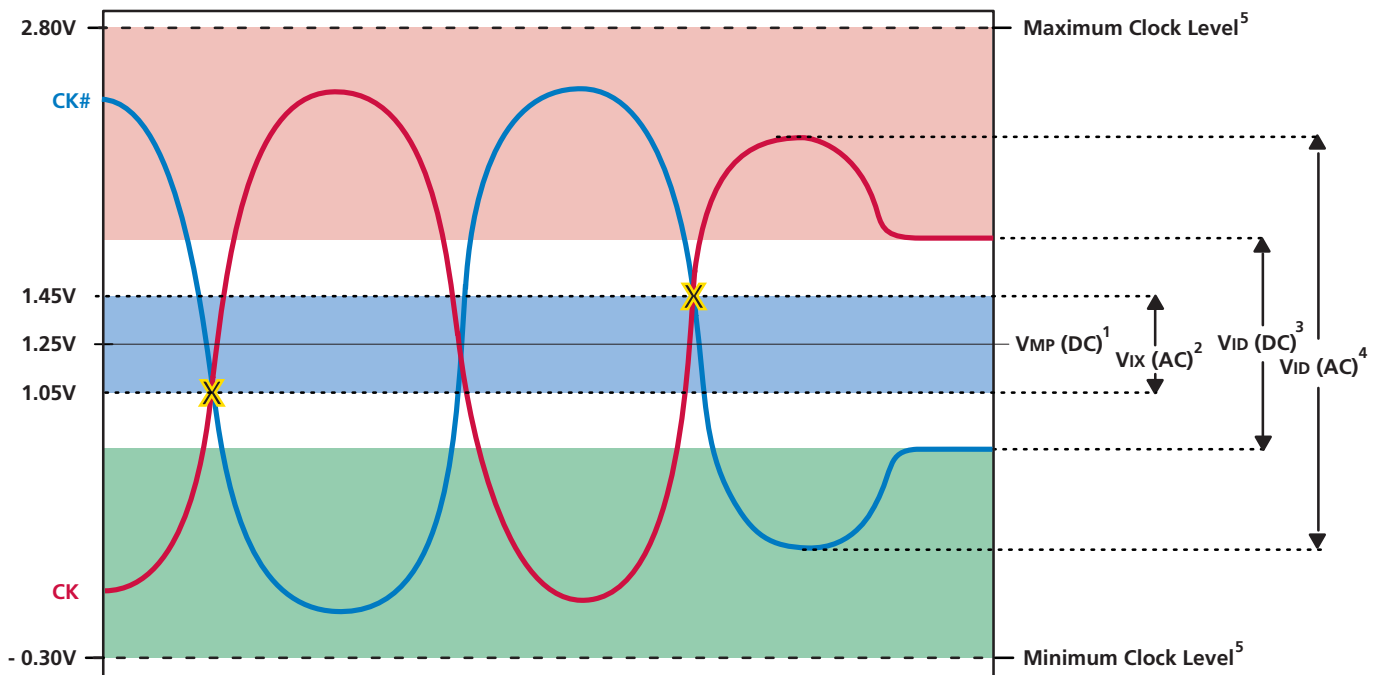
**Table 17: Clock Input Operating Conditions**

$0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ ;  $V_{DDQ} = V_{DD} = +2.5\text{V} \pm 0.2\text{V}$  ( $V_{DDQ} = V_{DD} = +2.6\text{V} \pm 0.1\text{V}$  for DDR400)

Notes: 1–5, 15, 16, 5; notes appear on page 69-74

Parameter/Condition	Symbol	Min	Max	Units	Notes
Clock Input Mid-Point Voltage; CK and CK#	$V_{MP(DC)}$	1.15	1.35	V	6, 9
Clock Input Voltage Level; CK and CK#	$V_{IN(DC)}$	-0.3	$V_{DDQ} + 0.3$	V	6
Clock Input Differential Voltage; CK and CK#	$V_{ID(DC)}$	0.36	$V_{DDQ} + 0.6$	V	6, 8
Clock Input Differential Voltage; CK and CK#	$V_{ID(AC)}$	0.7	$V_{DDQ} + 0.6$	V	8
Clock Input Crossing Point Voltage; CK and CK#	$V_{IX(AC)}$	$0.5 \times V_{DDQ} - 0.2$	$0.5 \times V_{DDQ} + 0.2$	V	9

**Figure 34: SSTL\_2 Clock Input**



- Notes:
1. This provides a minimum of 1.15V to a maximum of 1.35V, and is always half of  $V_{DDQ}$ .
  2. CK and CK# must cross in this region.
  3. CK and CK# must meet at least  $V_{ID(DC)}$  min when static and is centered around  $V_{MP(DC)}$
  4. CK and CK# must have a minimum 700mv peak to peak swing.
  5. CK or CK# may not be more positive than  $V_{DDQ} + 0.3\text{V}$  or more negative than  $V_{SS} - 0.3\text{V}$ .
  6. For AC operation, all DC clock requirements must also be satisfied.
  7. Numbers in diagram reflect nominal values, for non-DDR400 devices.

**Table 18: Capacitance (x4, x8 TSOP)**

Note: 13; notes appear on page 69-74

Parameter	Symbol	Min	Max	Units	Notes
Delta Input/Output Capacitance: DQ0-DQ3 (x4), DQ0-DQ7 (x8)	DC <sub>IO</sub>	–	0.50	pF	24
Delta Input Capacitance: Command and Address	DC <sub>I1</sub>	–	0.50	pF	4
Delta Input Capacitance: CK, CK#	DC <sub>I2</sub>	–	0.25	pF	4
Input/Output Capacitance: DQs, DQS, DM	C <sub>IO</sub>	4.0	5.0	pF	
Input Capacitance: Command and Address	C <sub>I1</sub>	2.0	3.0	pF	
Input Capacitance: CK, CK#	C <sub>I2</sub>	2.0	3.0	pF	
Input Capacitance: CKE	C <sub>I3</sub>	2.0	3.0	pF	

**Table 19: Capacitance (x4, x8 FBGA)**

Note: 13; notes appear on page 69-74

Parameter	Symbol	Min	Max	Units	Notes
Delta Input/Output Capacitance: DQs, DQS, DM	DC <sub>IO</sub>	–	0.50	pF	24
Delta Input Capacitance: Command and Address	DC <sub>I1</sub>	–	0.50	pF	4
Delta Input Capacitance: CK, CK#	DC <sub>I2</sub>	–	0.25	pF	4
Input/Output Capacitance: DQs, DQS, DM	C <sub>IO</sub>	3.5	4.5	pF	
Input Capacitance: Command and Address	C <sub>I1</sub>	1.5	2.5	pF	
Input Capacitance: CK, CK#	C <sub>I2</sub>	1.5	2.5	pF	
Input Capacitance: CKE	C <sub>I3</sub>	1.5	2.5	pF	

**Table 20: Capacitance (x16 TSOP)**

Note: 13; notes appear on page 69-74

Parameter	Symbol	Min	Max	Units	Notes
Delta Input/Output Capacitance: DQ0-DQ7, LDQS, LDM	DC <sub>IO</sub> L	–	0.50	pF	24
Delta Input/Output Capacitance: DQ8-DQ15, UDQS, UDM	DC <sub>IO</sub> U	–	0.50	pF	24
Delta Input Capacitance: Command and Address	DC <sub>I1</sub>	–	0.50	pF	4
Delta Input Capacitance: CK, CK#	DC <sub>I2</sub>	–	0.25	pF	4
Input/Output Capacitance: DQ, LDQS, UDQS, LDM, UDM	C <sub>IO</sub>	4.0	5.0	pF	
Input Capacitance: Command and Address	C <sub>I1</sub>	2.0	3.0	pF	
Input Capacitance: CK, CK#	C <sub>I2</sub>	2.0	3.0	pF	
Input Capacitance: CKE	C <sub>I3</sub>	2.0	3.0	pF	

**Table 21: I<sub>DD</sub> Specifications and Conditions (x4, x8; -5B)**
 $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ ;  $V_{DDQ} = +2.6\text{V} \pm 0.1\text{V}$ ,  $V_{DD} = +2.6\text{V} \pm 0.1\text{V}$ 

 Notes: 1–5, 10, 12, 14, 14; notes appear on page 69-74; See also Table 26, I<sub>DD</sub> Test Cycle Times, on page 64

Parameter/Condition	Symbol	Max		Units	Notes
		-5B			
OPERATING CURRENT: One bank; Active-Precharge; $t_{RC} = t_{RC}(\text{MIN})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	I <sub>DD0</sub>	115		mA	22, 15
OPERATING CURRENT: One bank; Active-Read-Precharge; Burst = 2; $t_{RC} = t_{RC}(\text{MIN})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; I <sub>OUT</sub> = 0mA; Address and control inputs changing once per clock cycle	I <sub>DD1</sub>	135		mA	22, 15
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$ ; CKE = (LOW)	I <sub>DD2P</sub>	3		mA	23, 7
IDLE STANDBY CURRENT: CS# = HIGH; All banks are idle; $t_{CK} = t_{CK}(\text{MIN})$ ; CKE = HIGH; Address and other control inputs changing once per clock cycle. $V_{IN} = V_{REF}$ for DQ, DQS, and DM	I <sub>DD2F</sub>	50		mA	18
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$ ; CKE = LOW	I <sub>DD3P</sub>	25		mA	23, 7
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One bank active; $t_{RC} = t_{RAS}(\text{MAX})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	I <sub>DD3N</sub>	50		mA	22
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$ ; I <sub>OUT</sub> = 0mA	I <sub>DD4R</sub>	135		mA	22, 15
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$ ; DQ, DM, and DQS inputs changing twice per clock cycle	I <sub>DD4W</sub>	155		mA	22
AUTO REFRESH BURST CURRENT:	$t_{REFC} = t_{RC}(\text{MIN})$	I <sub>DD5</sub>	240	mA	17
	$t_{REFC} = 15.6\mu\text{s}$	I <sub>DD5A</sub>	6	mA	27, 17
SELF REFRESH CURRENT: CKE $\leq$ 0.2V	Standard	I <sub>DD6</sub>	4	mA	11
	Low Power (L)	I <sub>DD6A</sub>	1.3	mA	11
OPERATING CURRENT: Four bank interleaving READs (Burst = 4) with auto precharge, $t_{RC} =$ minimum t <sub>RC</sub> allowed; $t_{CK} = t_{CK}(\text{MIN})$ ; Address and control inputs change only during Active READ, or WRITE commands	I <sub>DD7</sub>	355		mA	22, 16

**Table 22: IDD Specifications and Conditions (x4, x8; -6/-6T/-75E)**
 $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ ;  $V_{DDQ} = +2.5\text{V} \pm 0.2\text{V}$ ,  $V_{DD} = +2.5\text{V} \pm 0.2\text{V}$ 

Notes: 1–5, 10, 12, 14, 14; notes appear on page 69-74; See also Table 26, Idd Test Cycle Times, on page 64

Parameter/Condition	Symbol	Max		Units	Notes	
		-6/6T	-75E			
OPERATING CURRENT: One bank; Active-Precharge; $t_{RC} = t_{RC}(\text{MIN})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	IDD0	125	110	mA	22, 15	
OPERATING CURRENT: One bank; Active-Read-Precharge; Burst = 2; $t_{RC} = t_{RC}(\text{MIN})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; $I_{OUT} = 0\text{mA}$ ; Address and control inputs changing once per clock cycle	IDD1	135	120	mA	22, 15	
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$ ; CKE = (LOW)	IDD2P	3	3	mA	23, 7	
IDLE STANDBY CURRENT: CS# = HIGH; All banks are idle; $t_{CK} = t_{CK}(\text{MIN})$ ; CKE = HIGH; Address and other control inputs changing once per clock cycle. $V_{IN} = V_{REF}$ for DQ, DQS, and DM	IDD2F	45	45	mA	18	
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$ ; CKE = LOW	IDD3P	25	25	mA	23, 7	
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One bank active; $t_{RC} = t_{RAS}(\text{MAX})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	IDD3N	50	50	mA	22	
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$ ; $I_{OUT} = 0\text{mA}$	IDD4R	140	130	mA	22, 15	
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$ ; DQ, DM, and DQS inputs changing twice per clock cycle	IDD4W	140	125	mA	22	
AUTO REFRESH BURST CURRENT:	$t_{REFC} = t_{RC}(\text{MIN})$	IDD5	265	220	mA	17
	$t_{REFC} = 15.6\mu\text{s}$	IDD5A	5	5	mA	27, 17
SELF REFRESH CURRENT: CKE $\leq 0.2\text{V}$	Standard	IDD6	3	3	mA	11
	Low Power (L)	IDD6A	1.3	1.3	mA	11
OPERATING CURRENT: Four bank interleaving READs (Burst = 4) with auto precharge, $t_{RC} = \text{minimum } t_{RC} \text{ allowed}$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; Address and control inputs change only during Active READ, or WRITE commands	IDD7	355	330	mA	22, 16	

**Table 23: Idd Specifications and Conditions (x4, x8; -75Z/-75)**
 $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ ;  $V_{DDQ} = +2.5\text{V} \pm 0.2\text{V}$ ,  $V_{DD} = +2.5\text{V} \pm 0.2\text{V}$ 

Notes: 1–5, 10, 12, 14, 14; notes appear on page 69-74; See also Table 26, Idd Test Cycle Times, on page 64

Parameter/Condition	Symbol	Max		Units	Notes
		-75Z/-75			
OPERATING CURRENT: One bank; Active-Precharge; $t_{RC} = t_{RC}(\text{MIN})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	I <sub>DD0</sub>	105		mA	22, 15
OPERATING CURRENT: One bank; Active-Read-Precharge; Burst = 2; $t_{RC} = t_{RC}(\text{MIN})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; I <sub>OUT</sub> = 0mA; Address and control inputs changing once per clock cycle	I <sub>DD1</sub>	120		mA	22, 15
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$ ; CKE = (LOW)	I <sub>DD2P</sub>	3		mA	23, 7
IDLE STANDBY CURRENT: CS# = HIGH; All banks are idle; $t_{CK} = t_{CK}(\text{MIN})$ ; CKE = HIGH; Address and other control inputs changing once per clock cycle. $V_{IN} = V_{REF}$ for DQ, DQS, and DM	I <sub>DD2F</sub>	40		mA	18
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$ ; CKE = LOW	I <sub>DD3P</sub>	20		mA	23, 7
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One bank active; $t_{RC} = t_{RAS}(\text{MAX})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	I <sub>DD3N</sub>	45		mA	22
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$ ; I <sub>OUT</sub> = 0mA	I <sub>DD4R</sub>	125		mA	22, 15
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$ ; DQ, DM, and DQS inputs changing twice per clock cycle	I <sub>DD4W</sub>	120		mA	22
AUTO REFRESH BURST CURRENT:	$t_{REFC} = t_{RC}(\text{MIN})$	I <sub>DD5</sub>	220	mA	17
	$t_{REFC} = 15.6\mu\text{s}$	I <sub>DD5A</sub>	5	mA	27, 17
SELF REFRESH CURRENT: CKE $\leq$ 0.2V	Standard	I <sub>DD6</sub>	2	mA	11
	Low Power (L)	I <sub>DD6A</sub>	1.3	mA	11
OPERATING CURRENT: Four bank interleaving READs (Burst = 4) with auto precharge, $t_{RC} =$ minimum t <sub>RC</sub> allowed; $t_{CK} = t_{CK}(\text{MIN})$ ; Address and control inputs change only during Active READ, or WRITE commands	I <sub>DD7</sub>	325		mA	22, 16

**Table 24: Idd Specifications and Conditions (x16; -6/-6T/-75E)**
 $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ ;  $V_{DDQ} = +2.5\text{V} \pm 0.2\text{V}$ ,  $V_{DD} = +2.5\text{V} \pm 0.2\text{V}$ 

Notes: 1–5, 10, 12, 14, 14; notes appear on page 69-74; See also Table 26, Idd Test Cycle Times, on page 64

Parameter/Condition	Symbol	Max		Units	Notes	
		-6/6T	-75E			
OPERATING CURRENT: One bank; Active-Precharge; $t_{RC} = t_{RC}(\text{MIN})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	I <sub>DD0</sub>	125	115	mA	22, 15	
OPERATING CURRENT: One bank; Active-Read-Precharge; Burst = 2; $t_{RC} = t_{RC}(\text{MIN})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; I <sub>OUT</sub> = 0mA; Address and control inputs changing once per clock cycle	I <sub>DD1</sub>	135	135	mA	22, 15	
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$ ; CKE = (LOW)	I <sub>DD2P</sub>	3	3	mA	23, 7	
IDLE STANDBY CURRENT: CS# = HIGH; All banks are idle; $t_{CK} = t_{CK}(\text{MIN})$ ; CKE = HIGH; Address and other control inputs changing once per clock cycle. $V_{IN} = V_{REF}$ for DQ, DQS, and DM	I <sub>DD2F</sub>	45	45	mA	18	
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$ ; CKE = LOW	I <sub>DD3P</sub>	25	25	mA	23, 7	
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One bank active; $t_{RC} = t_{RAS}(\text{MAX})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	I <sub>DD3N</sub>	50	50	mA	22	
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$ ; I <sub>OUT</sub> = 0mA	I <sub>DD4R</sub>	145	140	mA	22, 15	
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$ ; DQ, DM, and DQS inputs changing twice per clock cycle	I <sub>DD4W</sub>	155	135	mA	22	
AUTO REFRESH BURST CURRENT:	$t_{REFC} = t_{RC}(\text{MIN})$	I <sub>DD5</sub>	265	250	mA	17
	$t_{REFC} = 15.6\mu\text{s}$	I <sub>DD5A</sub>	5	5	mA	27, 17
SELF REFRESH CURRENT: CKE $\leq$ 0.2V	Standard	I <sub>DD6</sub>	3	3	mA	11
	Low Power (L)	I <sub>DD6A</sub>	1.3	1.3	mA	11
OPERATING CURRENT: Four bank interleaving READs (Burst = 4) with auto precharge, $t_{RC} =$ minimum t <sub>RC</sub> allowed; $t_{CK} = t_{CK}(\text{MIN})$ ; Address and control inputs change only during Active READ, or WRITE commands	I <sub>DD7</sub>	385	375	mA	22, 16	

**Table 25: Idd Specifications and Conditions (x16; -75Z/-75)**
 $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ ;  $V_{DDQ} = +2.5\text{V} \pm 0.2\text{V}$ ,  $V_{DD} = +2.5\text{V} \pm 0.2\text{V}$ 

Notes: 1–5, 10, 12, 14, 14; notes appear on page 69-74; See also Table 26, Idd Test Cycle Times, on page 64

Parameter/Condition	Symbol	Max		Units	Notes
		-75Z/-75			
OPERATING CURRENT: One bank; Active-Precharge; $t_{RC} = t_{RC}(\text{MIN})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	I <sub>DD0</sub>	110		mA	22, 15
OPERATING CURRENT: One bank; Active-Read-Precharge; Burst = 2; $t_{RC} = t_{RC}(\text{MIN})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; $I_{OUT} = 0\text{mA}$ ; Address and control inputs changing once per clock cycle	I <sub>DD1</sub>	125		mA	22, 15
PRECHARGE POWER-DOWN STANDBY CURRENT: All banks idle; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$ ; CKE = (LOW)	I <sub>DD2P</sub>	3		mA	23, 7
IDLE STANDBY CURRENT: CS# = HIGH; All banks are idle; $t_{CK} = t_{CK}(\text{MIN})$ ; CKE = HIGH; Address and other control inputs changing once per clock cycle. $V_{IN} = V_{REF}$ for DQ, DQS, and DM	I <sub>DD2F</sub>	40		mA	18
ACTIVE POWER-DOWN STANDBY CURRENT: One bank active; Power-down mode; $t_{CK} = t_{CK}(\text{MIN})$ ; CKE = LOW	I <sub>DD3P</sub>	20		mA	23, 7
ACTIVE STANDBY CURRENT: CS# = HIGH; CKE = HIGH; One bank active; $t_{RC} = t_{RAS}(\text{MAX})$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	I <sub>DD3N</sub>	45		mA	22
OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$ ; $I_{OUT} = 0\text{mA}$	I <sub>DD4R</sub>	135		mA	22, 15
OPERATING CURRENT: Burst = 2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; $t_{CK} = t_{CK}(\text{MIN})$ ; DQ, DM, and DQS inputs changing twice per clock cycle	I <sub>DD4W</sub>	130		mA	22
AUTO REFRESH BURST CURRENT:	$t_{REFC} = t_{RC}(\text{MIN})$	I <sub>DD5</sub>	250	mA	17
	$t_{REFC} = 15.6\mu\text{s}$	I <sub>DD5A</sub>	5	mA	27, 17
SELF REFRESH CURRENT: CKE $\leq 0.2\text{V}$	Standard	I <sub>DD6</sub>	2	mA	11
	Low Power (L)	I <sub>DD6A</sub>	1.3	mA	11
OPERATING CURRENT: Four bank interleaving READs (Burst = 4) with auto precharge, $t_{RC} = \text{minimum } t_{RC} \text{ allowed}$ ; $t_{CK} = t_{CK}(\text{MIN})$ ; Address and control inputs change only during Active READ, or WRITE commands	I <sub>DD7</sub>	375		mA	22, 16

**Table 26: IDD Test Cycle Times**

Values reflect number of clock cycles for each test.

IDD Test	Speed Grade	Clock Cycle Time	t <sub>RRD</sub>	t <sub>RCD</sub>	t <sub>RAS</sub>	t <sub>RP</sub>	t <sub>RC</sub>	t <sub>RFC</sub>	t <sub>REFI</sub>	CL
IDD0	-75/75Z	7.5ns	NA	NA	6	3	9	NA	NA	NA
	-75E	7.5ns	NA	NA	6	2	8	NA	NA	NA
	-6/-6T	6ns	NA	NA	7	3	10	NA	NA	NA
	-5B	5ns	NA	NA	8	3	11	NA	NA	NA
IDD1	-75	7.5ns	NA	NA	6	3	9	NA	NA	2.5
	-75Z	7.5ns	NA	NA	6	3	9	NA	NA	2
	-75E	7.5ns	NA	NA	6	2	8	NA	NA	2
	-6/-6T	6ns	NA	NA	7	3	10	NA	NA	2.5
	-5B	5ns	NA	NA	NA	NA	NA	NA	NA	3
IDD4R	-75	7.5ns	NA	NA	NA	NA	NA	NA	NA	2.5
	-75Z	7.5ns	NA	NA	NA	NA	NA	NA	NA	2
	-75E	7.5ns	NA	NA	NA	NA	NA	NA	NA	2
	-6/-6T	6ns	NA	NA	NA	NA	NA	NA	NA	2.5
	-5B	5ns	NA	NA	NA	NA	NA	NA	NA	3
IDD4W	-75	7.5ns	NA	NA	NA	NA	NA	NA	NA	NA
	-75Z	7.5ns	NA	NA	NA	NA	NA	NA	NA	NA
	-75E	7.5ns	NA	NA	NA	NA	NA	NA	NA	NA
	-6/-6T	6ns	NA	NA	NA	NA	NA	NA	NA	NA
	-5B	5ns	NA	NA	NA	NA	NA	NA	NA	NA
IDD5	-75/75Z	7.5ns	NA	NA	NA	NA	NA	10	10	NA
	-75E	7.5ns	NA	NA	NA	NA	NA	9	9	NA
	-6/-6T	6ns	NA	NA	NA	NA	NA	12	12	NA
	-5B	5ns	NA	NA	NA	NA	NA	14	14	NA
IDD5A	-75/75Z	7.5ns	NA	NA	NA	NA	NA	10	1,030	NA
	-75E	7.5ns	NA	NA	NA	NA	NA	9	1,031	NA
	-6/-6T	6ns	NA	NA	NA	NA	NA	12	1,288	NA
	-5B	5ns	NA	NA	NA	NA	NA	14	1,564	NA
IDD7	-75	7.5ns	2/4	3	NA	3	10	NA	NA	2.5
	-75Z	7.5ns	2/4	3	NA	3	10	NA	NA	2
	-75E	7.5ns	2	3	NA	2	8	NA	NA	2
	-6/-6T	6ns	2/4	3	NA	3	10	NA	NA	2.5
	-5B	5ns	2/4	3	NA	3	11	NA	NA	3



**Table 27: Electrical Characteristics and Recommended AC Operating Conditions (-5B)**

 Notes: 1–5, 14–17, 8; notes appear on page 69-74;  $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ ;  $V_{DD} = V_{DDQ} = +2.6\text{V} \pm 0.1\text{V}$ 

AC Characteristics		-5B				
Parameter	Symbol	Min	Max	Units	Notes	
Access window of DQs from CK/CK#	$t_{AC}$	-0.70	+0.70	ns		
CK high-level width	$t_{CH}$	0.45	0.55	$t_{CK}$	5	
CK low-level width	$t_{CL}$	0.45	0.55	$t_{CK}$	5	
Clock cycle time	CL=3	$t_{CK} (3)$	5	7.5	ns	19
	CL=2.5	$t_{CK} (2.5)$	6	13	ns	13, 19
	CL=2	$t_{CK} (2)$	7.5	13	ns	13, 19
DQ and DM input hold time relative to DQS	$t_{DH}$	0.40		ns	26, 6	
DQ and DM input setup time relative to DQS	$t_{DS}$	0.40		ns	26, 6	
DQ and DM input pulse width (for each input)	$t_{DIPW}$	1.75		ns	6	
Access window of DQS from CK/CK#	$t_{DQSCK}$	-0.6	+0.6	ns		
DQS input high pulse width	$t_{DQSH}$	0.35		$t_{CK}$		
DQS input low pulse width	$t_{DQSL}$	0.35		$t_{CK}$		
DQS-DQ skew, DQS to last DQ valid, per group, per access	$t_{DQSQ}$		0.4	ns	25, 26	
Write command to first DQS latching transition	$t_{DQSS}$	0.72	1.28	$t_{CK}$		
DQS falling edge to CK rising - setup time	$t_{DSS}$	0.2		$t_{CK}$		
DQS falling edge from CK rising - hold time	$t_{DSH}$	0.2		$t_{CK}$		
Half clock period	$t_{HP}$	$t_{CH}, t_{CL}$		ns	9	
Data-out high-impedance window from CK/CK#	$t_{HZ}$		+0.7	ns	18, 10	
Data-out low-impedance window from CK/CK#	$t_{LZ}$	-0.7		ns	18, 10	
Address and control input hold time (fast slew rate)	$t_{IH_F}$	0.6		ns		
Address and control input setup time (fast slew rate)	$t_{IS_F}$	0.6		ns		
Address and control input hold time (slow slew rate)	$t_{IH_S}$	0.6		ns	14	
Address and control input setup time (slow slew rate)	$t_{IS_S}$	0.6		ns	14	
Address and Control input pulse width (for each input)	$t_{IPW}$	2.2		ns		
LOAD MODE REGISTER command cycle time	$t_{MRD}$	10		ns		
DQ-DQS hold, DQS to first DQ to go non-valid, per access	$t_{QH}$	$t_{HP} - t_{QHS}$		ns	25, 26	
Data Hold Skew Factor	$t_{QHS}$		0.5	ns		
ACTIVE to PRECHARGE command	$t_{RAS}$	40	70,000	ns	10	
ACTIVE to READ with Auto precharge command	$t_{RAP}$	15		ns		
ACTIVE to ACTIVE/AUTO REFRESH command period	$t_{RC}$	55		ns		
AUTO REFRESH command period	$t_{RFC}$	70		ns	17	
ACTIVE to READ or WRITE delay	$t_{RCD}$	15		ns		
PRECHARGE command period	$t_{RP}$	15		ns		
DQS read preamble	$t_{RPRE}$	0.9	1.1	$t_{CK}$	11	
DQS read postamble	$t_{RPST}$	0.4	0.6	$t_{CK}$	11	
ACTIVE bank a to ACTIVE bank b command	$t_{RRD}$	10		ns		
DQS write preamble	$t_{WPRE}$	0.25		$t_{CK}$		
DQS write preamble setup time	$t_{WPRES}$	0		ns	20, 21	
DQS write postamble	$t_{WPST}$	0.4	0.6	$t_{CK}$	19	
Write recovery time	$t_{WR}$	15		ns		
Internal WRITE to READ command delay	$t_{WTR}$	2		$t_{CK}$		
Data valid output window (DVW)	N/A		$t_{QH} - t_{DQSQ}$	ns	25	
REFRESH to REFRESH command interval	$t_{REFC}$		140.6	$\mu\text{s}$	23	
Average periodic refresh interval	$t_{REFI}$		15.6	$\mu\text{s}$	23	
Terminating voltage delay to $V_{DD}$	$t_{VTD}$	0		ns		
Exit SELF REFRESH to non-READ command	$t_{XSNR}$	70		ns		
Exit SELF REFRESH to READ command	$t_{XSRD}$	200		$t_{CK}$		

**Table 28: Electrical Characteristics and Recommended AC Operating Conditions (-6/-6T/-75E)**

 Notes: 1–5, 14–17, 8; notes appear on page 69-74;  $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ ;  $V_{DDQ} = +2.5\text{V} \pm 0.2\text{V}$ ,  $V_{DD} = +2.5\text{V} \pm 0.2\text{V}$ 

AC Characteristics		-6 (FBGA)		-6T (TSOP)		-75E				
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Units	Notes	
Access window of DQs from CK/CK#	$t_{AC}$	-0.70	+0.70	-0.70	+0.70	-0.75	+0.75	ns		
CK high-level width	$t_{CH}$	0.45	0.55	0.45	0.55	0.45	0.55	$t_{CK}$	5	
CK low-level width	$t_{CL}$	0.45	0.55	0.45	0.55	0.45	0.55	$t_{CK}$	5	
Clock cycle time	CL=2.5	$t_{CK} (2.5)$	6	13	6	13	7.5	13	ns	13, 19
	CL=2	$t_{CK} (2)$	7.5	13	7.5	13	7.5	13	ns	13, 19
DQ and DM input hold time relative to DQS	$t_{DH}$	0.45		0.45		0.5		ns	26, 6	
DQ and DM input setup time relative to DQS	$t_{DS}$	0.45		0.45		0.5		ns	26, 6	
DQ and DM input pulse width (for each input)	$t_{DIPW}$	1.75		1.75		1.75		ns	6	
Access window of DQS from CK/CK#	$t_{DQSK}$	-0.6	+0.6	-0.6	+0.6	-0.75	+0.75	ns		
DQS input high pulse width	$t_{DQSH}$	0.35		0.35		0.35		$t_{CK}$		
DQS input low pulse width	$t_{DQSL}$	0.35		0.35		0.35		$t_{CK}$		
DQS-DQ skew, DQS to last DQ valid, per group, per access	$t_{DQSQ}$		0.4		0.45		0.5	ns	25, 26	
Write command to first DQS latching transition	$t_{DQSS}$	0.75	1.25	0.75	1.25	0.75	1.25	$t_{CK}$		
DQS falling edge to CK rising - setup time	$t_{DSS}$	0.2		0.2		0.2		$t_{CK}$		
DQS falling edge from CK rising - hold time	$t_{DSH}$	0.2		0.2		0.2		$t_{CK}$		
Half clock period	$t_{HP}$	$t_{CH}, t_{CL}$		$t_{CH}, t_{CL}$		$t_{CH}, t_{CL}$		ns	9	
Data-out high-impedance window from CK/CK#	$t_{HZ}$		+0.7		+0.7		+0.75	ns	18, 10	
Data-out low-impedance window from CK/CK#	$t_{LZ}$	-0.7		-0.7		-0.75		ns	18, 10	
Address and control input hold time (fast slew rate)	$t_{IH_F}$	0.75		0.75		.90		ns		
Address and control input setup time (fast slew rate)	$t_{IS_F}$	0.75		0.75		.90		ns		
Address and control input hold time (slow slew rate)	$t_{IH_S}$	0.8		0.8		1		ns	14	
Address and control input setup time (slow slew rate)	$t_{IS_S}$	0.8		0.8		1		ns	14	
Address and Control input pulse width (for each input)	$t_{IPW}$	2.2		2.2		2.2		ns		
LOAD MODE REGISTER command cycle time	$t_{MRD}$	12		12		15		ns		
DQ-DQS hold, DQS to first DQ to go non-valid, per access	$t_{QH}$	$t_{HP}$ $-t_{QHS}$		$t_{HP}$ $-t_{QHS}$		$t_{HP}$ $-t_{QHS}$		ns	25, 26	
Data Hold Skew Factor	$t_{QHS}$		0.5		0.55		0.75	ns		
ACTIVE to PRECHARGE command	$t_{RAS}$	42	70,000	42	70,000	40	120,000	ns	10, 21	
ACTIVE to READ with Auto precharge command	$t_{RAP}$	15		15		15		ns		
ACTIVE to ACTIVE/AUTO REFRESH command period	$t_{RC}$	60		60		60		ns		
AUTO REFRESH command period	$t_{RFC}$	72		72		75		ns	17	
ACTIVE to READ or WRITE delay	$t_{RCD}$	15		15		15		ns		
PRECHARGE command period	$t_{RP}$	15		15		15		ns		
DQS read preamble	$t_{RPRE}$	0.9	1.1	0.9	1.1	0.9	1.1	$t_{CK}$	11	
DQS read postamble	$t_{RPST}$	0.4	0.6	0.4	0.6	0.4	0.6	$t_{CK}$	11	
ACTIVE bank a to ACTIVE bank b command	$t_{RRD}$	12		12		15		ns		
DQS write preamble	$t_{WPRE}$	0.25		0.25		0.25		$t_{CK}$		
DQS write preamble setup time	$t_{WPRES}$	0		0		0		ns	20, 21	
DQS write postamble	$t_{WPST}$	0.4	0.6	0.4	0.6	0.4	0.6	$t_{CK}$	19	
Write recovery time	$t_{WR}$	15		15		15		ns		
Internal WRITE to READ command delay	$t_{WTR}$	1		1		1		$t_{CK}$		
Data valid output window (DVW)	N/A	$t_{QH} - t_{DQSQ}$		$t_{QH} - t_{DQSQ}$		$t_{QH} - t_{DQSQ}$		ns	25	
REFRESH to REFRESH command interval	$t_{REFC}$		140.6		140.6		140.6	$\mu\text{s}$	23	
Average periodic refresh interval	$t_{REFI}$		15.6		15.6		15.6	$\mu\text{s}$	23	
Terminating voltage delay to V <sub>DD</sub>	$t_{VTD}$	0		0		0		ns		
Exit SELF REFRESH to non-READ command	$t_{XSNR}$	75		75		75		ns		
Exit SELF REFRESH to READ command	$t_{XSRD}$	200		200		200		$t_{CK}$		

**Table 29: Electrical Characteristics and Recommended AC Operating Conditions (-75Z/-75)**

 Notes: 1–5, 14–17, 8; notes appear on page 69-74;  $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ ;  $V_{DDQ} = +2.5\text{V} \pm 0.2\text{V}$ ,  $V_{DD} = +2.5\text{V} \pm 0.2\text{V}$ 

AC Characteristics		-75Z		-75			
Parameter	Symbol	Min	Max	Min	Max	Units	Notes
Access window of DQs from CK/CK#	$t_{AC}$	-0.75	+0.75	-0.75	+0.75	ns	
CK high-level width	$t_{CH}$	0.45	0.55	0.45	0.55	$t_{CK}$	5
CK low-level width	$t_{CL}$	0.45	0.55	0.45	0.55	$t_{CK}$	5
Clock cycle time	CL=2.5 $t_{CK}(2.5)$	7.5	13	7.5	13	ns	13, 19
	CL=2 $t_{CK}(2)$	7.5	13	10	13	ns	13, 19
DQ and DM input hold time relative to DQS	$t_{DH}$	0.5		0.5		ns	26, 6
DQ and DM input setup time relative to DQS	$t_{DS}$	0.5		0.5		ns	26, 6
DQ and DM input pulse width (for each input)	$t_{DIPW}$	1.75		1.75		ns	6
Access window of DQS from CK/CK#	$t_{DQSCK}$	-0.75	+0.75	-0.75	+0.75	ns	
DQS input high pulse width	$t_{DQSH}$	0.35		0.35		$t_{CK}$	
DQS input low pulse width	$t_{DQSL}$	0.35		0.35		$t_{CK}$	
DQS-DQ skew, DQS to last DQ valid, per group, per access	$t_{DQSQ}$		0.5		0.5	ns	25, 26
Write command to first DQS latching transition	$t_{DQSS}$	0.75	1.25	0.75	1.25	$t_{CK}$	
DQS falling edge to CK rising - setup time	$t_{DSS}$	0.2		0.2		$t_{CK}$	
DQS falling edge from CK rising - hold time	$t_{DSH}$	0.2		0.2		$t_{CK}$	
Half clock period	$t_{HP}$	$t_{CH}, t_{CL}$		$t_{CH}, t_{CL}$		ns	9
Data-out high-impedance window from CK/CK#	$t_{HZ}$		+0.75		+0.75	ns	18, 10
Data-out low-impedance window from CK/CK#	$t_{LZ}$	-0.75		-0.75		ns	18, 10
Address and control input hold time (fast slew rate)	$t_{IH_F}$	.90		.90		ns	
Address and control input setup time (fast slew rate)	$t_{IS_F}$	.90		.90		ns	
Address and control input hold time (slow slew rate)	$t_{IH_S}$	1		1		ns	14
Address and control input setup time (slow slew rate)	$t_{IS_S}$	1		1		ns	14
Address and Control input pulse width (for each input)	$t_{IPW}$	2.2		2.2		ns	
LOAD MODE REGISTER command cycle time	$t_{MRD}$	15		15		ns	
DQ-DQS hold, DQS to first DQ to go non-valid, per access	$t_{QH}$	$t_{HP}$ $-t_{QHS}$		$t_{HP}$ $-t_{QHS}$		ns	25, 26
Data Hold Skew Factor	$t_{QHS}$		0.75		0.75	ns	
ACTIVE to PRECHARGE command	$t_{RAS}$	40	120,000	40	120,000	ns	10
ACTIVE to READ with Auto precharge command	$t_{RAP}$	20		20		ns	
ACTIVE to ACTIVE/AUTO REFRESH command period	$t_{RC}$	65		65		ns	
AUTO REFRESH command period	$t_{RFC}$	75		75		ns	17
ACTIVE to READ or WRITE delay	$t_{RCD}$	20		20		ns	
PRECHARGE command period	$t_{RP}$	20		20		ns	
DQS read preamble	$t_{RPRE}$	0.9	1.1	0.9	1.1	$t_{CK}$	11
DQS read postamble	$t_{RPST}$	0.4	0.6	0.4	0.6	$t_{CK}$	11
ACTIVE bank a to ACTIVE bank b command	$t_{RRD}$	15		15		ns	
DQS write preamble	$t_{WPRE}$	0.25		0.25		$t_{CK}$	
DQS write preamble setup time	$t_{WPRES}$	0		0		ns	20, 21
DQS write postamble	$t_{WPST}$	0.4	0.6	0.4	0.6	$t_{CK}$	19
Write recovery time	$t_{WR}$	15		15		ns	
Internal WRITE to READ command delay	$t_{WTR}$	1		1		$t_{CK}$	
Data valid output window (DVW)	N/A	$t_{QH} - t_{DQSQ}$		$t_{QH} - t_{DQSQ}$		ns	25
REFRESH to REFRESH command interval	$t_{REFC}$		140.6		140.6	$\mu\text{s}$	23
Average periodic refresh interval	$t_{REFI}$		15.6		15.6	$\mu\text{s}$	23
Terminating voltage delay to V <sub>DD</sub>	$t_{VTD}$	0		0		ns	
Exit SELF REFRESH to non-READ command	$t_{XSNR}$	75		75		ns	
Exit SELF REFRESH to READ command	$t_{XSRD}$	200		200		$t_{CK}$	

**Table 30: Input Slew Rate Derating Values for Addresses and Commands**
 $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ ;  $V_{DDQ} = +2.5\text{V} \pm 0.2\text{V}$ ,  $V_{DD} = +2.5\text{V} \pm 0.2\text{V}$ ; notes: 14; notes appear on page 69-74

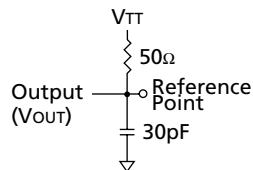
Speed	Slew Rate	$t_{IS}$	$t_{IH}$	Units
-75/-75Z/-75E	$0.5 \text{ V/ns} \leq \text{Slew Rate} < 1.0 \text{ V/ns}$	1.00	1	ns
-75/-75Z/-75E	$0.4 \text{ V/ns} \leq \text{Slew Rate} < 0.5 \text{ V/ns}$	1.05	1	ns
-75/-75Z/-75E	$0.3 \text{ V/ns} \leq \text{Slew Rate} < 0.4 \text{ V/ns}$	1.15	1	ns

**Table 31: Input Slew Rate Derating Values for DQ, DQS, and DM**
 $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ ;  $V_{DDQ} = +2.5\text{V} \pm 0.2\text{V}$ ,  $V_{DD} = +2.5\text{V} \pm 0.2\text{V}$ ; notes: 6; notes appear on page 69-74

Speed	Slew Rate	$t_{DS}$	$t_{DH}$	Units
-75/-75Z/-75E	$0.5 \text{ V/ns} \leq \text{Slew Rate} < 1.0 \text{ V/ns}$	0.50	0.50	ns
-75/-75Z/-75E	$0.4 \text{ V/ns} \leq \text{Slew Rate} < 0.5 \text{ V/ns}$	0.55	0.55	ns
-75/-75Z/-75E	$0.3 \text{ V/ns} \leq \text{Slew Rate} < 0.4 \text{ V/ns}$	0.60	0.60	ns

## Notes

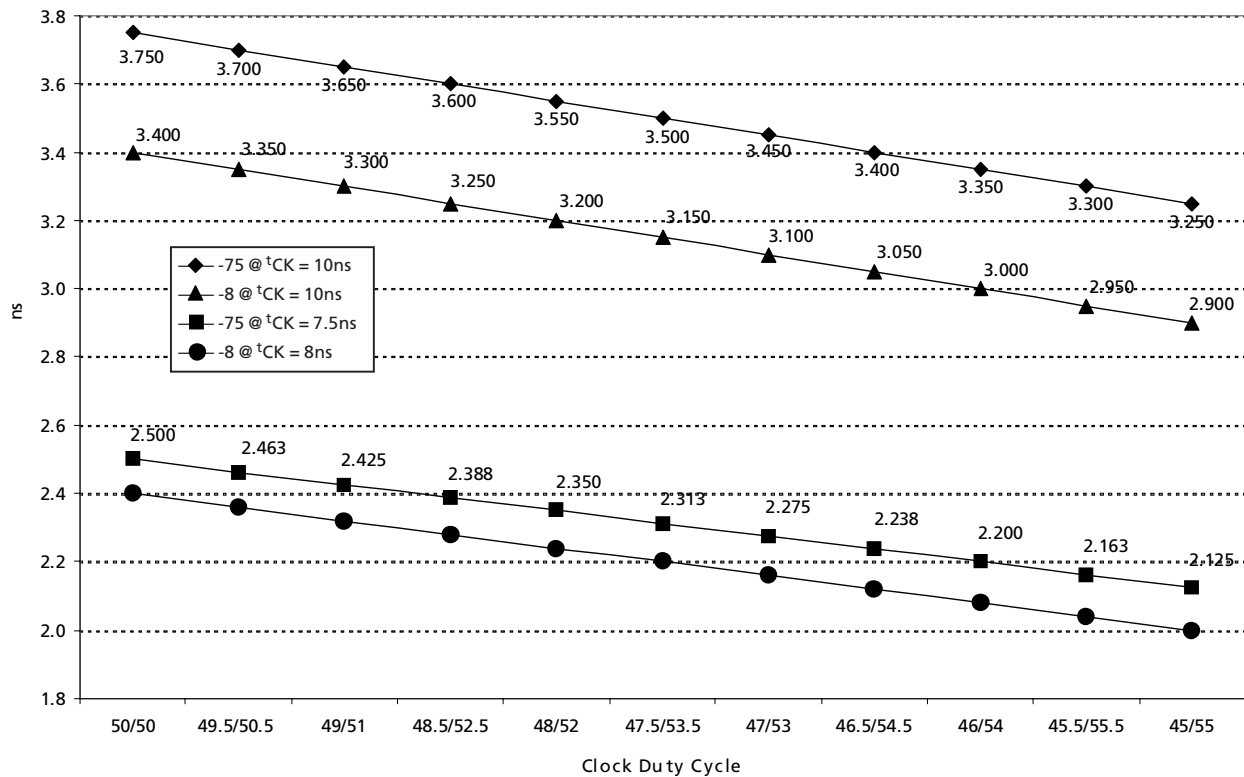
1. All voltages referenced to VSS.
2. Tests for AC timing, IDD, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Outputs (except for IDD measurements) measured with equivalent load:



4. AC timing and IDD tests may use a VIL-to-VIH swing of up to 1.5V in the test environment, but input timing is still referenced to VREF (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between VIL(AC) and VIH(AC).
5. The AC and DC input level specifications are as defined in the SSTL\_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. VREF is expected to equal VDDQ/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on VREF may not exceed  $\pm 2$  percent of the DC value. Thus, from VDDQ/2, VREF is allowed  $\pm 25$ mV for DC error and an additional  $\pm 25$ mV for AC noise. This measurement is to be taken at the nearest VREF by-pass capacitor.
7. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF and must track variations in the DC level of VREF.
8. VID is the magnitude of the difference between the input level on CK and the input level on CK#.
9. The value of VIX and VMP are expected to equal VDDQ/2 of the transmitting device and must track variations in the DC level of the same.
10. IDD is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle times at CL = 3 for -5B, CL = 2.5 for -6/-6T and -75, and CL=2 for -75E/-75Z speeds with the outputs open.
11. Enables on-chip refresh and address counters.
12. IDD specifications are tested after the device is properly initialized, and is averaged at the defined cycle rate.
13. This parameter is sampled. VDD=+2.5V $\pm$ 0.2V, VDDQ=+2.5V $\pm$ 0.2V, VREF=VSS, f=100MHz, TA=25°C VOUT(DC)=VDDQ/2, VOUT (peak to peak)=0.2V. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
14. For slew rates less than 1V/ns and greater than or equal to 0.5V/ns. If slew rate is less than 0.5V/ns, timing must be derated: tIS has an additional 50ps per each 100mV/ns reduction in slew rate from 500mV/ns, while tIH has 0pF is unaffected. If slew rate exceeds 4.5V/ns, functionality is uncertain. For -5B, -6, and -6T speed grades, slew rates must be greater than or equal 0.5V/ns.

15. The CK/CK# input reference level (for timing referenced to CK/CK#) is the point at which CK and CK# cross; the input reference level for signals other than CK/CK# is VREF.
16. Inputs are not recognized as valid until VREF stabilizes. Once initialized, including self refresh mode, VREF must be powered within specified range. Exception: during the period before VREF stabilizes, CKE  $0.3 \times V_{DDQ}$  is recognized as LOW.
17. The output timing reference level, as measured at the timing reference point indicated in Note 3, is VTT.
18. Transitions occur in the same access time windows as data valid transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving ( $t_{HZ}$ ) or begins driving ( $t_{LZ}$ ).
19. The intent of the Don't Care state after completion of the postamble is the DQS-driven signal should either be high, low, or high-Z and that any signal transition within the input switching region must follow valid input requirements. That is, if DQS transitions high (above  $V_{IHDC}(\text{MIN})$ ) then it must not transition low (below  $V_{IHDC}$ ) prior to  $t_{DQSH}(\text{MIN})$ .
20. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
21. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITES were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on  $t_{DQSS}$ .
22. MIN ( $t_{RC}$  or  $t_{RFC}$ ) for IDD measurements is the smallest multiple of  $t_{CK}$  that meets the minimum absolute value for the respective parameter.  $t_{RAS}(\text{MAX})$  for IDD measurements is the largest multiple of  $t_{CK}$  that meets the maximum absolute value for  $t_{RAS}$ .
23. The refresh period is 64ms. This equates to an average refresh rate of 15.625 $\mu$ s. However, an AUTO REFRESH command must be asserted at least once every 140.6 $\mu$ s; burst refreshing or posting by the DRAM controller greater than eight refresh cycles is not allowed.
24. The I/O capacitance per DQS and DQ byte/group will not differ by more than this maximum amount for any given device.
25. The data valid window is derived by achieving other specifications -  $t_{HP}$  ( $t_{CK}/2$ ),  $t_{DQSQ}$ , and  $t_{QH}$  ( $t_{QH} = t_{HP} - t_{QHS}$ ). The data valid window derates in direct proportion to the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycle variation of 45/55, because functionality is uncertain when operating beyond a 45/55 ratio. The data valid window derating curves are provided in Figure 35 on page 71 for duty cycles ranging between 50/50 and 45/55.
26. Referenced to each output group: x4 = DQS with DQ0-DQ3; x8 = DQS with DQ0-DQ7; x16 = LDQS with DQ0-DQ7; and UDQS with DQ8-DQ15.
27. This limit is actually a nominal value and does not result in a fail value. CKE is HIGH during REFRESH command period ( $t_{RFC}(\text{MIN})$ ) else CKE is LOW (i.e., during standby).
28. To maintain a valid level, the transitioning edge of the input must:
  - a. Sustain a constant slew rate from the current AC level through to the target AC level,  $V_{IL}(\text{AC})$  or  $V_{IH}(\text{AC})$ .
  - b. Reach at least the target AC level.
  - c. After the AC target level is reached, continue to maintain at least the target DC level,  $V_{IL}(\text{DC})$  or  $V_{IH}(\text{DC})$ .

Figure 35: Derating Data Valid Window ( $t_{QH} - t_{DQSQ}$ )

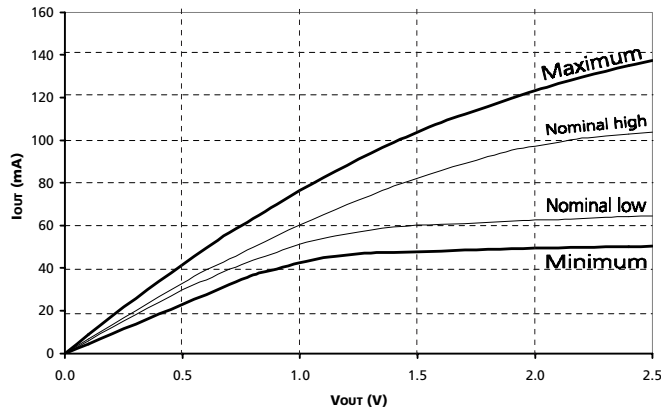


4. The Input capacitance per pin group will not differ by more than this maximum amount for any given device.
5. CK and CK# input slew rate must be  $\geq 1V/ns$  ( $\geq 2V/ns$  if measured differentially).
6. DQ and DM input slew rates must not deviate from DQS by more than 10 percent. If the DQ/DM/DQS slew rate is less than  $0.5V/ns$ , timing must be derated: 50ps must be added to  $t_{DS}$  and  $t_{DH}$  for each  $100mV/ns$  reduction in slew rate. For -6, -6T, and -5B speed grades, slew rate must be  $\geq 0.5V/ns$ . If slew rate exceeds  $4V/ns$ , functionality is uncertain.
7. VDD must not vary more than 4 percent if CKE is not active while any bank is active.
8. The clock is allowed up to  $\pm 150ps$  of jitter. Each timing parameter is allowed to vary by the same amount.
9.  $t_{HP}$  (MIN) is the lesser of  $t_{CL}$  minimum and  $t_{CH}$  minimum actually applied to the device CK and CK# inputs, collectively during bank active.
10. READs and WRITEs with auto precharge are not allowed to be issued until  $t_{RAS}$  (MIN) can be satisfied prior to the internal precharge command being issued.
11. Any positive glitch must be less than 1/3 of the clock cycle and not more than +400mV or 2.9V (+300mV or 2.9V maximum for -5B), whichever is less. Any negative glitch must be less than 1/3 of the clock cycle and not exceed either -300mV or 2.2V, (2.4V for -5B) whichever is more positive. The average cannot be below the +2.5V (2.6V for -5B) minimum.
12. Normal Output Drive Curves:
  - a. The full variation in driver pull-down current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 36

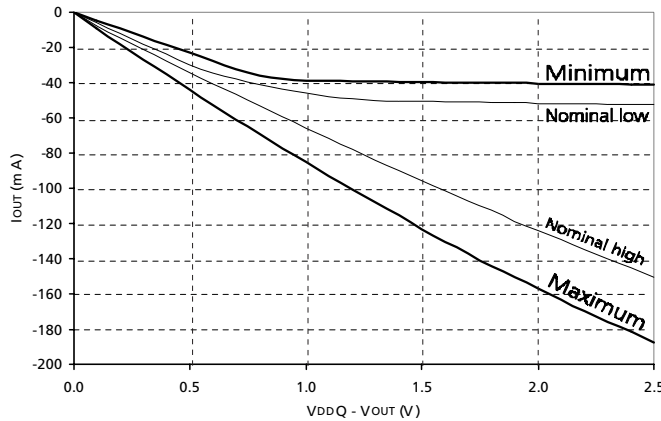


- b. The variation in driver pull-down current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 36.
- c. The full variation in driver pull-up current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 37.
- d. The variation in driver pull-up current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 37.
- e. The full variation in the ratio of the maximum to minimum pull-up and pull-down current should be between 0.71 and 1.4, for device drain-to-source voltages from 0.1V to 1.0V, and at the same voltage and temperature. f) The full variation in the ratio of the nominal pull-up to pull-down current should be unity  $\pm 10$  percent, for device drain-to-source voltages from 0.1V to 1.0V.

**Figure 36: Full Drive Pull-Down Characteristics**



**Figure 37: Full Drive Pull-Up Characteristics**



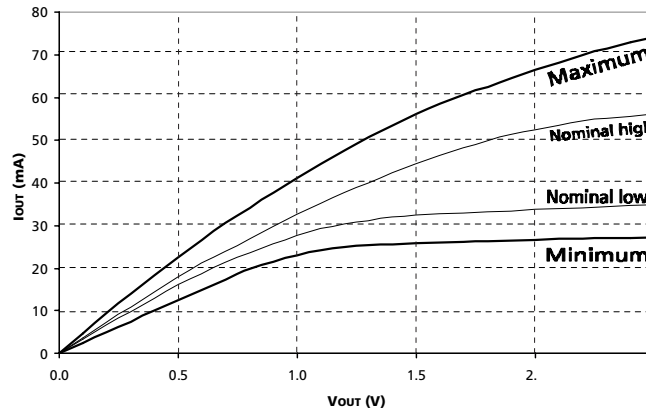
**6. Reduced Output Drive Curves:**

- a. The full variation in driver pull-down current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 38.
- b. The variation in driver pull-down current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 38.
- c. The full variation in driver pull-up current from minimum to maximum process, temperature and voltage will lie within the outer bounding lines of the V-I curve of Figure 39.
- d. The variation in driver pull-up current within nominal limits of voltage and temperature is expected, but not guaranteed, to lie within the inner bounding lines of the V-I curve of Figure 39.

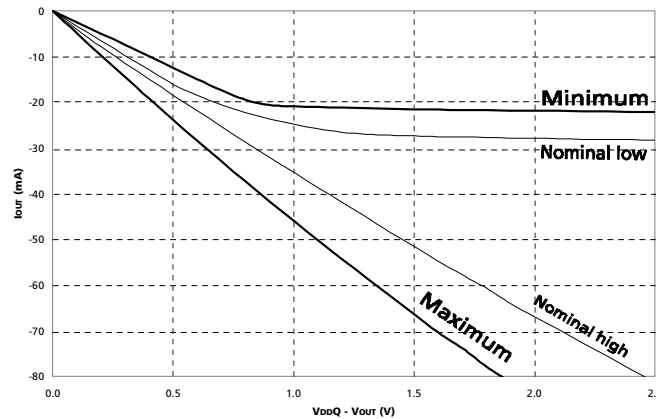


- e. The full variation in the ratio of the maximum to minimum pull-up and pull-down current should be between 0.71 and 1.4 for device drain-to-source voltages from 0.1V to 1.0V, and at the same voltage and temperature.
- f. The full variation in the ratio of the nominal pull-up to pull-down current should be unity  $\pm 10$  percent, for device drain-to-source voltages from 0.1V to 1.0V.

**Figure 38: Reduced Drive Pull-Down Characteristics**



**Figure 39: Reduced Drive Pull-Up Characteristics**



- 7. The voltage levels used are derived from a minimum  $V_{DD}$  level and the referenced test load. In practice, the voltage levels obtained from a properly terminated bus will provide significantly different voltage values.
- 8.  $V_{IH}$  overshoot:  $V_{IH} (MAX) = V_{DDQ} + 1.5V$  for a pulse width  $\leq 3ns$  and the pulse width can not be greater than 1/3 of the cycle rate.  $V_{IL}$  undershoot:  $V_{IL} (MIN) = -1.5V$  for a pulse width  $\leq 3ns$  and the pulse width can not be greater than 1/3 of the cycle rate.
- 9.  $V_{DD}$  and  $V_{DDQ}$  must track each other.
- 10.  $t_{HZ} (MAX)$  will prevail over  $t_{DQSK} (MAX) + t_{RPST} (MAX)$  condition.  $t_{LZ} (MIN)$  will prevail over  $t_{DQSK} (MIN) + t_{RPRE} (MAX)$  condition.
- 11.  $t_{RPST}$  end point and  $t_{RPRE}$  begin point are not referenced to a specific voltage level but specify when the device output is no longer driving ( $t_{RPST}$ ), or begins driving ( $t_{RPRE}$ ).

12. During initialization,  $V_{DDQ}$ ,  $V_{TT}$ , and  $V_{REF}$  must be equal to or less than  $V_{DD} + 0.3V$ . Alternatively,  $V_{TT}$  may be 1.35V maximum during power up, even if  $V_{DD}/V_{DDQ}$  are 0V, provided a minimum of  $42\Omega$  of series resistance is used between the  $V_{TT}$  supply and the input pin.
13. The current Micron part operates below the slowest JEDEC operating frequency of 83 MHz. As such, future die may not reflect this option.
14. When an input signal is HIGH or LOW, it is defined as a steady state logic high or logic low.
15. Random addressing, 50 percent of data changing at every transfer.
16. Random addressing, 100 percent of data changing at every transfer.
17. CKE must be active (HIGH) during the entire time a refresh command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until  $t_{RFC}$  has been satisfied.
18.  $IDD2N$  specifies the DQ, DQS and DM to be driven to a valid high or low logic level.  $IDD2Q$  is similar to  $IDD2F$  except  $IDD2Q$  specifies the address and control inputs to remain stable. Although  $IDD2F$ ,  $IDD2N$ , and  $IDD2Q$  are similar,  $IDD2F$  is "worst case."
19. Whenever the operating frequency is altered, not including jitter, the DLL is required to be reset followed by 200 clock cycles before any READ command.
20. This is the DC voltage supplied at the DRAM and is inclusive of all noise up to 20 MHz. Any noise above 20 MHz at the DRAM generated from any source other than that of the DRAM itself may not exceed the DC voltage range of  $2.6V \pm 100mV$ .
21. The -6/-6T speed grades will operate with  $t_{RAS(min)} = 40ns$  and  $t_{RAS(max)} = 120,000ns$  at any slower frequency.

## Output Drive Characteristics and Timing

**Table 32: Normal Output Drive Characteristics**

Voltage (V)	Pull-Down Current (mA)				Pull-Up Current (mA)			
	Nominal Low	Nominal High	Minimum	Maximum	Nominal Low	Nominal High	Minimum	Maximum
0.1	6.0	6.8	4.6	9.6	-6.1	-7.6	-4.6	-10.0
0.2	12.2	13.5	9.2	18.2	-12.2	-14.5	-9.2	-20.0
0.3	18.1	20.1	13.8	26.0	-18.1	-21.2	-13.8	-29.8
0.4	24.1	26.6	18.4	33.9	-24.0	-27.7	-18.4	-38.8
0.5	29.8	33.0	23.0	41.8	-29.8	-34.1	-23.0	-46.8
0.6	34.6	39.1	27.7	49.4	-34.3	-40.5	-27.7	-54.4
0.7	39.4	44.2	32.2	56.8	-38.1	-46.9	-32.2	-61.8
0.8	43.7	49.8	36.8	63.2	-41.1	-53.1	-36.0	-69.5
0.9	47.5	55.2	39.6	69.9	-43.8	-59.4	-38.2	-77.3
1.0	51.3	60.3	42.6	76.3	-46.0	-65.5	-38.7	-85.2
1.1	54.1	65.2	44.8	82.5	-47.8	-71.6	-39.0	-93.0
1.2	56.2	69.9	46.2	88.3	-49.2	-77.6	-39.2	-100.6
1.3	57.9	74.2	47.1	93.8	-50.0	-83.6	-39.4	-108.1
1.4	59.3	78.4	47.4	99.1	-50.5	-89.7	-39.6	-115.5
1.5	60.1	82.3	47.7	103.8	-50.7	-95.5	-39.9	-123.0
1.6	60.5	85.9	48.0	108.4	-51.0	-101.3	-40.1	-130.4
1.7	61.0	89.1	48.4	112.1	-51.1	-107.1	-40.2	-136.7
1.8	61.5	92.2	48.9	115.9	-51.3	-112.4	-40.3	-144.2
1.9	62.0	95.3	49.1	119.6	-51.5	-118.7	-40.4	-150.5
2.0	62.5	97.2	49.4	123.3	-51.6	-124.0	-40.5	-156.9
2.1	62.8	99.1	49.6	126.5	-51.8	-129.3	-40.6	-163.2
2.2	63.3	100.9	49.8	129.5	-52.0	-134.6	-40.7	-169.6
2.3	63.8	101.9	49.9	132.4	-52.2	-139.9	-40.8	-176.0
2.4	64.1	102.8	50.0	135.0	-52.3	-145.2	-40.9	-181.3
2.5	64.6	103.8	50.2	137.3	-52.5	-150.5	-41.0	-187.6
2.6	64.8	104.6	50.4	139.2	-52.7	-155.3	-41.1	-192.9
2.7	65.0	105.4	50.5	140.8	-52.8	-160.1	-41.2	-198.2

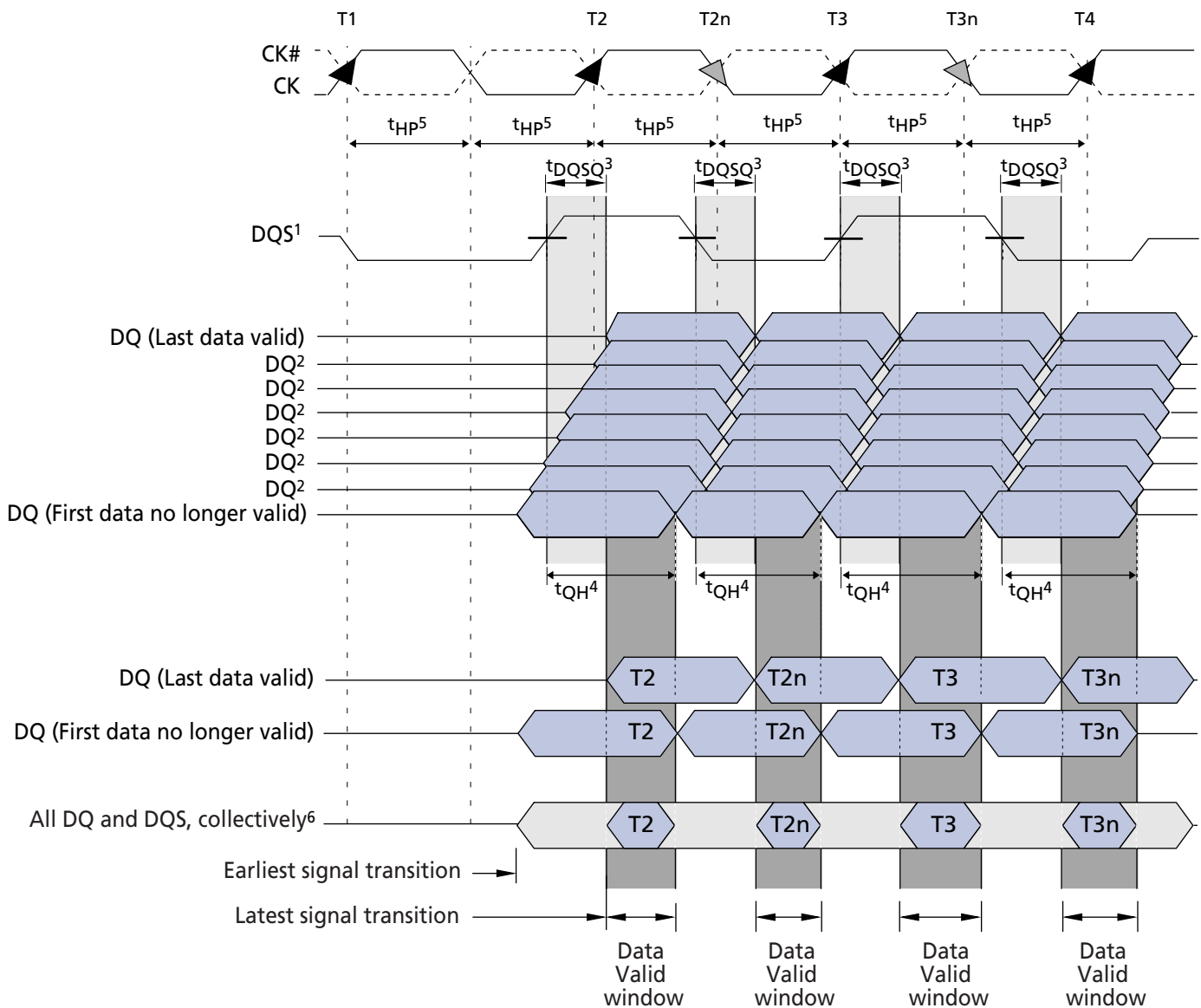
Note: The above characteristics are specified under best, worst, and nominal process variation/conditions.

**Table 33: Reduced Output Drive Characteristics**

Voltage (V)	Pull-Down Current (mA)				Pull-Up Current (mA)			
	Nominal Low	Nominal High	Minimum	Maximum	Nominal Low	Nominal High	Minimum	Maximum
0.1	3.4	3.8	2.6	5.0	-3.5	-4.3	-2.6	-5.0
0.2	6.9	7.6	5.2	9.9	-6.9	-7.8	-5.2	-9.9
0.3	10.3	11.4	7.8	14.6	-10.3	-12.0	-7.8	-14.6
0.4	13.6	15.1	10.4	19.2	-13.6	-15.7	-10.4	-19.2
0.5	16.9	18.7	13.0	23.6	-16.9	-19.3	-13.0	-23.6
0.6	19.9	22.1	15.7	28.0	-19.4	-22.9	-15.7	-28.0
0.7	22.3	25.0	18.2	32.2	-21.5	-26.5	-18.2	-32.2
0.8	24.7	28.2	20.8	35.8	-23.3	-30.1	-20.4	-35.8
0.9	26.9	31.3	22.4	39.5	-24.8	-33.6	-21.6	-39.5
1.0	29.0	34.1	24.1	43.2	-26.0	-37.1	-21.9	-43.2
1.1	30.6	36.9	25.4	46.7	-27.1	-40.3	-22.1	-46.7
1.2	31.8	39.5	26.2	50.0	-27.8	-43.1	-22.2	-50.0
1.3	32.8	42.0	26.6	53.1	-28.3	-45.8	-22.3	-53.1
1.4	33.5	44.4	26.8	56.1	-28.6	-48.4	-22.4	-56.1
1.5	34.0	46.6	27.0	58.7	-28.7	-50.7	-22.6	-58.7
1.6	34.3	48.6	27.2	61.4	-28.9	-52.9	-22.7	-61.4
1.7	34.5	50.5	27.4	63.5	-28.9	-55.0	-22.7	-63.5
1.8	34.8	52.2	27.7	65.6	-29.0	-56.8	-22.8	-65.6
1.9	35.1	53.9	27.8	67.7	-29.2	-58.7	-22.9	-67.7
2.0	35.4	55.0	28.0	69.8	-29.2	-60.0	-22.9	-69.8
2.1	35.6	56.1	28.1	71.6	-29.3	-61.2	-23.0	-71.6
2.2	35.8	57.1	28.2	73.3	-29.5	-62.4	-23.0	-73.3
2.3	36.1	57.7	28.3	74.9	-29.5	-63.1	-23.1	-74.9
2.4	36.3	58.2	28.3	76.4	-29.6	-63.8	-23.2	-76.4
2.5	36.5	58.7	28.4	77.7	-29.7	-64.4	-23.2	-77.7
2.6	36.7	59.2	28.5	78.8	-29.8	-65.1	-23.3	-78.8
2.7	36.8	59.6	28.6	79.7	-29.9	-65.8	-23.3	-79.7

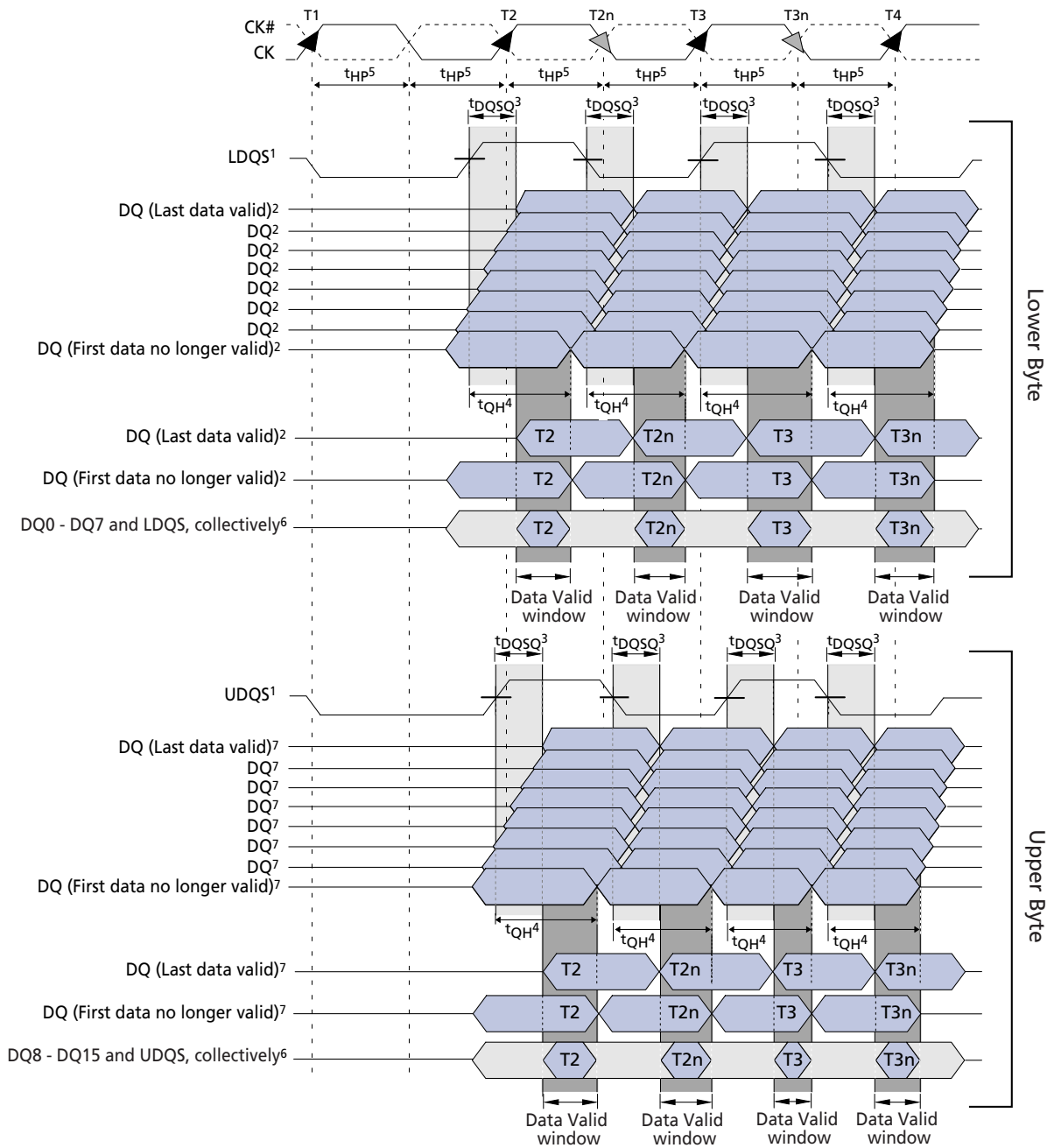
Note: The above characteristics are specified under best, worst, and nominal process variation/conditions.

**Figure 40: x4, x8 Data Output Timing –  $t_{DQSQ}$ ,  $t_{QH}$ , and Data Valid Window**



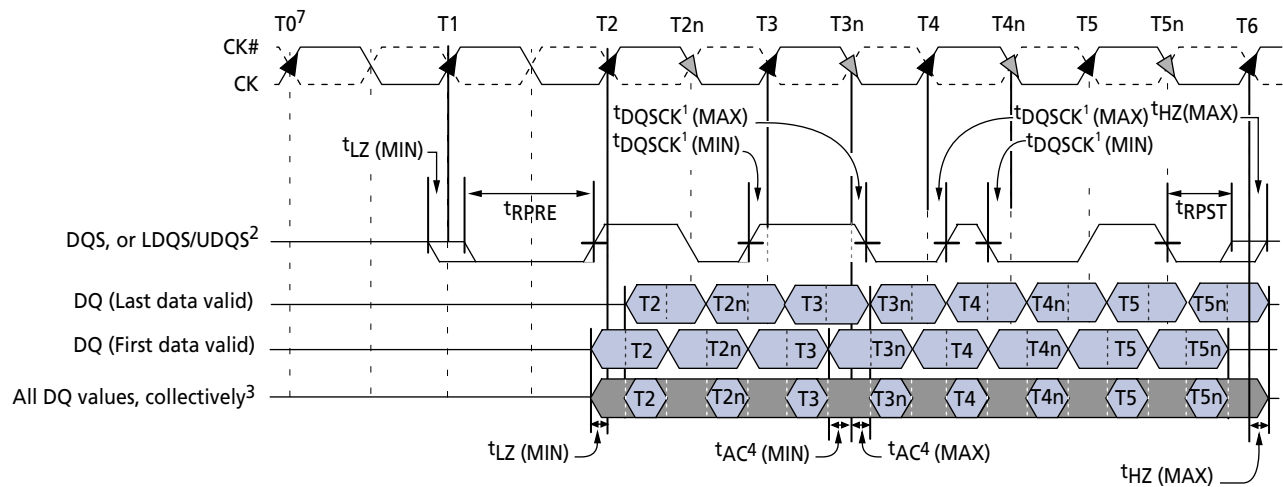
- Notes:
1. DQ transitioning after DQS transition define  $t_{DQSQ}$  window. DQS transitions at T2 and at T2n are an "early DQS," at T3 is a "nominal DQS," and at T3n is a "late DQS."
  2. For a x4, only two DQ apply.
  3.  $t_{DQSQ}$  is derived at each DQS clock edge and is not cumulative over time and begins with DQS transition and ends with the last valid DQ transition.
  4.  $t_{QH}$  is derived from  $t_{HP}$ :  $t_{QH} = t_{HP} - t_{QHS}$ .
  5.  $t_{HP}$  is the lesser of  $t_{CL}$  or  $t_{CH}$  clock transition collectively when a bank is active.
  6. The data valid window is derived for each DQS transitions and is defined as  $t_{QH}$  minus  $t_{DQSQ}$ .

**Figure 41: x16 Data Output Timing –  $t_{DQSQ}$ ,  $t_{QH}$ , and Data Valid Window**



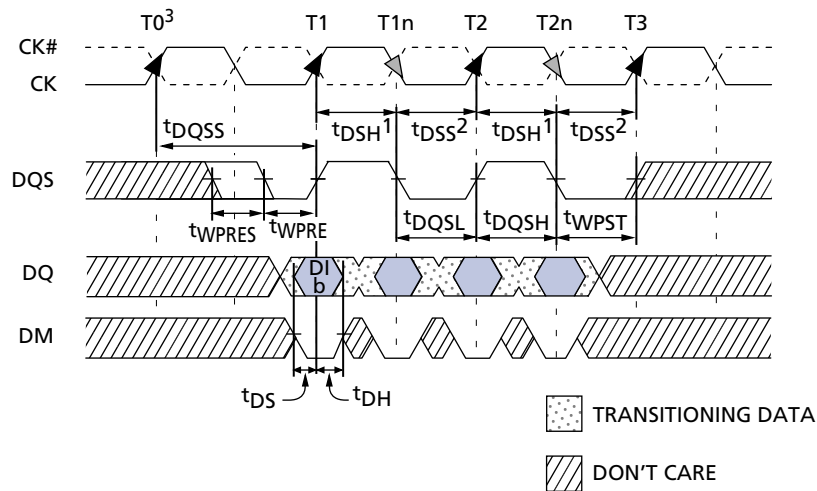
- Notes:
1. DQ transitioning after DQS transition define  $t_{DQSQ}$  window. LDQS defines the lower byte and UDQS defines the upper byte.
  2. DQ0, DQ1, DQ2, DQ3, DQ4, DQ5, DQ6, or DQ7.
  3.  $t_{DQSQ}$  is derived at each DQS clock edge and is not cumulative over time and begins with DQS transition and ends with the last valid DQ transition.
  4.  $t_{QH}$  is derived from  $t_{HP}$ :  $t_{QH} = t_{HP} - t_{QHS}$ .
  5.  $t_{HP}$  is the lesser of  $t_{CL}$  or  $t_{CH}$  clock transition collectively when a bank is active.
  6. The data valid window is derived for each DQS transition and is  $t_{QH}$  minus  $t_{DQSQ}$ .
  7. DQ8, DQ9, DQ10, D11, DQ12, DQ13, DQ14, or DQ15.

**Figure 42: Data Output Timing –  $t_{AC}$  and  $t_{DQSK}$**



- Notes:
- $t_{DQSK}$  is the DQS output window relative to CK and is the “long term” component of DQS skew.
  - DQ transitioning after DQS transition define  $t_{DQSQ}$  window.
  - All DQ must transition by  $t_{DQSQ}$  after DQS transitions, regardless of  $t_{AC}$ .
  - $t_{AC}$  is the DQ output window relative to CK, and is the “long term” component of DQ skew.
  - $t_{LZ}(\text{MIN})$  and  $t_{AC}(\text{MIN})$  are the first valid signal transition.
  - $t_{HZ}(\text{MAX})$ , and  $t_{AC}(\text{MAX})$  are the latest valid signal transition.
  - READ command with CL = 2 issued at T0.

**Figure 43: Data Input Timing**



- Notes:
- $t_{DSH}$  (MIN) generally occurs during  $t_{DQSS}$  (MIN).
  - $t_{DSS}$  (MIN) generally occurs during  $t_{DQSS}$  (MAX).
  - WRITE command issued at T0.
  - For x16, LDQS controls the lower byte and UDQS controls the upper byte.

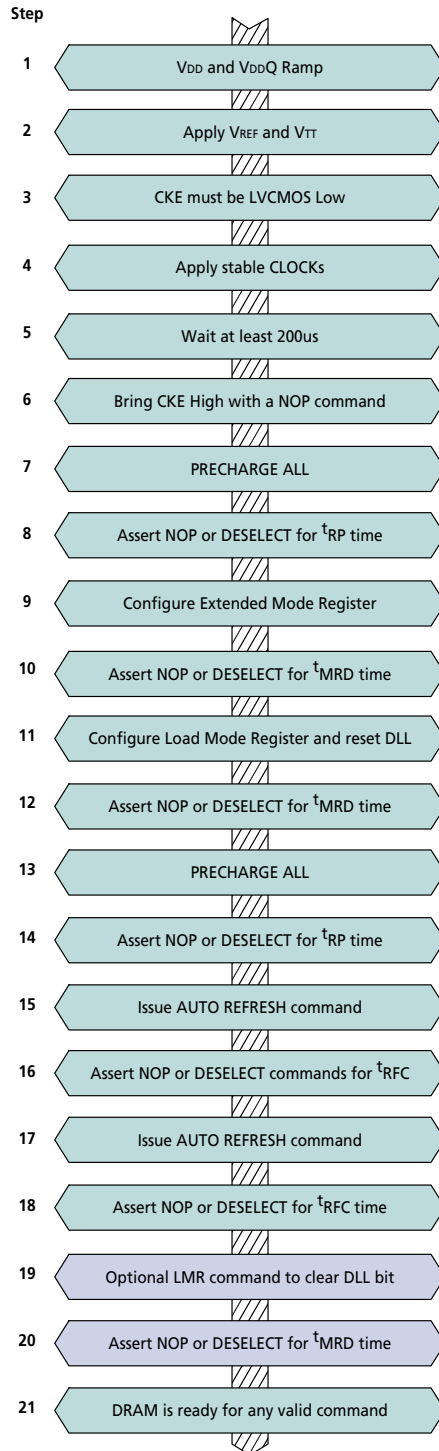


## Initialization

To ensure device operation the DRAM must be initialized as described below:

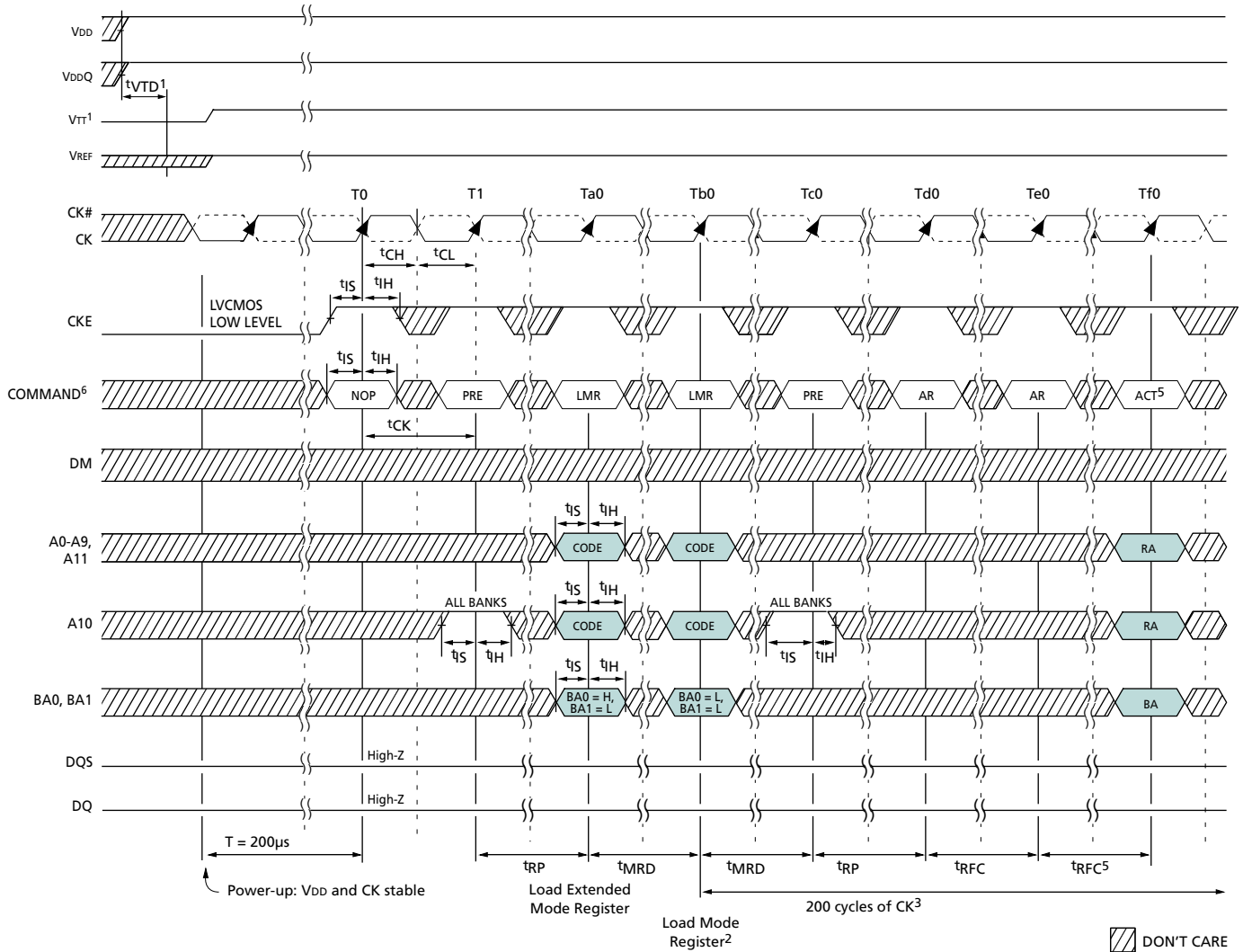
1. Simultaneously apply power to VDD and VDDQ.
2. Apply VREF and then VTT power.
3. Assert and hold CKE at a LVCMOS logic low.
4. Provide stable CLOCK signals.
5. Wait at least 200 $\mu$ s.
6. Bring CKE high and provide at least one NOP or DESELECT command. At this point the CKE input changes from a LVCMOS input to a SSTL2 input only and will remain a SSTL\_2 input unless a power cycle occurs.
7. Perform a PRECHARGE ALL command.
8. Wait at least  $t_{RP}$  time, during this time NOPs or DESELECT commands must be given.
9. Using the LMR command program the Extended Mode Register (E0 = 0 to enable the DLL and E1 = 0 for normal drive or E1 = 1 for reduced drive, E2 through En must be set to 0; where n = most significant bit).
10. Wait at least  $t_{MRD}$  time, only NOPs or DESELECT commands are allowed.
11. Using the LMR command program the mode register to set operating parameters and to reset the DLL. Note at least 200 clock cycles are required between a DLL reset and any READ command.
12. Wait at least  $t_{MRD}$  time, only NOPs or DESELECT commands are allowed.
13. Issue a PRECHARGE ALL command.
14. Wait at least  $t_{RP}$  time, only NOPs or DESELECT commands are allowed.
15. Issue an AUTO REFRESH command (Note this may be moved prior to step 13).
16. Wait at least  $t_{RFC}$  time, only NOPs or DESELECT commands are allowed.
17. Issue an AUTO REFRESH command (Note this may be moved prior to step 13).
18. Wait at least  $t_{RFC}$  time, only NOPs or DESELECT commands are allowed.
19. Although not required by the Micron device, JEDEC requires a LMR command to clear the DLL bit (set M8 = 0). If a LMR command is issued the same operating parameters should be utilized as in step 11.
20. Wait at least  $t_{MRD}$  time, only NOPs or DESELECT commands are allowed.
21. At this point the DRAM is ready for any valid command. Note 200 clock cycles are required between step 11 (DLL Reset) and any READ command.

**Figure 44: Initialization Flow Diagram**



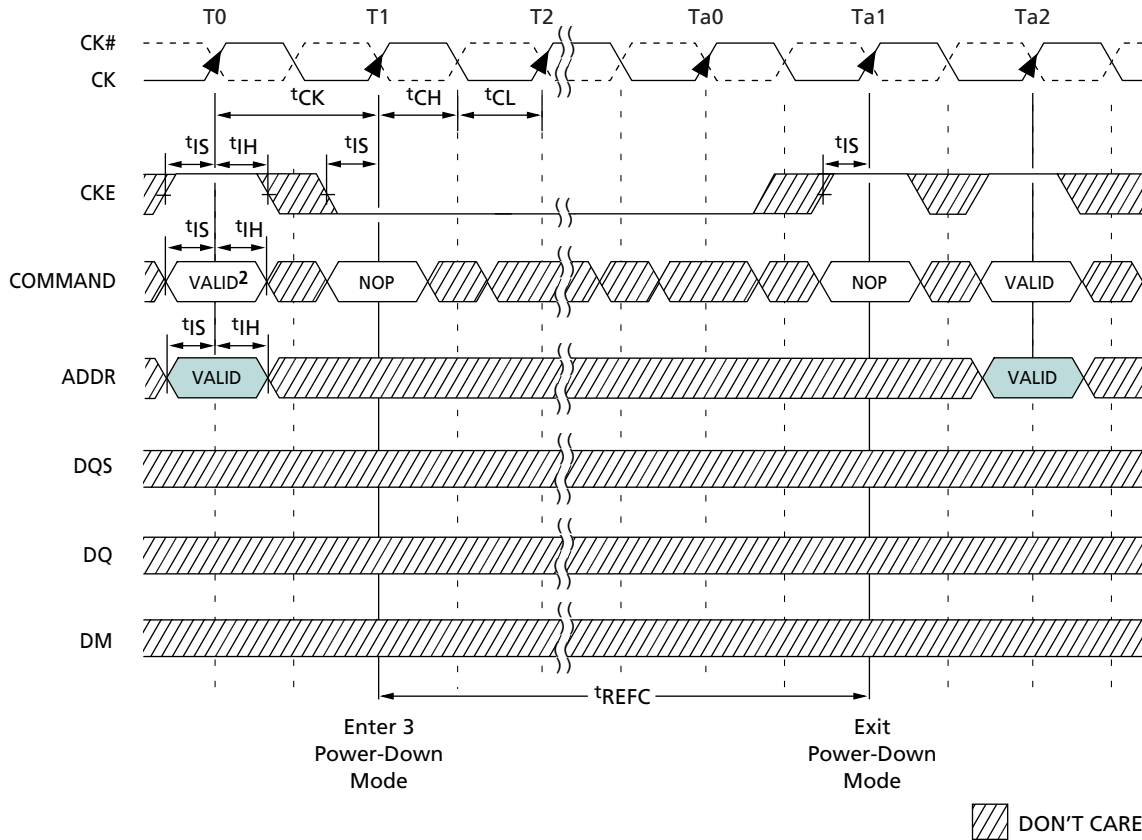
## Timing Diagrams

Figure 45: Initialize and Load Mode Registers



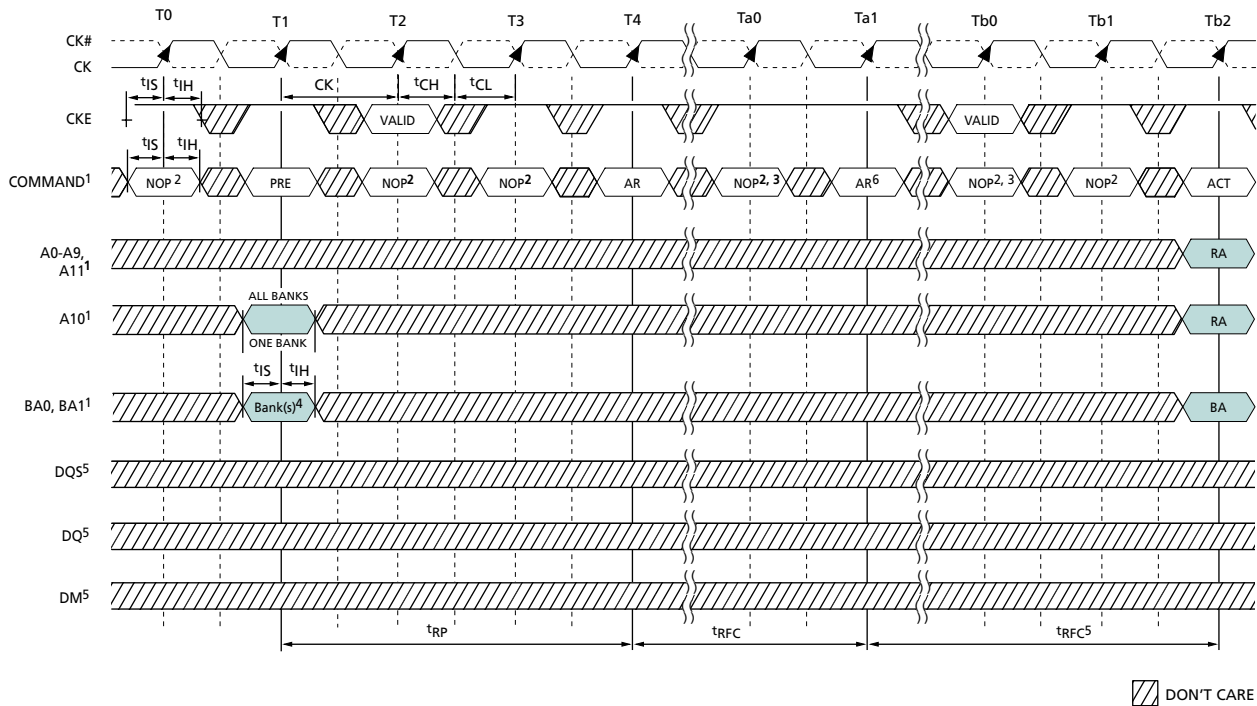
- Notes:
1. VTT is not applied directly to the device; however,  $t_{VTD}$  should be greater than or equal to zero to avoid device latch-up. VDDQ, VTT, and VREF, must be equal to or less than  $V_{DD} + 0.3V$ . Alternatively, VTT may be 1.35V maximum during power up, even if VDD/VDDQ are 0V, provided a minimum of 42 ohms of series resistance is used between the VTT supply and the input pin. Once initialized, including during self refresh mode, VREF must always be powered within specified range.
  2. Reset the DLL with A8 = H while programming the operating parameters.
  3.  $t_{MRD}$  is required before any command can be applied, and 200 cycles of CK are required before a READ command can be issued.
  4. The two AUTO REFRESH commands at Td0 and Te0 may be applied following the LOAD MODE REGISTER (LMR) command at Ta0.
  5. Although not required by the Micron device, JEDEC specifies issuing another LMR command (A8 = L) prior to activating any bank. If another command is issued, the same operating parameters previously issued must be used.
  6. PRE = PRECHARGE command, LMR = LOAD MODE REGISTER command, AR = AUTO REFRESH command, ACT = ACTIVE command, RA = Row Address, BA = Bank Address.

Figure 46: Power-Down Mode

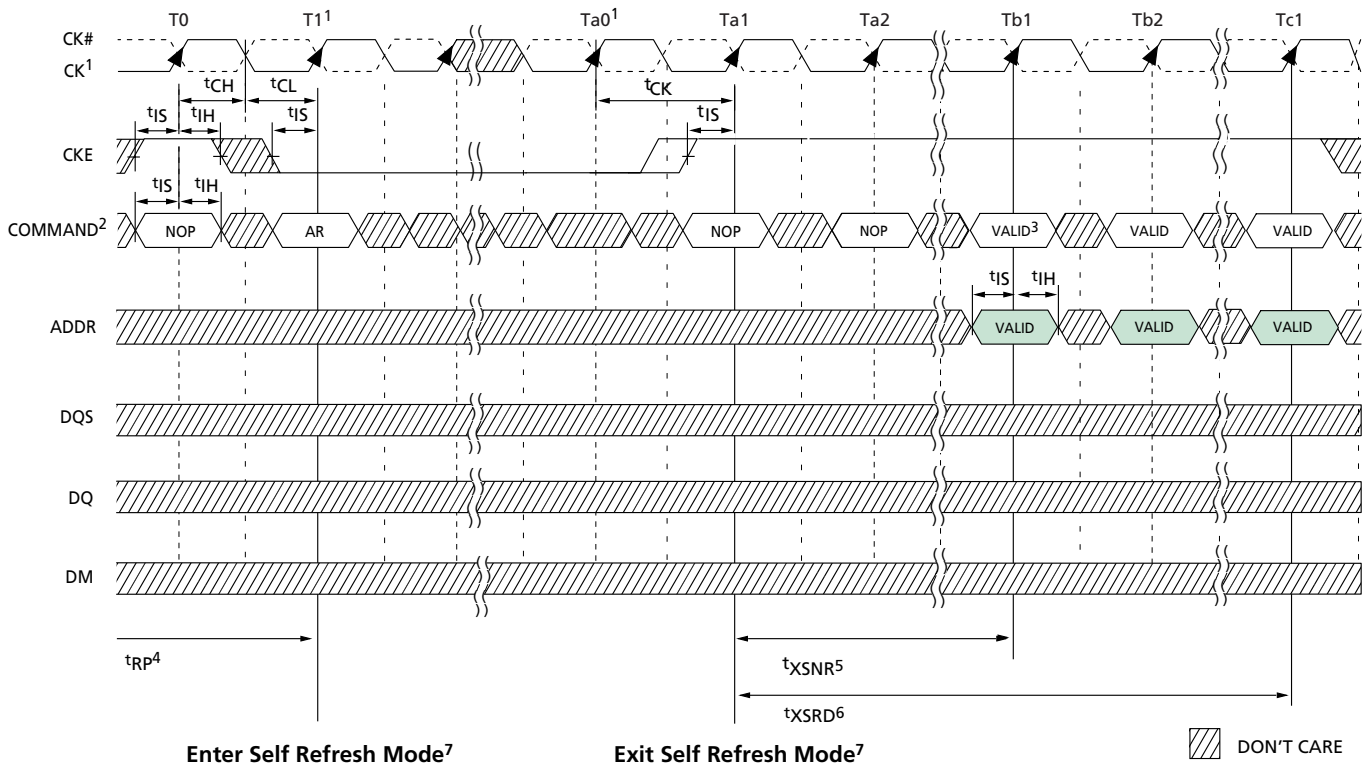


- Notes:
1. Once initialized, including during self refresh mode,  $V_{REF}$  must always be powered within specified range.
  2. If this command is a PRECHARGE (or if the device is already in the idle state), then the power-down mode shown is precharge power-down. If this command is an ACTIVE (or if at least one row is already active), then the power-down mode shown is active power-down.
  3. No column accesses are allowed to be in progress at the time power-down is entered.

Figure 47: Auto Refresh Mode



- Notes:
1. PRE = PRECHARGE, ACT = ACTIVE, AR = AUTO REFRESH, RA = Row Address, BA = Bank Address.
  2. NOP commands are shown for ease of illustration; other valid commands may be possible at these times. CKE must be active during clock positive transitions.
  3. NOP or COMMAND INHIBIT are the only commands allowed until after t<sub>RFC</sub> time, CKE must be active during clock positive transitions.
  4. "Don't Care" if A10 is HIGH at this point; A10 must be HIGH if more than one bank is active (i.e., must precharge all active banks).
  5. DM, DQ, and DQS signals are all "Don't Care"/High-Z for operations shown.
  6. The second AUTO REFRESH is not required and is only shown as an example of two back-to-back AUTO REFRESH commands.

**Figure 48: Self Refresh Mode**

**Enter Self Refresh Mode<sup>7</sup>**
**Exit Self Refresh Mode<sup>7</sup>**

DON'T CARE

Notes: 1. Clock must be stable until after the self refresh command has been registered. A change in clock frequency is allowed before  $Ta_0$ , provided it is within the specified  $t_{CK}$  limits. Regardless, the clock must be stable before exiting self refresh mode. That is, the clock must be cycling within specifications by  $Ta_0$ .

2. NOPs are interchangeable with DESELECT commands, AR = AUTO REFRESH command.

3. Auto Refresh is not required at this point, but is highly recommended.

4. Device must be in the all banks idle state prior to entering self refresh mode.

5.  $t_{XSNR}$  is required before any non-READ command can be applied. That is only NOP or DESELECT commands are allowed until  $Tb_1$ .

6.  $t_{XSRD}$  (200 cycles of a valid CK and CKE = high) is required before any READ command can be applied.

7. As a general rule, any time Self Refresh Mode is exited, the DRAM may not re-enter the Self Refresh Mode until all rows have been refreshed via the Auto Refresh command at the distributed refresh rate,  $t_{REFI}$ , or faster. However, the following exception is allowed. Self Refresh Mode may be re-entered anytime after exiting, if the following conditions are all met:

a. The DRAM had been in the Self Refresh Mode for a minimum of 200ms prior to exiting.

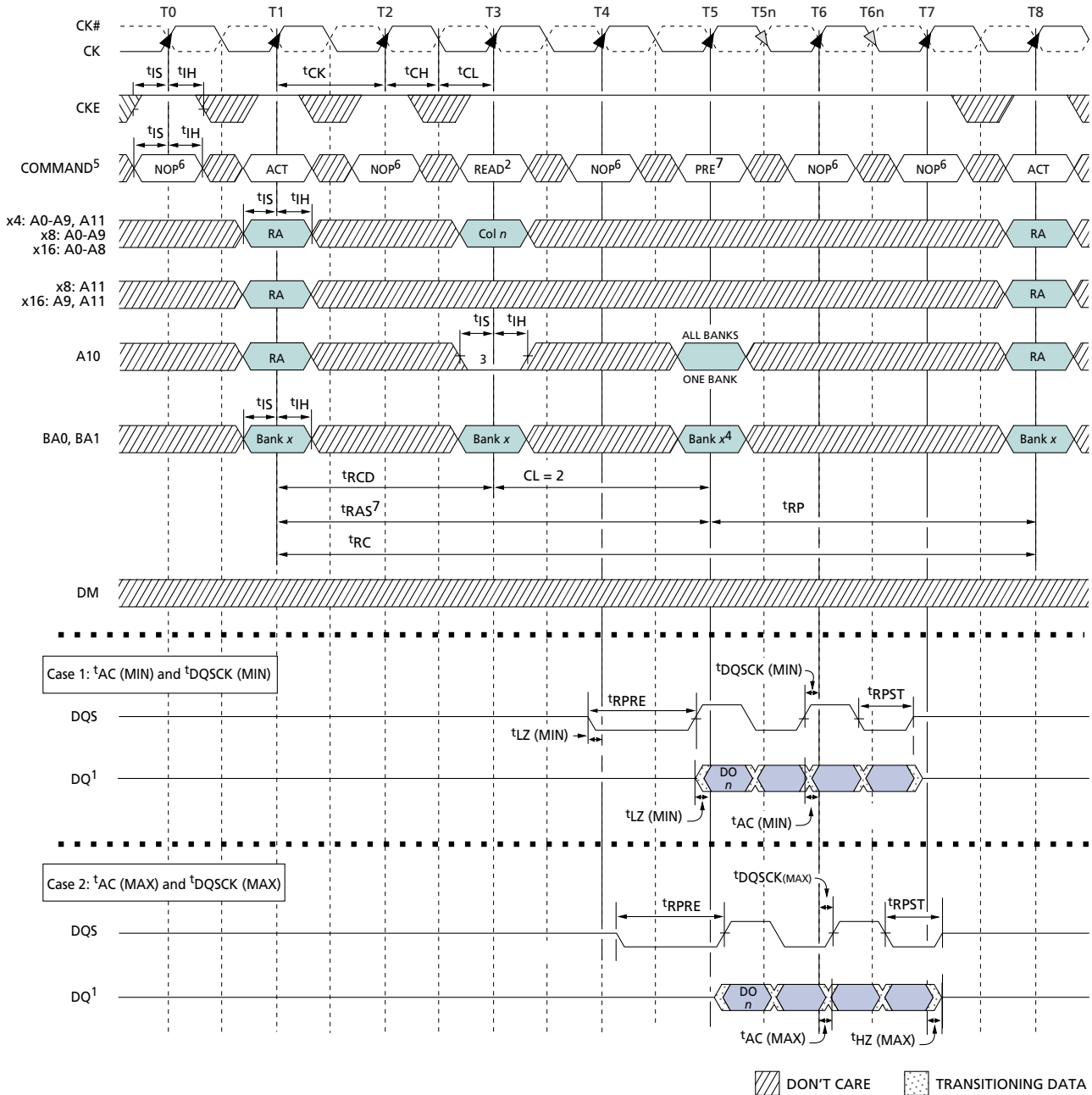
b.  $t_{XSNR}$  and  $t_{XSRD}$  are not violated.

c. At least two Auto Refresh commands are performed during each  $t_{REFI}$  interval while the DRAM remains out of Self Refresh mode.

8. If the clock frequency is changed during self refresh mode, a DLL reset is required upon exit.

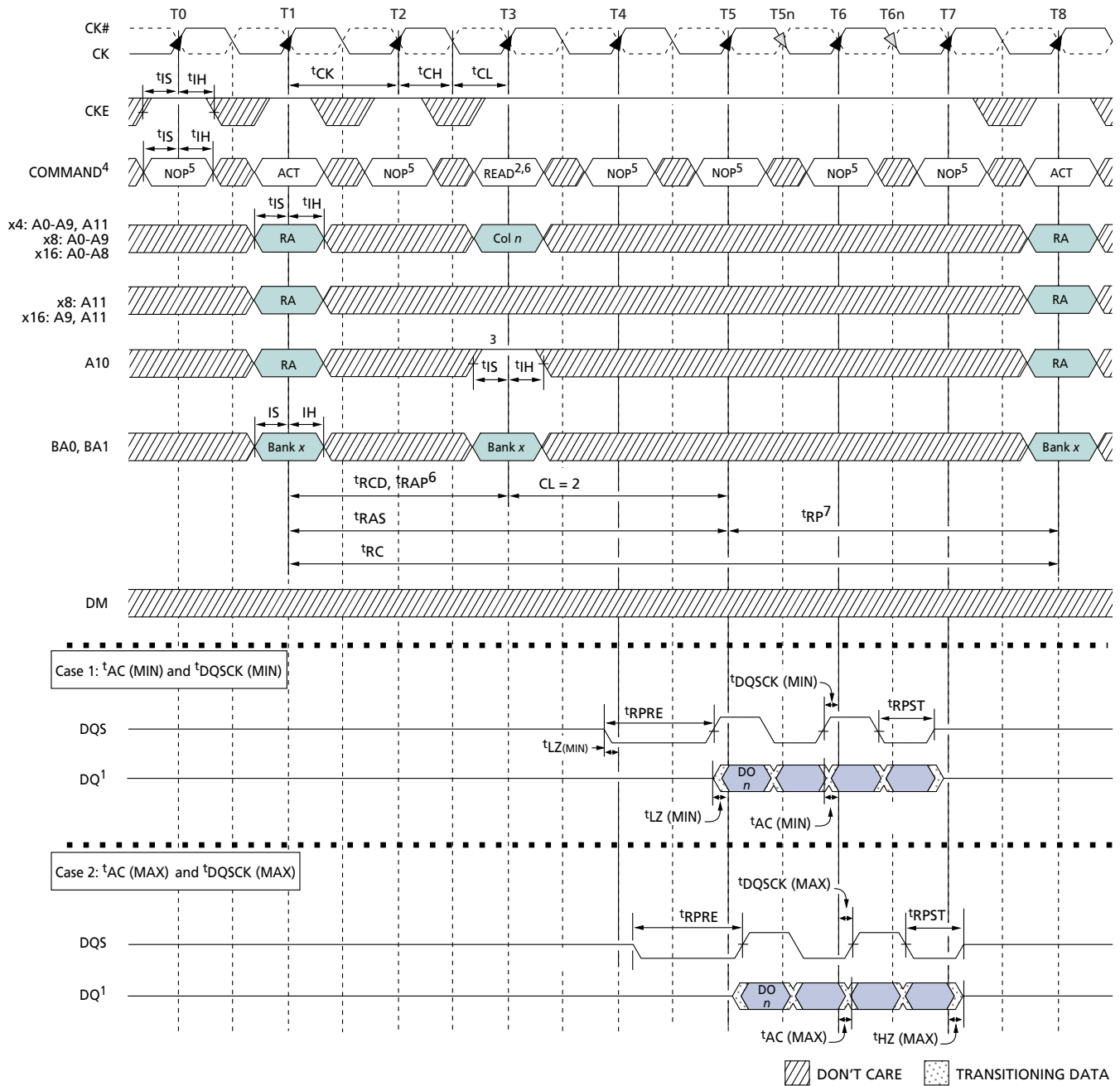
9. Once initialized, including during self refresh mode,  $V_{REF}$  must always be powered within specified range.

Figure 49: Bank Read - Without Auto Precharge



- Notes:
1.  $DO_n$  = data-out from column  $n$ ; subsequent elements are provided in the programmed order.
  2. Burst length = 4 in the case shown.
  3. Disable auto precharge.
  4. "Don't Care" if A10 is HIGH at T5.
  5. PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address.
  6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
  7. The PRECHARGE command can only be applied at T5 if  $t_{RAS}$  minimum is met.
  8. Refer to Figure 40 on page 77, Figure 41 on page 78, and Figure 42 on page 79 for detailed DQS and DQ timing.

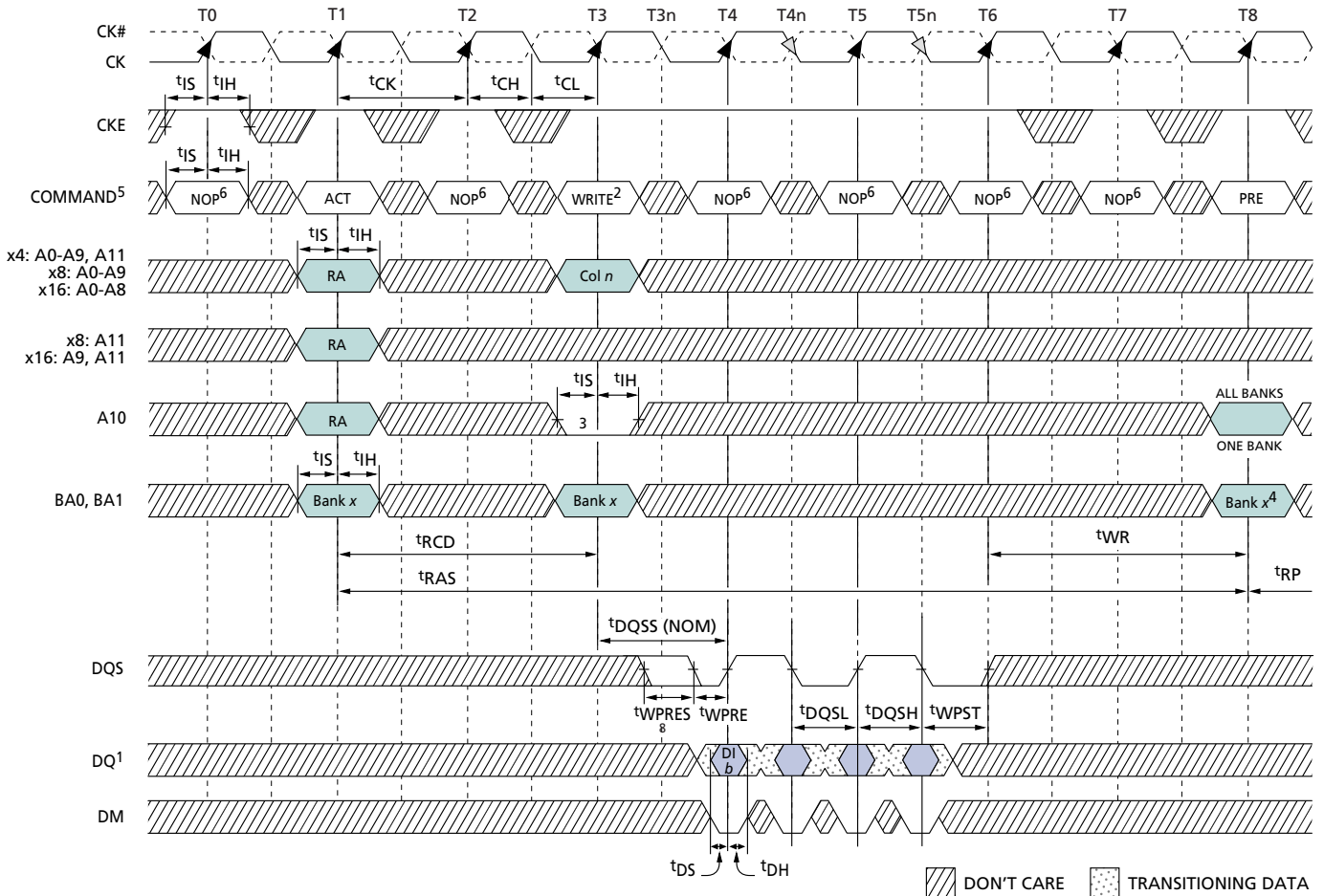
Figure 50: Bank Read - With Auto Precharge



- Notes:
1.  $DO_n$  = data-out from column  $n$ ; subsequent elements are provided in the programmed order.
  2. Burst length = 4 in the case shown.
  3. Enable auto precharge.
  4. ACT = ACTIVE, RA = Row Address, BA = Bank Address.
  5. NOP commands are shown for ease of illustration; other commands may be valid at these times.
  6. The READ command can only be applied at T3 if  $t_{RAP}$  is satisfied at T3.
  7.  $t_{RP}$  starts only after  $t_{RAS}$  has been satisfied.
  8. Refer to Figure 40 on page 77, Figure 41 on page 78, and Figure 42 on page 79 for detailed DQS and DQ timing.

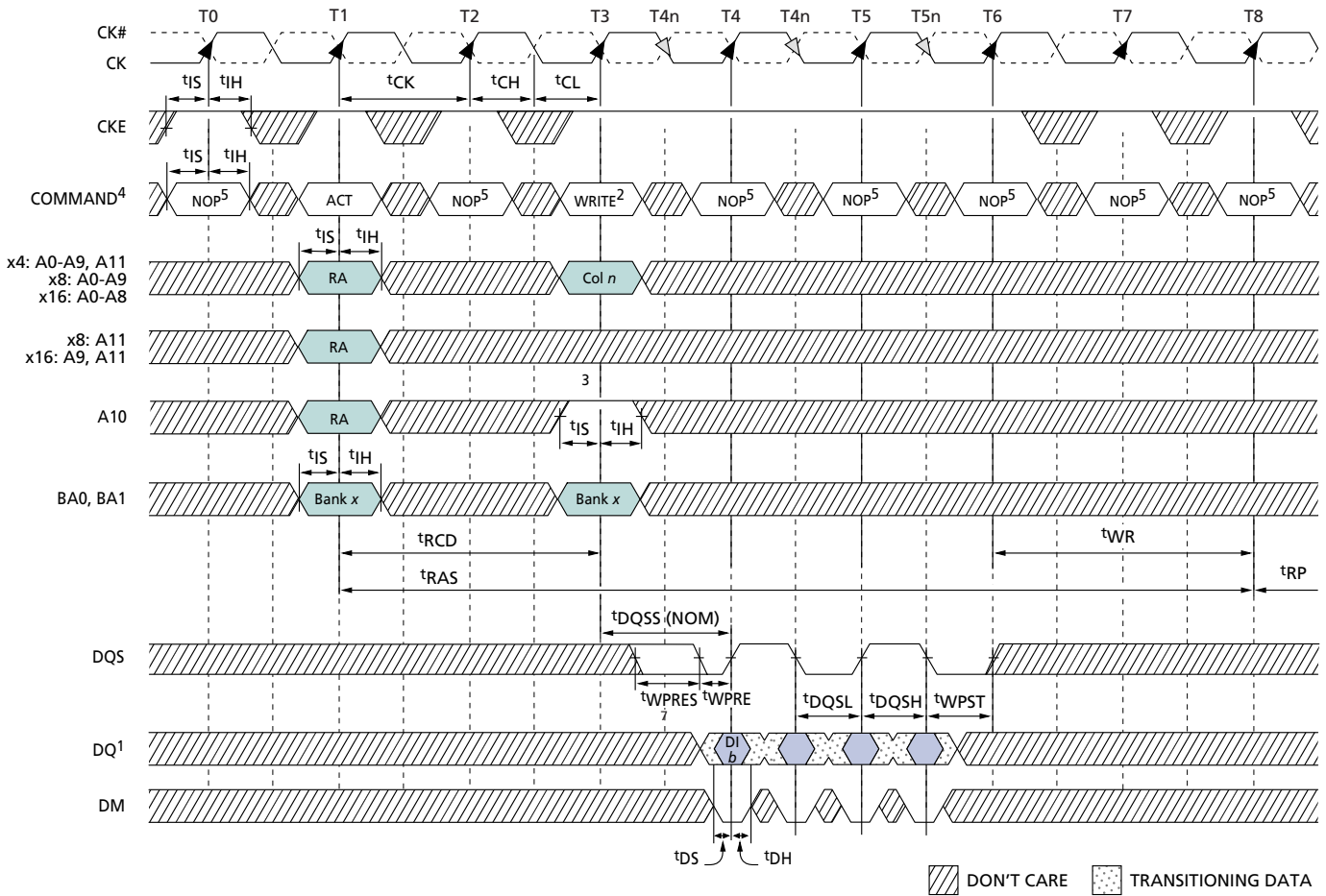


Figure 51: Bank Write - Without Auto Precharge



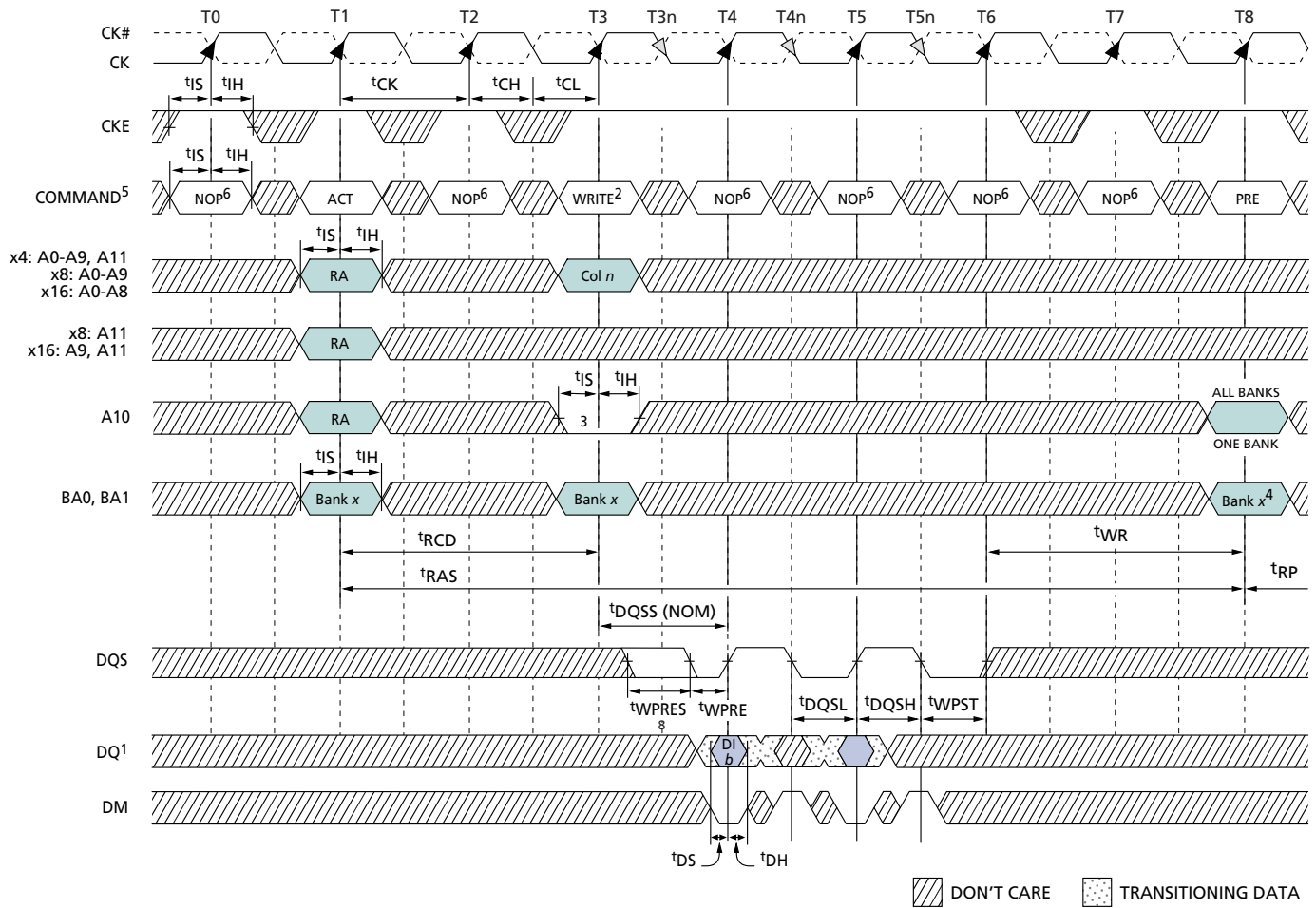
- Notes:
1.  $DIn$  = data-in. from column  $n$ ; subsequent elements are provided in the programmed order.
  2. Burst length = 4 in the case shown.
  3. Disable auto precharge.
  4. "Don't Care" if A10 is HIGH at T8.
  5. PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address.
  6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
  7. See Figure 45, Initialize and Load Mode Registers, on page 83 for detailed DQ timing.
  8. Although not required by the Micron device, JEDEC specifies that DQS be a valid HIGH, LOW or some point on a valid transition on or before this clock edge (T3n).

Figure 52: Bank Write - With Auto Precharge



- Notes:
1.  $DIn$  = data-out from column  $n$ ; subsequent elements are provided in the programmed order.
  2. Burst length = 4 in the case shown.
  3. Enable auto precharge.
  4. ACT = ACTIVE, RA = Row Address, BA = Bank Address.
  5. NOP commands are shown for ease of illustration; other commands may be valid at these times.
  6. See Figure 45, Initialize and Load Mode Registers, on page 83 for detailed DQ timing.
  7. Although not required by the Micron device, JEDEC specifies that DQS be a valid HIGH, LOW or some point on a valid transition on or before this clock edge (T3n).

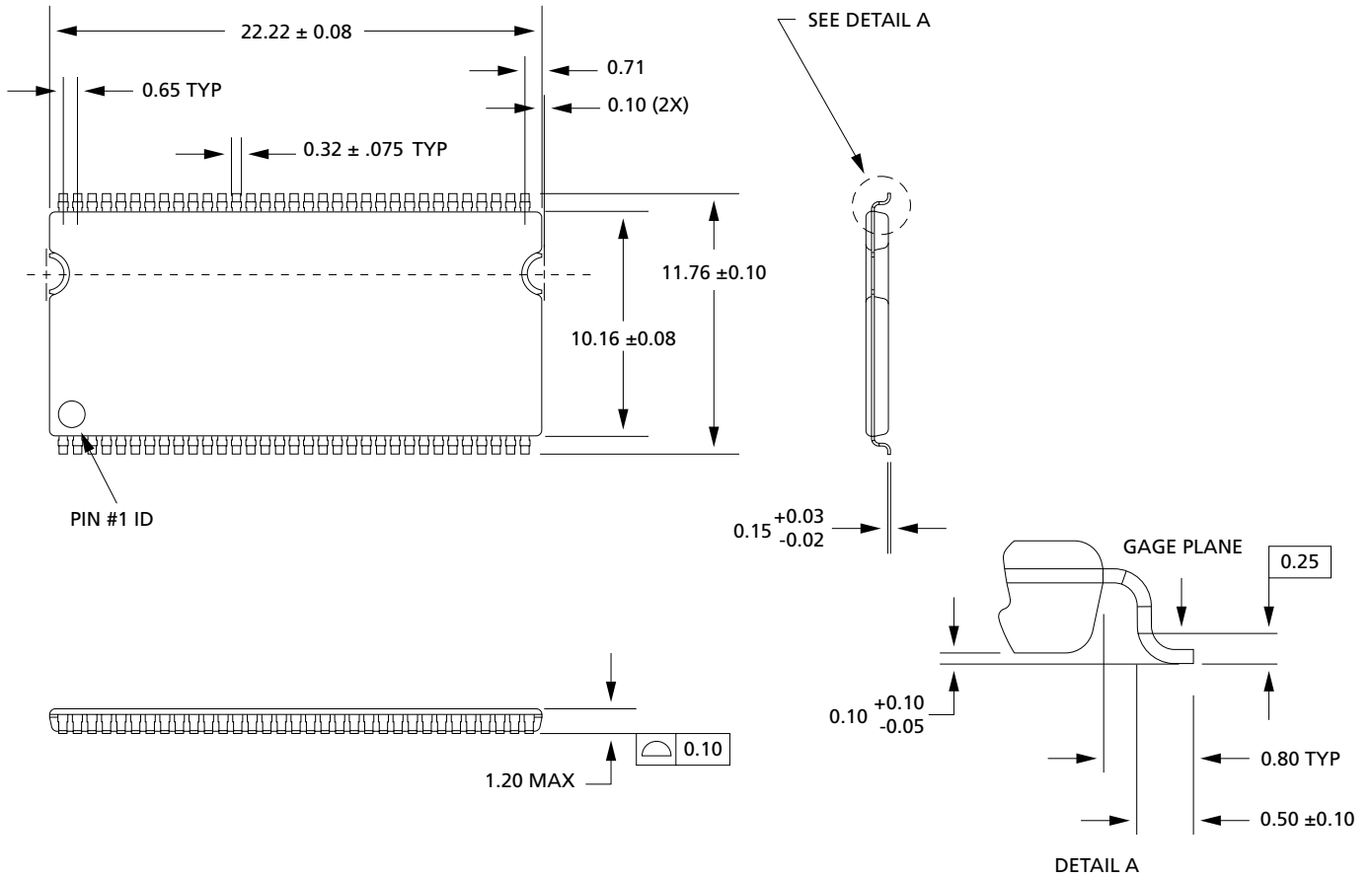
Figure 53: Write - DM Operation



- Notes:
1.  $DI_n$  = data-in from column  $n$ ; subsequent elements are provided in the programmed order.
  2. Burst length = 4 in the case shown.
  3. Disable auto precharge.
  4. "Don't Care" if A10 is HIGH at T8.
  5. PRE = PRECHARGE, ACT = ACTIVE, RA = Row Address, BA = Bank Address.
  6. NOP commands are shown for ease of illustration; other commands may be valid at these times.
  7. See Figure 45, Initialize and Load Mode Registers, on page 83 for detailed DQ timing.
  8. Although not required by the Micron device, JEDEC specifies that DQS be a valid HIGH, LOW or some point on a valid transition on or before this clock edge (T3n).

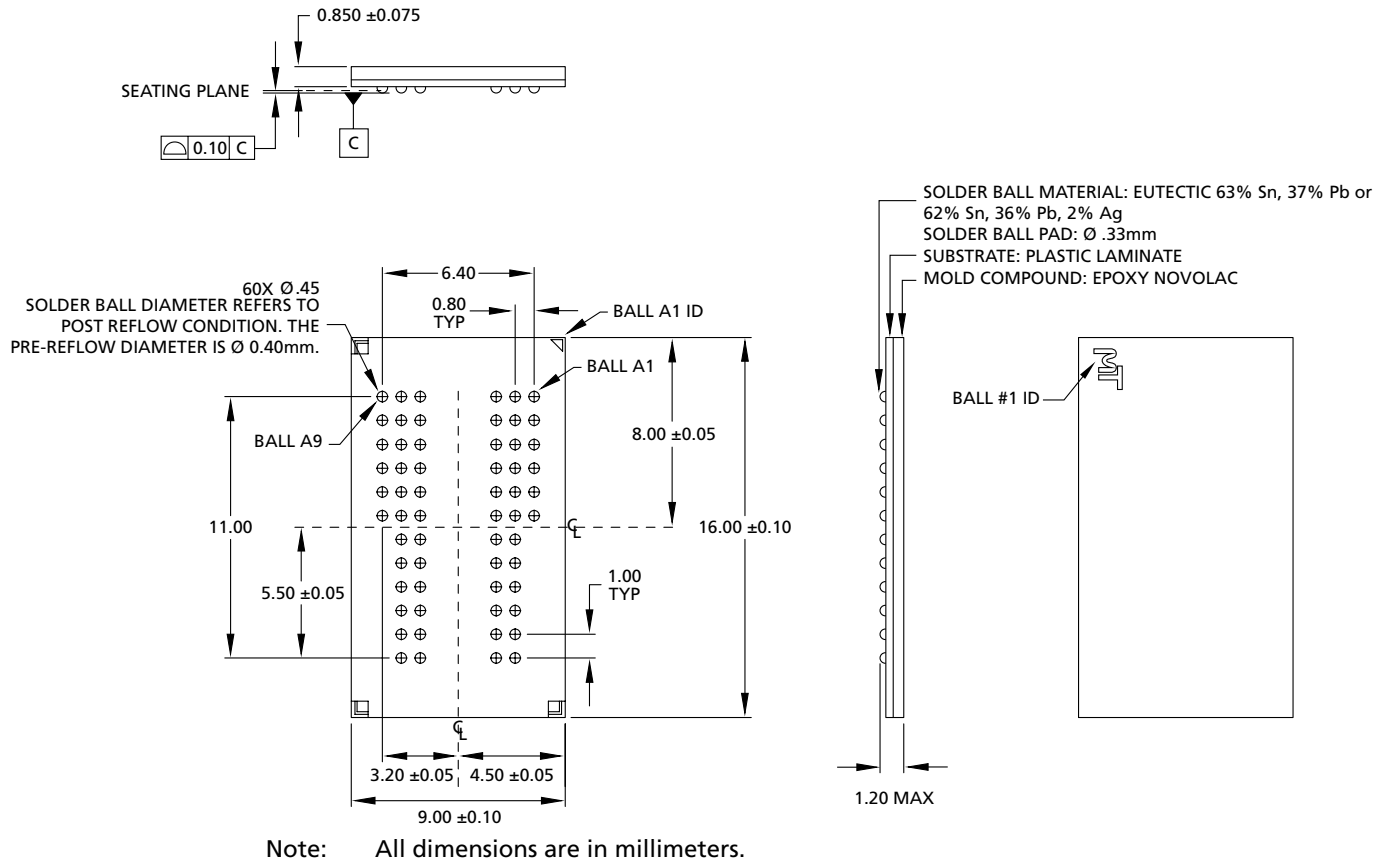
### Package Dimensions

Figure 54: 66-Pin Plastic TSOP (400 mil)



- Notes: 1. All dimensions are in millimeters.  
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

**Figure 55: 60-Ball FBGA (16 x 9mm)**



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**This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.**