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DS2502-E64
IEEE EUI-64 Node Address Chip
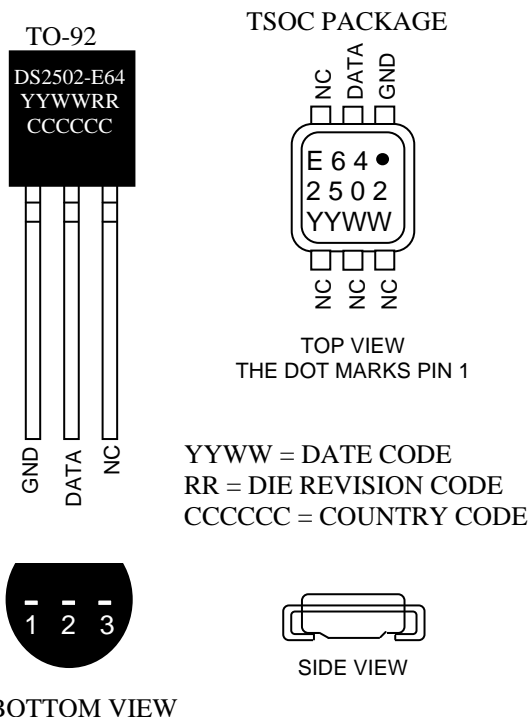
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FEATURES

- IEEE-approved factory programmed 64-bit node address chip (EUI-64) with 768 bits user-programmable OTP-EPROM communicates with the economy of one signal plus ground
- Meets the node identification requirements of IEEE Standard 1394-1995 (FireWire™)
- Unique, factory-lasered and tested 64-bit registration number assures absolute traceability because no two parts are alike
- Built-in multidrop controller ensures compatibility with other 1-Wire products
- Device is an "add only" memory where additional data can be programmed into EPROM without disturbing existing data
- Reduces control, address, data, power and programming signals to a single pin
- Directly connects to a single port pin of a microprocessor and communicates at up to 16.3k bits per second
- Presence detector acknowledges when reader first applies voltage
- Low cost TO-92 or TSOC surface mount packages
- Reads over a wide voltage range of 2.8V to 6.0V from -40°C to +85°C; programs at 11.5V to 12.0V from -40°C to +50°C

PIN ASSIGNMENT

TO-92

DS2502-E64
YYWWRR
CCCCCC

GND DATA NC

TSOC PACKAGE

NC DATA GND

E 6 4 ●
2 5 0 2
YYWW

NC NC NC

TOP VIEW
THE DOT MARKS PIN 1

YYWW = DATE CODE
RR = DIE REVISION CODE
CCCCCC = COUNTRY CODE

1 2 3
BOTTOM VIEW

SIDE VIEW

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS2502-E64+	-40°C to +85°C	3 TO-92
DS2502P-E64+	-40°C to +85°C	6 TSOC

+ Denotes a lead(Pb)-free/RoHS-compliant package.

FireWire™ is a trademark of Apple Computer, Inc.

DESCRIPTION

The DS2502-E64 is a variant of the DS2502 1024-bit Add-Only Memory. It differs from the standard DS2502 in its custom ROM family code 89h, and the UniqueWare Identifier 5E7h in place of the upper 12 bits of the standard ROM serialization field. Otherwise, the electrical and logical behavior is identical to that of the DS2502. For technical details please refer to the DS2502 data sheet.

The first 32 bytes of the DS2502-E64's EPROM memory contain a globally unique 64-bit node address (EUI-64) and are write-protected. The data structure follows the conventions of UniqueWare devices using Default Data Structure (Figure 1). This format is also known as UDP (universal data packet) and is commonly used in 1-Wire APIs. Therefore, if using one of those APIs one can call a high level function to read and verify the inverted CRC16. The UDP is defined in Application Note 114, *1-Wire File Structure*, and the APIs can be found in the *1-Wire Software Development Kits*.

Figure 1. EUI-64 NODE ADDRESS CHIP DATA STRUCTURE

(UNUSED)	$\overline{CRC16}$		COMPANY ID VALUE		EXTENSION ID VALUE		PROJECT ID		LENGTH
	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	
17 BYTES FFh	2 BYTES		3 BYTES CONSTANT 006035h		5 BYTES SERIALIZATION		4 BYTES CONSTANT 00001128h		1 BYTE 0Ch

HIGH ADDRESS   LOW ADDRESS

The data record starts with a length byte (0Ch) and the 4-byte UniqueWare Project ID 00001128h. The next eight bytes contain the EUI-64 global identifier (node address) which consists of an incrementing 40-bit extension identifier and the IEEE-assigned 24-bit company ID value 006035h. An inverted 16-bit CRC ends the data record. The remaining bytes of the 32-byte memory page remain unprogrammed. Neither the 40–bit extension identifier nor the 24-bit company ID are related to the 64-bit ROM registration number. The ROM registration number is used to provide a unique address to access the DS2502-E64 when multidropped on a 1-Wire bus.

EXAMPLE

Assume that a manufacturer's company ID value is 006035h and the 40-bit extension identifier is 234567ABCDh. The EUI-64 value generated from these two numbers is 006035234567ABCDh, whose byte and bit representations are illustrated in Figure 2.

Figure 2. SAMPLE EUI-64 VALUE

MOST SIGNIFICANTBYTE							LEAST SIGNIFICANTBYTE	
00	60	35	23	45	67	AB	CD	HEX
0000 0000	0110 0000	0011 0101	0010 0011	0100 0101	0110 0111	1010 1011	1100 1101	BINARY
MOST SIGNIFICANT BIT							LEAST SIGNIFICANT BIT	

This information is stored in the DS2502-E64 as 64-bit number with the least significant byte at the lower address. Including the length byte and the inverted CRC, the complete set of data is shown in Figure 3.

Figure 3. PHYSICAL ADDRESS AND DATA MAPPING INSIDE THE DEVICE

ADDRESS	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
DATA	3E	FF	00	60	35	23	45	67	AB	CD	00	00	11	28	0C

The four bytes at memory addresses 01h to 04h contain the UniqueWare Project ID 00001128h. The two bytes at addresses 0Dh and 0Eh are the inverted 16-bit CRC over the length byte, Project ID and EUI-64 value. The least significant byte of the CRC is stored at address 0Dh. This CRC is generated according to the standardized CRC16 polynomial function $X^{16} + X^{15} + X^2 + 1$. For more details on generating CRC values including examples in both hardware and software, see Application Note 27, *Understanding and Using Cyclic Redundancy Checks with Maxim iButton Products*.

The contents of the memory address range 0Fh to 1Fh is FFh. These cells cannot be altered since the whole memory page is write-protected. The memory range from 20h to 7Fh, however, is user-programmable. It can be write-protected by programming the corresponding write-protect bit in the status memory of the DS2502-E64.

REVISION HISTORY

REVISION DATE	DESCRIPTION	PAGES CHANGED
12/09	Changed the *Ordering Information* to lead free.	1
	Included an explanation of "Default Data Structure" above Figure 1.	2
	Emphasized that the 16-bit CRC is inverted.	2
	Inserted actual CRC value to Figure 3.	2
	Reformatted Figures 1 to 3.	2
	Removed reference to the Book of iButton Standards.	2
	Changed notation of hexadecimal numbers from $_{16}$ or H to h.	1, 2, 3