3 Volt Intel® Advanced+ Boot Block Flash Memory

28F800C3, 28F160C3, 28F320C3, 28F640C3

Specification Update

November 2002

Notice: The 28F800C3, 28F160C3, 28F320C3, 28F640C3 may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

Order Number: 297938-014

Contents

Revision History

Date	Version	Description
05/13/98	-001	Document includes all known specifications to date (original version).
06/02/98	-002	Changed Ordering Information for 32-Mbit densities to 95 ns and 115 ns available access speed only Added µBGA* package mark clarification Added test condition clarification for I_{PPD}
07/08/98	-003	Added specification change for µBGA* package pinout
08/12/98	-004	Added Errata for Maximum I_{CCD} Change
09/09/98	-005	Added Specification Change for Byte-Wide Protection Register Addressing
09/24/98	-006	Added CFI Primary-Vendor Specific Extended Query Change Added Block Locking Command Sequence Change V_{IH} Maximum Specification Change Removed 48-Lead TSOP Package Pinout Change (fixed in 290645-002) Removed Protection Register Addressing Change (fixed in 290645-002) Removed CFI Query Structure Output Table Change (fixed in 290645-002) Removed Ordering Information Change (fixed in 290645-002) Removed µBGA* Package Pinout Change (fixed in 290645-002) Removed Protection Register Addressing Clarification (fixed in 290645-002) Removed µBGA* Package Mark Clarification (fixed in 290645-002)
10/02/98	-007	Removed Byte-Wide Protection Register Addressing Change (fixed in 290645-003) Removed V_{IH} Maximum Change (fixed in 290645-003) Removed I_{PPD} Test Condition Clarification (fixed in 290645-003) Name changed from *3 Volt Advanced+ Boot Block Flash Memory Family*
05/04/99	-008	Added Specification Change #1, *Maximum I_{CCD} Change* Added Specification Change #2, *CFI Primary-Vendor Specific Extended Query Change* Added Specification Change #3, *Block Locking Command Sequence Change* Added Specification Change #4, *32-Mb Maximum V_{CC} Change* Updated CFI feature identification bit definition
10/05/00	-009	Renamed Specification Change #4, *32-Mb Maximum V_{CC} Change*, to *0.25µm 32-Mb Maximum V_{CC} Change*, and modified it to indicate that the affected product is the 32-Mb product on the 0.25µm process Revised Erratum #1, *Maximum I_{CCE} when V_{PP}=12 V*
05/03/01	-010	Added Erratum #2, *28F320C3xC Reset Failure*
07/23/01	-011	Updated Erratum #2, *28F320C3xC Reset Failure, added 3.3v Vcc max*
11/05/01	-012	Added Erratum #3, *28F640C3xC* for Maximum I_{CCD} / I_{CCS} Change
3/05/02	-013	Added Erratum #4, *28F160C3xC Erase Resume Issue*
11/21/02	-014	Added Erratum #5, *28F160C3xC and 28F640C3xC Lock/Unlock/Lock-Down Operation*

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
3 Volt Intel® Advanced+ Boot Block Flash Memory, 28F800C3, 28F160C3, 28F320C3, 28F640C3 (x16) Datasheet	290645-014

Nomenclature

Errata are design defects or errors. These may cause the behavior of the 28F800C3, 28F160C3, 28F320C3, 28F640C3 to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's life cycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications, and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 28F800C3, 28F160C3, 28F320C3, 28F640C3 product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	This erratum exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping, or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.

Row

	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

Number	Page	Status	Errata
1	10	Plan Fix	"28F320C3xC Maximum ICCE when Vpp=12V"
2	10	Plan Fix	"28F320C3xC Reset Failure"
3	11	Plan Fix	"28F640C3xC Maximum ICCS and ICCD Change"
4	12	Plan Fix	"28F160C3xC Erase Resume Issue"
5	14	Plan Fix	"28F160C3xC and 28F640C3xC Lock/Unlock/Lock-Down Operation"

Specification Changes

8 Mb and 16Mb - 28F160C3 and 28F800C3

Number	Page	Specification Changes
1	15	Maximum I_{CCD} Change
2	15	CFI Primary-Vendor Specific Extended Query Change
3	15	Block Locking Command Sequence Change

32Mb - 28F320C3

Number	Page	Specification Changes
1	15	Maximum I_{CCD} Change
2	15	CFI Primary-Vendor Specific Extended Query Change
3	15	Block Locking Command Sequence Change
4	16	0.25µm 32-Mb Maximum V_{CC} Change

Specification Clarifications

Number	Page	Specification Clarifications
N/A	17	None in this Specification Update revision

Documentation Changes

Number	Document Revision	Page	Documentation Changes
N/A		17	None in this Specification Update revision

Identification Information

Markings

The Finished Processing Order (FPO) number correlates to a specific device stepping as illustrated in the table below:

Stepping[1]	Identifier
A Stepping	Ninth digit on topside FPO mark (third line) = anything

Note: Device steppings are based on continuous improvements made in manufacturing and testing of the device and represent the current material shipped.

Errata

1. 28F320C3xC Maximum I_{CCE} when V_{pp}=12V

Problem: When V_{PP}=12V, I_{CCE} Max on 28F320C3xC devices on the 0.18µm deviates from the published specification and increases from 15mA to 25mA. The following is the revised specification for these products.

Sym	Parameter	V_{PP}	11.4 V –12.6 V		Unit	Test Conditions
		V_{CC}/ V_{CCQ}	2.7 V –3.6 V			
			Typ	Max		
I_{CCE}	V_{CC} Erase Current		8	25	mA	V_{PP} = V_{PP2} (12V), Erase in Progress

Implication: The increased current requirements may result in increased power drawn from the power supply during limited 12 V production programming. 3 V programming is unaffected.

Status: 32-Mb devices on the 0.18mm process are affected.

2. 28F320C3xC Reset Failure

Problem: The 0.18µm 28F320C3xC devices can unintentionally reset under certain conditions where V_{PP} toggles.

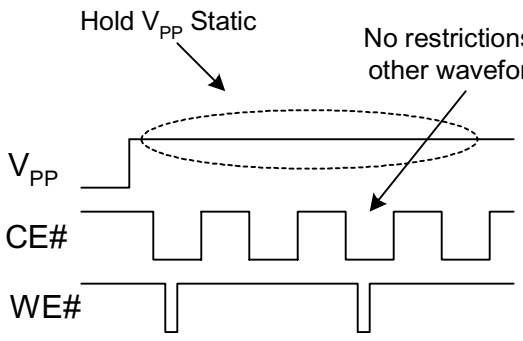
Implication: When the reset occurs, any command being executed is interrupted and the flash switches to read array mode.

Workaround: There are four workarounds for this erratum:

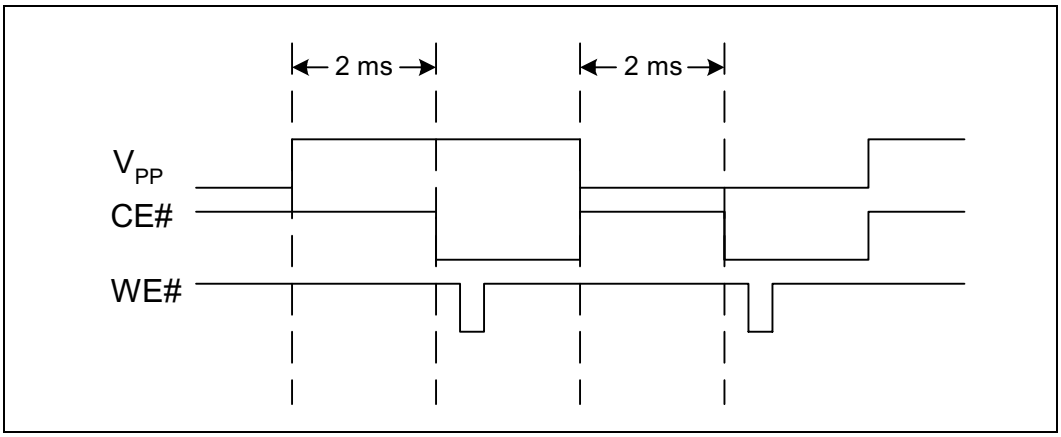
1) Tie V_{PP} to V_{CC};

2) If the third and forth digits on the top side FPO mark (third line) is equal or greater than “23”, then V_{CC} may be set from 2.7v to 3.3v. V_{CC} must not exceed 3.3v

3) Set V_{PP} to a static high or static low level as shown here; and



4) Wait 2 ms after a V_{PP} transition to access the flash device, as shown here.



Status: This erratum affects all 0.18µm 28F320C3 devices. Root cause has been identified and this erratum may be fixed in a future stepping of the product.

3. 28F640C3xC Maximum I_{CCS} and I_{CCD} Change

Problem: On the 0.18µm 28F640C3xC devices, the maximum $I_{CCS\ and}$ I_{CCD} deviates from the published specification and increases from 15 µA to 20 µA. The following table shows the revised I_{CCS} and I_{CCD} specifications.

Sym	Parameter	V_{CC}	2.7 V –3.6 V		Unit	Test Conditions
		V_{CCQ}	2.7 V –3.6 V			
		Note	Type	Max		
I_{CCS}	V_{CC} Standby Current	1,7	7	20	µA	$V_{CC} = V_{CC}Max$ CE# = RP# = V_{CCQ} or during Program/ Erase Suspend WP# = V_{CCQ} or GND
I_{CCD}	V_{CC} Deep Power-Down Current	1,7	7	20	µA	$V_{CC} = V_{CC}Max$ $V_{CCQ} = V_{CCQ}Max$ $V_{IN} = V_{CCQ}$ or GND RP# = GND ± 0.2 V

NOTE:
1. All currents are in RMS unless otherwise noted. Typical values at nominal V_{CC}, T_A = +25 °C.
2. The test conditions $V_{CC}Max$, $V_{CCQ}Max$, $V_{CC}Min$, and $V_{CCQ}Min$ refer to the maximum or minimum V_{CC} or V_{CCQ} voltage listed at the top of each column.

Implication: The increased current requirements may result in a nominal increase in power drawn from the power supply.

Workaround: None

Status: This erratum affects all 0.18µm 28F640C3xC devices. Root cause has been identified and this erratum may be fixed in a future stepping of the product.

4. 28F160C3xC Erase Resume Issue

Problem: On the 0.18µm 28F160C3xC devices, a design anomaly was discovered. During an Erase-Suspend operation, if the Program (40H/10H) sequence is executed, under limited conditions the proceeding Erase Resume command (D0H) may not actually resume the device. No customers have reported failures in product applications. Customers who use any version of FDI (Intel Flash Data Integrator) software will not see this issue. If the Read Array command is issued prior to the Erase Resume command, users will not see the issue (typical in XIP applications).

Implication: The Resume Command (D0H) may be ignored by the device and will not correctly resume. The device will appear to remain in suspend (via status register). After a reset of the flash device the status register will clear. This failure has been recreated in a lab environment only.

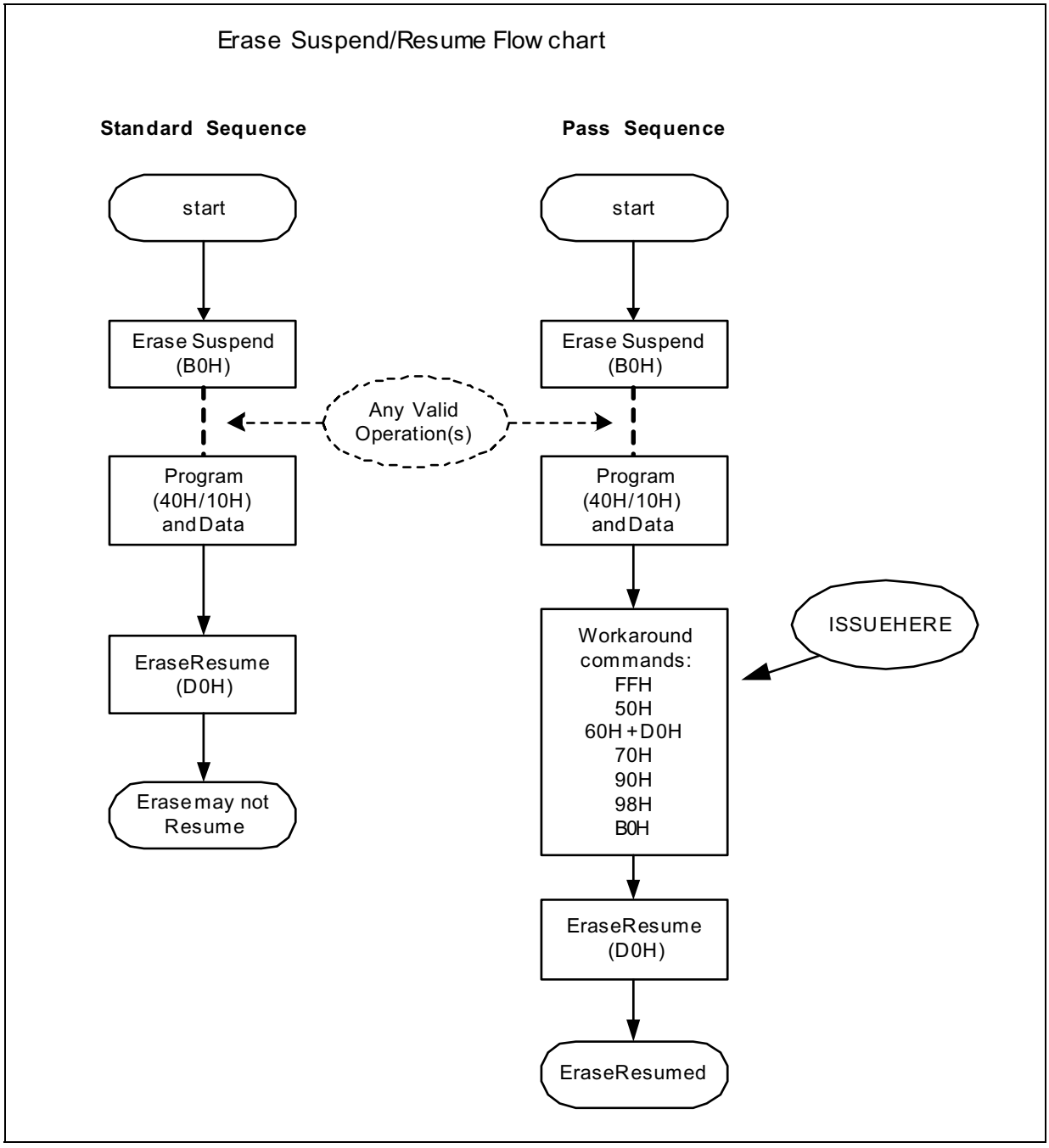
Workaround: There are 2 workarounds for this erratum.

1. If FDI (Intel Flash Data Integrator) software is used, users will not see the issue.
2. During an Erase-Suspend (B0H), user must issue any of the following commands after issuing the Program (40H/10H) and data sequence but before issuing the Erase-Resume (D0H) command.

Command	First Bus Cycle			Second Bus Cycle		
	Oper	Addr	Data	Oper	Addr	Data
Read Array	Write	X	FFH			
Read Configuration	Write	X	90H	Read	IA	ID
Read Query	Write	X	98H	Read	QA	QD
Read Status Register	Write	X	70H	Read	X	SRD
Clear Status Register	Write	X	50H			
Program/Erase Suspend	Write	X	B0H			
Unlock Block	Write	X	60H	Write	BA	D0H

PA: Program Address QA: Query Addr **BA:** Block Address QD: Query Data
IA: Identifier Address **ID:** Identifier Data **SRD:** Status Register Data

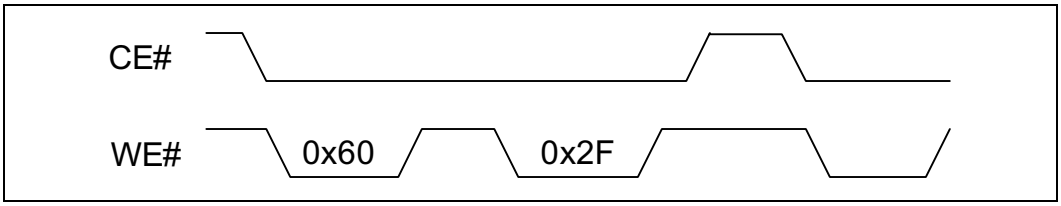
Figure 1. Workaround Placement



Status: Root cause has been identified. New material will be available in August 2002.

5. 28F160C3xC and 28F640C3xC Lock/Unlock/Lock-Down Operation

Problem: On the 16Mb and 64Mb 0.18µm devices, if CE# is deasserted after any block lock operation and before the next write sequence, the part may perform the same operation on additional blocks. (See waveform below.)



Implication: When CE# is deasserted after performing a block lock operation to a specific block and prior to the next write sequence, other blocks may perform the same operation.

Workaround: Depending on software implementation, systems may already be effectively managing this erratum. There is currently a workaround for this erratum:

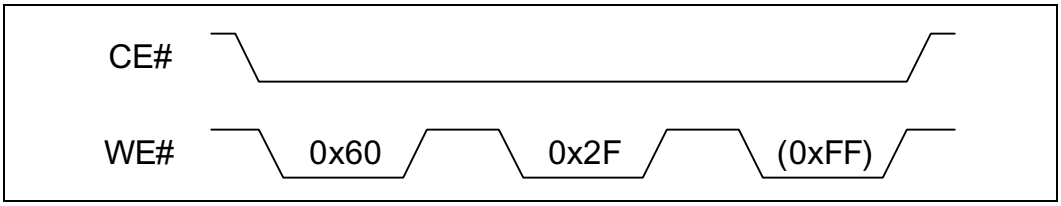
Immediately after performing a block lock, unlock, or lock-down operation, perform a valid write sequence before chip enable (CE#) is deasserted.

For example, one possible solution is shown below:

1) Assert CE# and toggle WE# to write the block lock setup command (0x60).

2) Toggle WE# a second time to write the confirm command (lock = 0x01; unlock = 0xD0; lock-down = 0x2F).

3) Toggle WE# a third time (ex: 0xFF- Read Array) before CE# is deasserted. (See waveform below.) Any other valid write sequence will also work (i.e., 0x90 - Read Configuration, 0x40 - Program, 0x20 - Erase).



Status: 16Mb and 64Mb devices on the 0.18µm process are affected. Root cause has been identified and this erratum may be fixed in a future stepping of the product.

Specification Changes

1. Maximum I_{CCD} Change

Issue: The maximum I_{CCD} increases from 20 µA to 25 µA on 0.25µm 8-Mb, 16-Mb and 32-Mb versions only. The following table shows the revised I_{CCD} specification.

Sym	Parameter	V_{CC}	2.7 V –3.6 V		Unit	Test Conditions
		V_{CCQ}	2.7 V –3.6 V			
		Note	Type	Max		
I_{CCD}	V_{CC} Deep Power-Down Current	1,7	7	25	µA	$V_{CC} = V_{CC}Max$ $V_{CCQ} = V_{CCQ}Max$ $V_{IN} = V_{CCQ}$ or GND RP# = GND ± 0.2 V

NOTE:
1. All currents are in RMS unless otherwise noted. Typical values at nominal V_{CC}, T_A = +25 °C.
2. The test conditions $V_{CC}Max$, $V_{CCQ}Max$, $V_{CC}Min$, and $V_{CCQ}Min$ refer to the maximum or minimum V_{CC} or V_{CCQ} voltage listed at the top of each column.

2. CFI Primary-Vendor Specific Extended Query Change

Issue: The value for address 3A in the CFI Primary-Vendor Specific Extended Query Table (Optional Feature and Command Support) has been changed from 0Eh to 66h.

Offset(1)	Length (bytes)	Description	8-Mbit, 16-Mbit, 32-Mbit
(P+5)h	04h	Optional Feature & Command Support bit 0 Chip Erase Supported (1=yes, **0=no**) bit 1 Suspend Erase Supported (**1=yes**, 0=no) bit 2 Suspend Program Supported (**1=yes,** 0=no) bit 3 Legacy Lock/Unlock Supported**)** (1=yes, **0=no**) bit 4 Queued Erase Supported (1=yes, **0=no**) bit 5 IBL Supported (2) (**1=yes,** 0=no) bit 6 OTP Bits Supported (3) (**1=yes**, 0=no) bit 7 Page Mode Reads Supported (1=yes, **0=no**) bit 8 Synchronous Burst Supported (1=yes, **0=no**) bits 9–31 reserved for future use; undefined bits are “0”	**3A: 66** 3B: 00 3C: 00 3D: 00

NOTES:
1. The variable P is a pointer that is defined at offset 15H Table D5
2. IIBL refers to “Instant, Individual Block Locking.”
3. OTP refers to “One Time Programmable.”

CFI templates that support the Advanced+ Boot Block features will recognize block locking and unlocking support on affected devices. The CFI Primary-Vendor Specific Extended Query Table will be corrected on future steppings.

3. Block Locking Command Sequence Change

Issue: A Read Status Register command must be issued following an Unlock Block command to a block that is in the Lockdown or Locked-Lockdown state. WP# must be held valid for all three bus

cycles. See the *3 Volt Advanced+ Boot Block Flash Memory* datasheet for a description of the Lockdown and Locked-Lockdown states.

Command	Notes	First Bus Cycle			Second Buss Cycle			Third Bus Cycle		
		Oper	Addr	Data	Oper	Addr	Data	Oper	Addr	Data
Unlock Block	4	Write	X	60H	Write	BA	D0H	Write	X	70H

Customers may need to modify their software. Note: If the Locking Operations Flowchart (Figure 16 in the datasheet) is implemented for locking operations with WP# held valid through the Read Status Register command, software modifications are not necessary. Future steppings will require WP# valid only through the Write Lock, Unlock, or Lockdown commands.

4. 0.25µm 32-Mb Maximum V_{CC} Change

Issue: The maximum V_{CC} decreases from 3.6 V to 3.3 V on 0.25µm 32-Mb versions only. The following table shows the revised V_{CC} specification.

Symbol	Parameter	Notes	Min	Max	Units
V_{CC}	V_{CC} Supply Voltage	1	2.7	3.3	Volts

Other implied specification changes, as a result of the V_{CC} change, are described in the following table:

Symbol	Parameter	Notes	Min	Max	Units
V_{CC1}	V_{CC} Supply Voltage	1	2.7	3.3	Volts
V_{CC2}	V_{CC} Supply Voltage	1	3.0	3.3	Volts
V_{CCQ1}	I/O Supply Voltage	1	2.7	3.3	Volts
V_{PP1}	Supply Voltage	1	1.65	3.3	Volts

NOTE: 1. V_{CC} and V_{CCQ} must share the same the same supply when they are in the V_{CC1} range.

The maximum V_{CC} has changed on the 0.25µm 32-Mb devices. The maximum V_{CC} specification has not changed on the 16-Mb, 8-Mb. This may become an issue if the system voltage regulator used has a V_{CC} range tolerance that is outside the new specification, which may cause the device to operate in a condition which is outside the specifications of the current datasheet.

Specification Clarifications

There are no specification clarifications in this Specification Update revision.

Documentation Changes

There are no documentation changes in this Specification Update revision.