CY7C1470BV25
CY7C1472BV25, CY7C1474BV25

72-Mbit (2M x 36/4M x 18/1M x 72) Pipelined SRAM with NoBL™ Architecture

Features

- Pin-compatible and functionally equivalent to ZBT™
- Supports 250 MHz bus operations with zero wait states
  - Available speed grades are 250, 200, and 167 MHz
- Internally self-timed output buffer control to eliminate the need to use asynchronous OE
- Fully registered (inputs and outputs) for pipelined operation
- Byte Write capability
- Single 2.5V power supply
- 2.5V IO supply (V_{DDQ})
- Fast clock-to-output times
  - 3.0 ns (for 250-MHz device)
- Clock Enable (CEN) pin to suspend operation
- Synchronous self-timed writes
- CY7C1470BV25, CY7C1472BV25 available in JEDEC-standard Pb-free 100-pin TQFP, Pb-free and non-Pb-free 165-ball FBGA package. CY7C1474BV25 available in Pb-free and non-Pb-free 209-ball FBGA package
- IEEE 1149.1 JTAG Boundary Scan compatible
- Burst capability—linear or interleaved burst order
- "ZZ" Sleep Mode option and Stop Clock option

Functional Description

The CY7C1470BV25, CY7C1472BV25, and CY7C1474BV25 are 2.5V, 2M x 36/4M x 18/1M x 72 synchronous pipelined burst SRAMs with No Bus Latency™ (NoBL™) logic, respectively. They are designed to support unlimited true back-to-back read or write operations with no wait states. The CY7C1470BV25, CY7C1472BV25, and CY7C1474BV25 are equipped with the advanced (NoBL) logic required to enable consecutive read or write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data in systems that require frequent read or write transitions. The CY7C1470BV25, CY7C1472BV25, and CY7C1474BV25 are pin-compatible and functionally equivalent to ZBT devices.

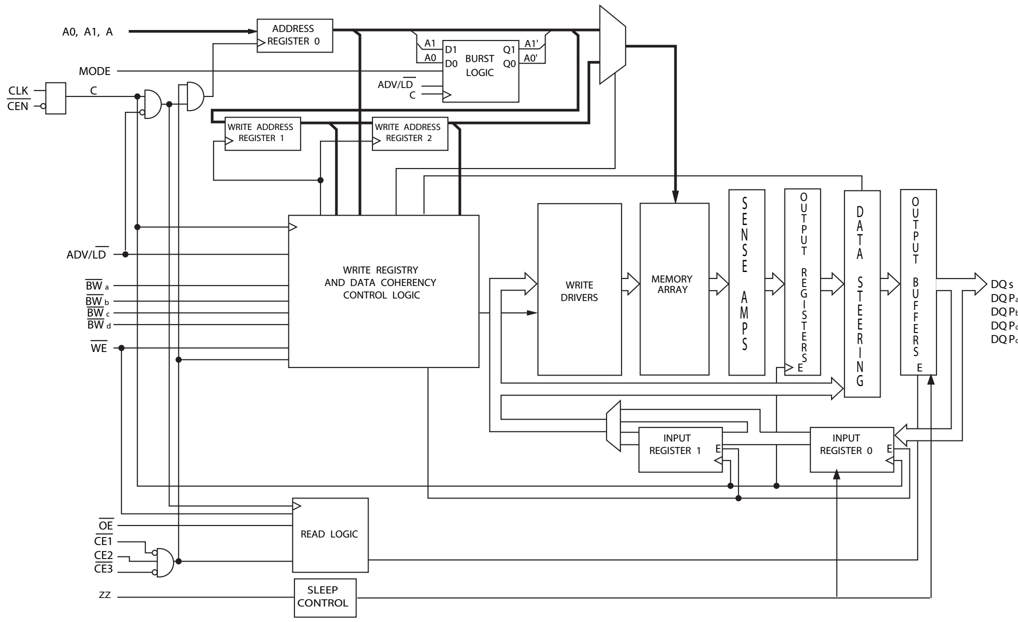
All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. The clock input is qualified by the Clock Enable (CEN) signal, which when deasserted suspends operation and extends the previous clock cycle. Write operations are controlled by the Byte Write Selects (BW_a–BW_d for CY7C1470BV25, BW_a–BW_b for CY7C1472BV25, and BW_a–BW_h for CY7C1474BV25) and a Write Enable (WE) input. All writes are conducted with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Enables ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous Output Enable (OE) provide for easy bank selection and output tri-state control. To avoid bus contention, the output drivers are synchronously tri-stated during the data portion of a write sequence.

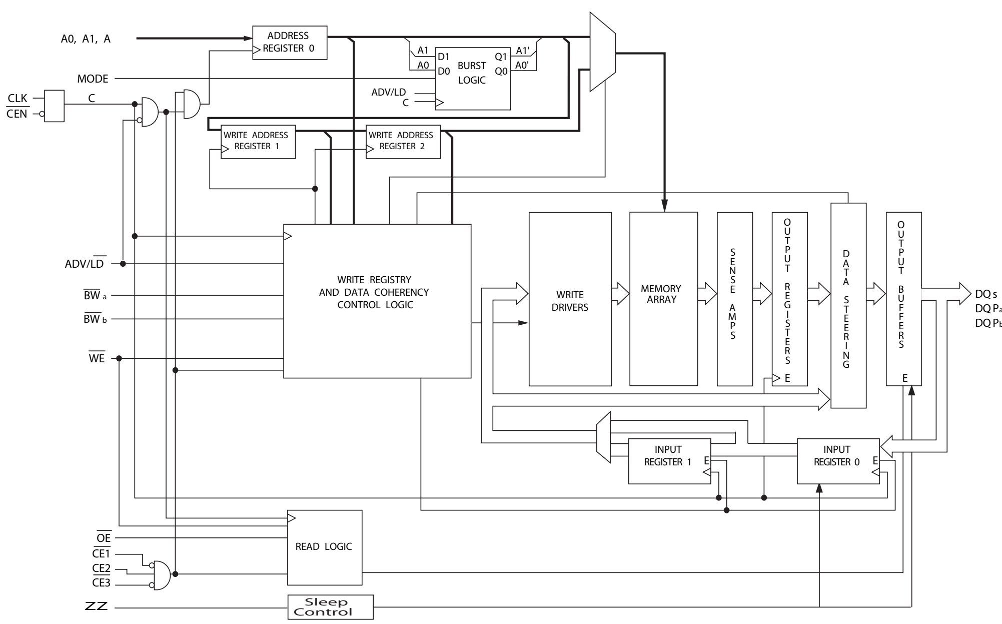
Selection Guide

Description	250 MHz	200 MHz	167 MHz	Unit
Maximum Access Time	3.0	3.0	3.4	ns
Maximum Operating Current	450	450	400	mA
Maximum CMOS Standby Current	120	120	120	mA

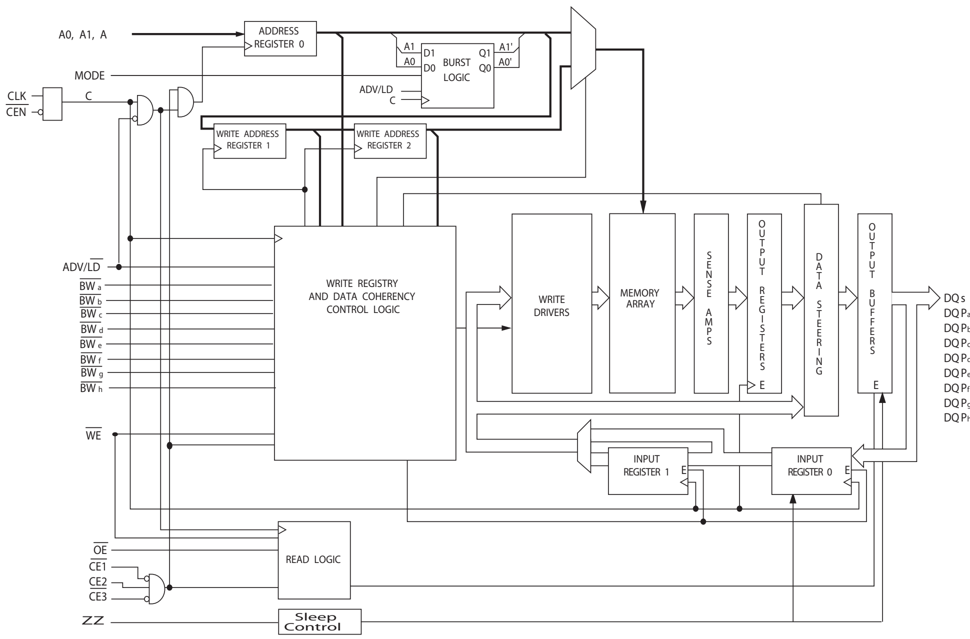
Logic Block Diagram – CY7C1470BV25 (2M x 36)



Logic Block Diagram – CY7C1472BV25 (4M x 18)

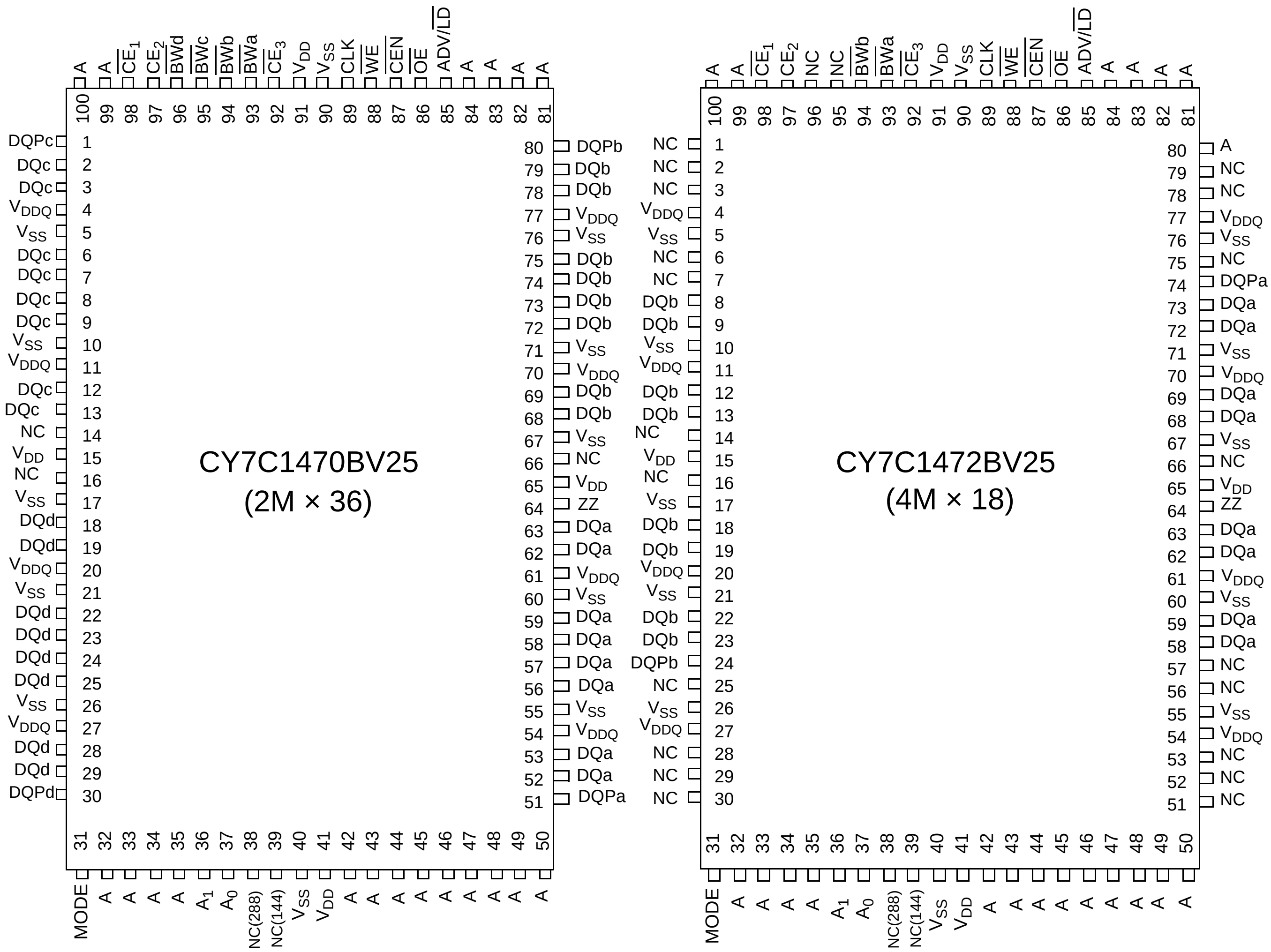


Logic Block Diagram – CY7C1474BV25 (1M x 72)



Pin Configurations

Figure 1. 100-Pin TQFP Pinout



Pin Configurations (continued)

165-Ball FBGA (15 x 17 x 1.4 mm) Pinout

CY7C1470BV25 (2M x 36)

	1	2	3	4	5	6	7	8	9	10	11
A	NC/576M	A	$\overline{CE}_1$	$\overline{BW}_c$	$\overline{BW}_b$	$\overline{CE}_3$	$\overline{CEN}$	ADV/$\overline{LD}$	A	A	NC
B	NC/1G	A	CE2	$\overline{BW}_d$	$\overline{BW}_a$	CLK	$\overline{WE}$	$\overline{OE}$	A	A	NC
C	DQP_c	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQP_b
D	DQ_c	DQ_c	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_b	DQ_b
E	DQ_c	DQ_c	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_b	DQ_b
F	DQ_c	DQ_c	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_b	DQ_b
G	DQ_c	DQ_c	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_b	DQ_b
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_d	DQ_d	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	DQ_a
K	DQ_d	DQ_d	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	DQ_a
L	DQ_d	DQ_d	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	DQ_a
M	DQ_d	DQ_d	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	DQ_a
N	DQP_d	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	DQP_a
P	NC/144M	A	A	A	TDI	A1	TDO	A	A	A	NC/288M
R	MODE	A	A	A	TMS	A0	TCK	A	A	A	A

CY7C1472BV25 (4M x 18)

	1	2	3	4	5	6	7	8	9	10	11
A	NC/576M	A	$\overline{CE}_1$	$\overline{BW}_b$	NC	$\overline{CE}_3$	$\overline{CEN}$	ADV/$\overline{LD}$	A	A	A
B	NC/1G	A	CE2	NC	$\overline{BW}_a$	CLK	$\overline{WE}$	$\overline{OE}$	A	A	NC
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQPa
D	NC	DQ_b	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_a
E	NC	DQ_b	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_a
F	NC	DQ_b	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_a
G	NC	DQ_b	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_a
H	NC	NC	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ
J	DQ_b	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	NC
K	DQ_b	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	NC
L	DQ_b	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	NC
M	DQ_b	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_a	NC
N	DQP_b	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	NC
P	NC/144M	A	A	A	TDI	A1	TDO	A	A	A	NC/288M
R	MODE	A	A	A	TMS	A0	TCK	A	A	A	A

Pin Configurations (continued)

209-Ball FBGA (14 x 22 x 1.76 mm) Pinout

CY7C1474BV25 (1M × 72)

	1	2	3	4	5	6	7	8	9	10	11
A	DQg	DQg	A	CE_2	A	ADV/$\overline{LD}$	A	$\overline{CE}_3$	A	DQb	DQb
B	DQg	DQg	$\overline{BWS}_c$	$\overline{BWS}_g$	NC	$\overline{WE}$	A	$\overline{BWS}_b$	$\overline{BWS}_f$	DQb	DQb
C	DQg	DQg	$\overline{BWS}_h$	$\overline{BWS}_d$	NC/576M	$\overline{CE}_1$	NC	$\overline{BWS}_e$	$\overline{BWS}_a$	DQb	DQb
D	DQg	DQg	V_{SS}	NC	NC/1G	$\overline{OE}$	NC	NC	V_{SS}	DQb	DQb
E	DQPg	DQPc	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQPf	DQPb
F	DQc	DQc	V_{SS}	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}	DQf	DQf
G	DQc	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	NC	V_{DD}	V_{DDQ}	V_{DDQ}	DQf	DQf
H	DQc	DQc	V_{SS}	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}	DQf	DQf
J	DQc	DQc	V_{DDQ}	V_{DDQ}	V_{DD}	NC	V_{DD}	V_{DDQ}	V_{DDQ}	DQf	DQf
K	NC	NC	CLK	NC	V_{SS}	$\overline{CEN}$	V_{SS}	NC	NC	NC	NC
L	DQh	DQh	V_{DDQ}	V_{DDQ}	V_{DD}	NC	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQa
M	DQh	DQh	V_{SS}	V_{SS}	V_{SS}	NC	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
N	DQh	DQh	V_{DDQ}	V_{DDQ}	V_{DD}	NC	V_{DD}	V_{DDQ}	V_{DDQ}	DQa	DQa
P	DQh	DQh	V_{SS}	V_{SS}	V_{SS}	ZZ	V_{SS}	V_{SS}	V_{SS}	DQa	DQa
R	DQPd	DQPh	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQPa	DQPe
T	DQd	DQd	V_{SS}	NC	NC	MODE	NC	NC	V_{SS}	DQe	DQe
U	DQd	DQd	NC/144M	A	A	A	A	A	NC/288M	DQe	DQe
V	DQd	DQd	A	A	A	A1	A	A	A	DQe	DQe
W	DQd	DQd	TMS	TDI	A	A0	A	TDO	TCK	DQe	DQe

Table 1. Pin Definitions

Pin Name	IO Type	Pin Description
A0 A1 A	Input-Synchronous	**Address Inputs Used to Select One of the Address Locations**. Sampled at the rising edge of the CLK.
$\overline{BW}_a$ $\overline{BW}_b$ $\overline{BW}_c$ $\overline{BW}_d$ $\overline{BW}_e$ $\overline{BW}_f$ $\overline{BW}_g$ $\overline{BW}_h$	Input-Synchronous	**Byte Write Select Inputs, Active LOW**. Qualified with $\overline{WE}$ to conduct writes to the SRAM. Sampled on the rising edge of CLK. $\overline{BW}_a$ controls DQ_a and DQP_a, $\overline{BW}_b$ controls DQ_b and DQP_b, $\overline{BW}_c$ controls DQ_c and DQP_c, $\overline{BW}_d$ controls DQ_d and DQP_d, $\overline{BW}_e$ controls DQ_e and DQP_e, $\overline{BW}_f$ controls DQ_f and DQP_f, $\overline{BW}_g$ controls DQ_g and DQP_g, $\overline{BW}_h$ controls DQ_h and DQP_h.
$\overline{WE}$	Input-Synchronous	**Write Enable Input, Active LOW**. Sampled on the rising edge of CLK if $\overline{CEN}$ is active LOW. This signal must be asserted LOW to initiate a write sequence.
ADV/$\overline{LD}$	Input-Synchronous	**Advance/Load Input Used to Advance the On-Chip Address Counter or Load a New Address**. When HIGH (and $\overline{CEN}$ is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, ADV/$\overline{LD}$ must be driven LOW to load a new address.
CLK	Input-Clock	**Clock Input**. Used to capture all synchronous inputs to the device. CLK is qualified with $\overline{CEN}$. CLK is only recognized if $\overline{CEN}$ is active LOW.
$\overline{CE}_1$	Input-Synchronous	**Chip Enable 1 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select/deselect the device.
CE_2	Input-Synchronous	**Chip Enable 2 Input, Active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device.
$\overline{CE}_3$	Input-Synchronous	**Chip Enable 3 Input, Active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device.
$\overline{OE}$	Input-Asynchronous	**Output Enable, Active LOW**. Combined with the synchronous logic block inside the device to control the direction of the IO pins. When LOW, the IO pins can behave as outputs. When deasserted HIGH, IO pins are tri-stated, and act as input data pins. $\overline{OE}$ is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state and when the device has been deselected.
$\overline{CEN}$	Input-Synchronous	**Clock Enable Input, Active LOW**. When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the clock signal is masked. Since deasserting $\overline{CEN}$ does not deselect the device, $\overline{CEN}$ can be used to extend the previous cycle when required.
DQ_s	IO-Synchronous	**Bidirectional Data IO Lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by $A_{[18:0]}$ during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$ and the internal control logic. When $\overline{OE}$ is asserted LOW, the pins can behave as outputs. When HIGH, DQ_a–DQ_h are placed in a tri-state condition. The outputs are automatically tri-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.
DQP_X	IO-Synchronous	**Bidirectional Data Parity IO Lines**. Functionally, these signals are identical to $DQ_{[71:0]}$. During write sequences, DQP_a is controlled by $\overline{BW}_a$, DQP_b is controlled by $\overline{BW}_b$, DQP_c is controlled by $\overline{BW}_c$, and DQP_d is controlled by $\overline{BW}_d$, DQP_e is controlled by $\overline{BW}_e$, DQP_f is controlled by $\overline{BW}_f$, DQP_g is controlled by $\overline{BW}_g$, DQP_h is controlled by $\overline{BW}_h$.
MODE	Input Strap Pin	**Mode Input**. Selects the burst order of the device. Tied HIGH selects the interleaved burst order. Pulled LOW selects the linear burst order. MODE must not change states during operation. When left floating MODE defaults HIGH, to an interleaved burst order.
TDO	JTAG Serial Output Synchronous	**Serial Data Out to the JTAG Circuit**. Delivers data on the negative edge of TCK.
TDI	JTAG Serial Input Synchronous	**Serial Data In to the JTAG Circuit**. Sampled on the rising edge of TCK.

Table 1. Pin Definitions (continued)

Pin Name	IO Type	Pin Description
TMS	Test Mode Select Synchronous	**TMS Pin Controls the Test Access Port State Machine**. Sampled on the rising edge of TCK.
TCK	JTAG Clock	**Clock Input to the JTAG Circuitry**.
V_{DD}	Power Supply	**Power Supply Inputs to the Core of the Device**.
V_{DDQ}	IO Power Supply	**Power Supply for the IO Circuitry**.
V_{SS}	Ground	**Ground for the Device**. Must be connected to ground of the system.
NC	–	**No Connects**. This pin is not connected to the die.
NC(144M, 288M, 576M, 1G)	–	**These Pins are Not Connected**. They are used for expansion to the 144M, 288M, 576M, and 1G densities.
ZZ	Input-Asynchronous	**ZZ "Sleep" Input**. This active HIGH input places the device in a non-time critical "sleep" condition with data integrity preserved. For normal operation, this pin has must be LOW or left floating. ZZ pin has an internal pull down.

Functional Overview

The CY7C1470BV25, CY7C1472BV25, and CY7C1474BV25 are synchronous-pipelined Burst NoBL SRAMs designed specifically to eliminate wait states during read or write transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the Clock Enable input signal (CEN). If CEN is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with CEN. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 3.0 ns (250-MHz device).

Accesses can be initiated by asserting all three Chip Enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) active at the rising edge of the clock. If CEN is active LOW and ADV/LD is asserted LOW, the address presented to the device is latched. The access can either be a read or write operation, depending on the status of the Write Enable (WE). $BW_{[x]}$ can be used to conduct Byte Write operations.

Write operations are qualified by the Write Enable ($\overline{WE}$). All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Enables ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) and an asynchronous Output Enable (OE) simplify depth expansion. All operations (reads, writes, and deselects) are pipelined. ADV/LD must be driven LOW after the device is deselected to load a new address for the next operation.

Single Read Accesses

A read access is initiated when the following conditions are satisfied at clock rise: (1) CEN is asserted LOW, (2) CE_1, CE_2, and CE_3 are ALL asserted active, (3) the input signal WE is deasserted HIGH, and (4) ADV/LD is asserted LOW. The address presented to the address inputs is latched into the Address Register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the rising edge of the next clock the requested data is allowed to propagate through the output register and onto the data bus within 2.6 ns (250-MHz device) provided OE is active LOW. After the first clock of the read access the output buffers are controlled by OE and the internal control logic. OE must be driven LOW to drive out the requested data. During the second clock, a subsequent operation (read, write, or deselect) can be initiated. Deselecting the device is also pipelined. Therefore, when the SRAM is deselected at clock rise by one of the chip enable signals, its output tri-states following the next clock rise.

Burst Read Accesses

The CY7C1470BV25, CY7C1472BV25, and CY7C1474BV25 have an on-chip burst counter that enables the user to supply a single address and conduct up to four reads without reasserting the address inputs. ADV/LD must be driven LOW to load a new address into the SRAM, as described in the Single Read Accesses section. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and wraps around when incremented sufficiently. A HIGH input on ADV/LD increments the internal burst counter regardless of the state of chip enables inputs or WE. WE is latched at the beginning of a burst cycle. Therefore, the type of access (read or write) is maintained throughout the burst sequence.

Single Write Accesses

Write accesses are initiated when the following conditions are satisfied at clock rise: (1) CEN is asserted LOW, (2) CE_1, CE_2, and CE_3 are ALL asserted active, and (3) the signal WE is asserted LOW. The address presented to the address inputs is loaded into the Address Register. The write signals are latched into the Control Logic block.

On the subsequent clock rise the data lines are automatically tri-stated regardless of the state of the OE input signal. This allows the external logic to present the data on DQ and DQP ($DQ_{a,b,c,d}$/$DQP_{a,b,c,d}$ for CY7C1470BV25, $DQ_{a,b}$/$DQP_{a,b}$ for CY7C1472BV25, and $DQ_{a,b,c,d,e,f,g,h}$/$DQP_{a,b,c,d,e,f,g,h}$ for CY7C1474BV25). In addition, the address for the subsequent access (read, write, or deselect) is latched into the Address Register (provided the appropriate control signals are asserted).

On the next clock rise the data presented to DQ and DQP ($DQ_{a,b,c,d}/DQP_{a,b,c,d}$ for CY7C1470BV25, $DQ_{a,b}/DQP_{a,b}$ for CY7C1472BV25, $DQ_{a,b,c,d,e,f,g,h}/DQP_{a,b,c,d,e,f,g,h}$ for CY7C1474BV25) (or a subset for Byte Write operations, see “Partial Write Cycle Description” on page 11 for details) inputs is latched into the device and the Write is complete.

The data written during the Write operation is controlled by $\overline{BW}$ ($\overline{BW}_{a,b,c,d}$ for CY7C1470BV25, $\overline{BW}_{a,b}$ for CY7C1472BV25, and $\overline{BW}_{a,b,c,d,e,f,g,h}$ for CY7C1474BV25) signals. The CY7C1470BV25, CY7C1472BV25, and CY7C1474BV25 provides Byte Write capability that is described in “Partial Write Cycle Description” on page 11. Asserting the $\overline{WE}$ input with the selected $\overline{BW}$ input selectively writes to only the desired bytes. Bytes not selected during a Byte Write operation remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations. Byte Write capability has been included to greatly simplify read, modify, or write sequences, which can be reduced to simple Byte Write operations.

Because the CY7C1470BV25, CY7C1472BV25, and CY7C1474BV25 are common IO devices, data must not be driven into the device while the outputs are active. $\overline{OE}$ can be deasserted HIGH before presenting data to the DQ and DQP ($DQ_{a,b,c,d}/DQP_{a,b,c,d}$ for CY7C1470BV25, $DQ_{a,b}/DQP_{a,b}$ for CY7C1472BV25, and $DQ_{a,b,c,d,e,f,g,h}/DQP_{a,b,c,d,e,f,g,h}$ for CY7C1474BV25) inputs. Doing so tri-states the output drivers. As a safety precaution, DQ and DQP ($DQ_{a,b,c,d}/DQP_{a,b,c,d}$ for CY7C1470BV25, $DQ_{a,b}/DQP_{a,b}$ for CY7C1472BV25, and $DQ_{a,b,c,d,e,f,g,h}/DQP_{a,b,c,d,e,f,g,h}$ for CY7C1474BV25) are automatically tri-stated during the data portion of a write cycle, regardless of the state of $\overline{OE}$.

Burst Write Accesses

The CY7C1470BV25, CY7C1472BV25, and CY7C1474BV25 has an on-chip burst counter that enables the user to supply a single address and conduct up to four write operations without reasserting the address inputs. ADV/$\overline{LD}$ must be driven LOW to load the initial address, as described in “Single Write Accesses” on page 8. When ADV/$\overline{LD}$ is driven HIGH on the subsequent clock rise, the Chip Enables ($\overline{CE}_1$, CE_2, and $\overline{CE}_3$) and $\overline{WE}$ inputs are ignored and the burst counter is incremented. The correct $\overline{BW}$ ($\overline{BW}_{a,b,c,d}$ for CY7C1470BV25, $\overline{BW}_{a,b}$ for CY7C1472BV25, and $\overline{BW}_{a,b,c,d,e,f,g,h}$ for CY7C1474BV25) inputs must be driven in each cycle of the burst write to write the correct bytes of data.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected before entering the “sleep” mode. $\overline{CE}_1$, CE_2, and $\overline{CE}_3$, must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Table 2. Linear Burst Address Table (MODE = GND)

First Address	Second Address	Third Address	Fourth Address
A1,A0	A1,A0	A1,A0	A1,A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Table 3. Interleaved Burst Address Table (MODE = Floating or V_{DD})

First Address	Second Address	Third Address	Fourth Address
A1,A0	A1,A0	A1,A0	A1,A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	$ZZ \geq V_{DD} - 0.2V$		120	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2V$		$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2V$	$2t_{CYC}$		ns
t_{ZZI}	ZZ active to sleep current	This parameter is sampled		$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit sleep current	This parameter is sampled	0		ns

Table 4. Truth Table

The truth table for CY7C1470BV25, CY7C1472BV25, and CY7C1474BV25 follows. [1, 2, 3, 4, 5, 6, 7]

Operation	Address Used	$\overline{CE}$	ZZ	ADV/$\overline{LD}$	$\overline{WE}$	$\overline{BW}_x$	$\overline{OE}$	$\overline{CEN}$	CLK	DQ
Deselect Cycle	None	H	L	L	X	X	X	L	L-H	Tri-State
Continue Deselect Cycle	None	X	L	H	X	X	X	L	L-H	Tri-State
Read Cycle (Begin Burst)	External	L	L	L	H	X	L	L	L-H	Data Out (Q)
Read Cycle (Continue Burst)	Next	X	L	H	X	X	L	L	L-H	Data Out (Q)
NOP/Dummy Read (Begin Burst)	External	L	L	L	H	X	H	L	L-H	Tri-State
Dummy Read (Continue Burst)	Next	X	L	H	X	X	H	L	L-H	Tri-State
Write Cycle (Begin Burst)	External	L	L	L	L	L	X	L	L-H	Data In (D)
Write Cycle (Continue Burst)	Next	X	L	H	X	L	X	L	L-H	Data In (D)
NOP/Write Abort (Begin Burst)	None	L	L	L	L	H	X	L	L-H	Tri-State
Write Abort (Continue Burst)	Next	X	L	H	X	H	X	L	L-H	Tri-State
Ignore Clock Edge (Stall)	Current	X	L	X	X	X	X	H	L-H	–
Sleep Mode	None	X	H	X	X	X	X	X	X	Tri-State

Notes
1. X = "Don't Care", H = Logic HIGH, L = Logic LOW, $\overline{CE}$ stands for ALL Chip Enables active. $\overline{BW}_x$ = L signifies at least one Byte Write Select is active, $\overline{BW}_x$ = Valid signifies that the desired Byte Write Selects are asserted, see "Partial Write Cycle Description" on page 11 for details.
2. Write is defined by $\overline{WE}$ and $\overline{BW}_{[a:d]}$. See "Partial Write Cycle Description" on page 11 for details.
3. When a write cycle is detected, all IOs are tri-stated, even during Byte Writes.
4. The DQ and DQP pins are controlled by the current cycle and the $\overline{OE}$ signal.
5. $\overline{CEN}$ = H inserts wait states.
6. Device powers up deselected with the IOs in a tri-state condition, regardless of $\overline{OE}$.
7. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles.During a Read cycle DQ_s and $DQP_{[a:d]}$ = tri-state when $\overline{OE}$ is inactive or when the device is deselected, and DQ_s = data when $\overline{OE}$ is active.

Table 5. Partial Write Cycle Description

The partial write cycle description for CY7C1470BV25, CY7C1472BV25, and CY7C1474BV25 follows.[1, 2, 3, 8]

Function (CY7C1470BV25)	$\overline{WE}$	$\overline{BW}_d$	$\overline{BW}_c$	$\overline{BW}_b$	$\overline{BW}_a$
Read	H	X	X	X	X
Write – No bytes written	L	H	H	H	H
Write Byte a – (DQ_a and DQP_a)	L	H	H	H	L
Write Byte b – (DQ_b and DQP_b)	L	H	H	L	H
Write Bytes b, a	L	H	H	L	L
Write Byte c – (DQ_c and DQP_c)	L	H	L	H	H
Write Bytes c, a	L	H	L	H	L
Write Bytes c, b	L	H	LL	L	H
Write Bytes c, b, a	L	H	L	L	L
Write Byte d – (DQ_d and DQP_d)	L	L	H	H	H
Write Bytes d, a	L	L	H	H	L
Write Bytes d, b	L	L	H	L	H
Write Bytes d, b, a	L	L	H	L	L
Write Bytes d, c	L	L	L	H	H
Write Bytes d, c, a	L	L	L	H	L
Write Bytes d, c, b	L	L	L	L	H
Write All Bytes	L	L	L	L	L

Function (CY7C1472BV25)	$\overline{WE}$	$\overline{BW}_b$	$\overline{BW}_a$
Read	H	x	x
Write – No Bytes Written	L	H	H
Write Byte a – (DQ_a and DQP_a)	L	H	L
Write Byte b – (DQ_b and DQP_b)	L	L	H
Write Both Bytes	L	L	L

Function (CY7C1474BV25)	$\overline{WE}$	$\overline{BW}_x$
Read	H	x
Write – No Bytes Written	L	H
Write Byte X – (DQ_x and DQP_x)	L	L
Write All Bytes	L	All $\overline{BW}$ = L

Note

8. Table lists only a partial listing of the Byte Write combinations. Any combination of $\overline{BW}_{[a:d]}$ is valid. Appropriate write is based on which Byte Write is active.

IEEE 1149.1 Serial Boundary Scan (JTAG)

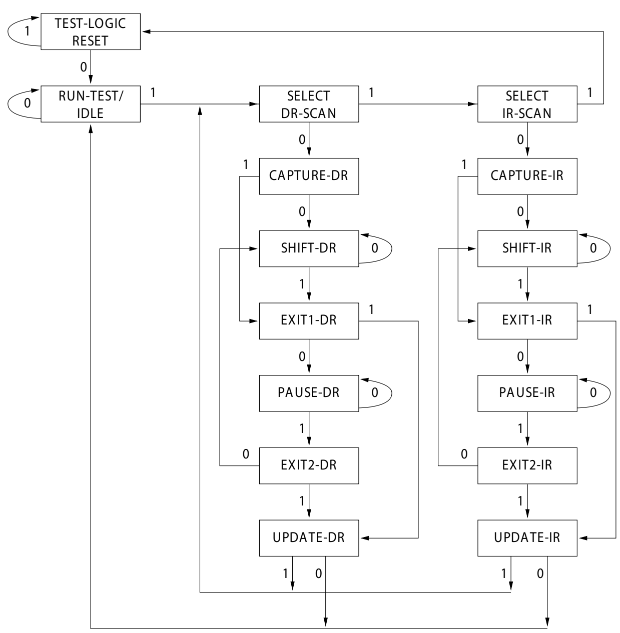
The CY7C1470BV25, CY7C1472BV25, and CY7C1474BV25 incorporates a serial boundary scan test access port (TAP). This port operates in accordance with IEEE Standard 1149.1-1990 but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC-standard 2.5V IO logic levels.

The CY7C1470BV25, CY7C1472BV25, and CY7C1474BV25 contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull up resistor. TDO must be left unconnected. During power up, the device comes up in a reset state, which does not interfere with the operation of the device.

Figure 2. TAP Controller State Diagram



The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test MODE SELECT (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

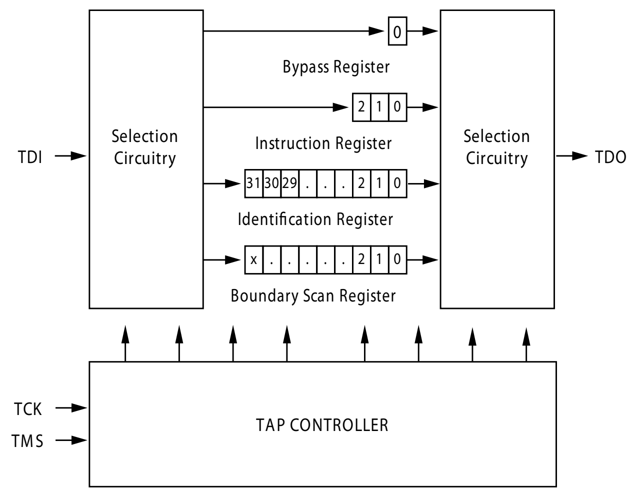
Test Data-In (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information about loading the instruction register, see the TAP Controller State Diagram. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register. (See TAP Controller Block Diagram.)

Test Data-Out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. (See TAP Controller State Diagram.)

Figure 3. TAP Controller Block Diagram



Performing a TAP Reset

A RESET is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

During power up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP Registers

Registers are connected between the TDI and TDO balls to scan the data in and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the "TAP Controller Block Diagram" on page 12. During power up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary '01' pattern to enable fault isolation of the board-level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This shifts the data through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM.

The boundary scan register is loaded with the contents of the RAM IO ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the IO ring.

The Boundary Scan Order tables on page 17 show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in "Identification Register Definitions" on page 16.

TAP Instruction Set

Overview

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in "Identification Codes" on page 17. Three of these instructions are listed as RESERVED and must not be used. The other five instructions are described in this section in detail.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented.

The TAP controller cannot be used to load address data or control signals into the SRAM and cannot preload the IO buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; rather, it performs a capture of the IO ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction after it is shifted in, the TAP controller must be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in this SRAM TAP controller, and therefore this device is not compliant to 1149.1. The TAP controller does recognize an all-0 instruction.

When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

IDCODE

The IDCODE instruction loads a vendor-specific, 32-bit code into the instruction register. It also places the instruction register between the TDI and TDO balls and shifts the IDCODE out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register during power up or whenever the TAP controller is in a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction connects the boundary scan register between the TDI and TDO pins when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the device TAP controller is not fully 1149.1 compliant.

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and bidirectional balls is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output may undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that is captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time (t_{CS} plus t_{CH}).

The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CLK captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO balls.

Note that since the PRELOAD part of the command is not implemented, putting the TAP to the Update-DR state while performing a SAMPLE/PRELOAD instruction has the same effect as the Pause-DR command.

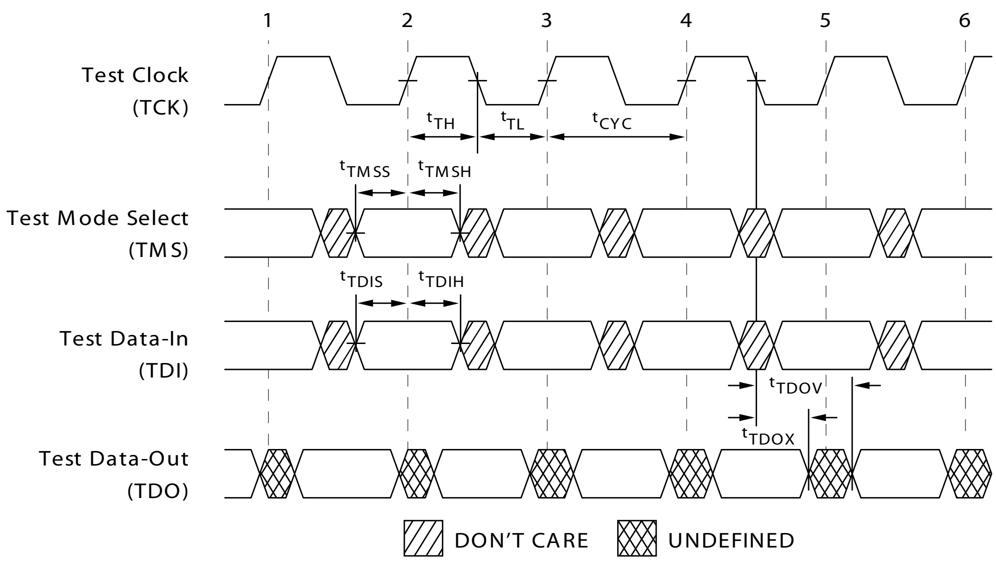
BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO balls. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

Figure 4. TAP Timing



TAP AC Switching Characteristics

Over the Operating Range [9, 10]

Parameter	Description	Min	Max	Unit
Clock				
t_{TCYC}	TCK Clock Cycle Time	50		ns
t_{TF}	TCK Clock Frequency		20	MHz
t_{TH}	TCK Clock HIGH time	20		ns
t_{TL}	TCK Clock LOW time	20		ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid		10	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0		ns
Setup Times				
t_{TMSS}	TMS Setup to TCK Clock Rise	5		ns
t_{TDIS}	TDI Setup to TCK Clock Rise	5		ns
t_{CS}	Capture Setup to TCK Rise	5		ns
Hold Times				
t_{TMSH}	TMS Hold after TCK Clock Rise	5		ns
t_{TDIH}	TDI Hold after Clock Rise	5		ns
t_{CH}	Capture Hold after Clock Rise	5		ns

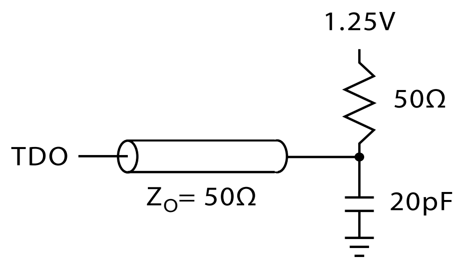
Notes

9. t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.
10. Test conditions are specified using the load in TAP AC Test Conditions. t_R/t_F = 1 ns.

2.5V TAP AC Test Conditions

Input pulse levels .... V_{SS} to 2.5V
Input rise and fall time .... 1 ns
Input timing reference levels.. 1.25V
Output reference levels 1.25V
Test load termination supply voltage 1.25V

Figure 5. 2.5V TAP AC Output Load Equivalent



TAP DC Electrical Characteristics And Operating Conditions

(0°C < T_A < +70°C; V_{DD} = 2.5V ±0.125V unless otherwise noted)[11]

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH1}	Output HIGH Voltage	I_{OH} = –1.0 mA, V_{DDQ} = 2.5V	1.7		V
V_{OH2}	Output HIGH Voltage	I_{OH} = –100 µA, V_{DDQ} = 2.5V	2.1		V
V_{OL1}	Output LOW Voltage	I_{OL} = 1.0 mA, V_{DDQ} = 2.5V		0.4	V
V_{OL2}	Output LOW Voltage	I_{OL} = 100 µA, V_{DDQ} = 2.5V		0.2	V
V_{IH}	Input HIGH Voltage	V_{DDQ} = 2.5V	1.7	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage	V_{DDQ} = 2.5V	–0.3	0.7	V
I_X	Input Load Current	GND ≤ V_I ≤ V_{DDQ}	–5	5	µA

Table 6. Identification Register Definitions

Instruction Field	CY7C1470BV25 (2M x 36)	CY7C1472BV25 (4M x 18)	CY7C1474BV25 (1M x 72)	Description
Revision Number (31:29)	000	000	000	Describes the version number
Device Depth (28:24)	01011	01011	01011	Reserved for internal use
Architecture/Memory Type(23:18)	001000	001000	001000	Defines memory type and architecture
Bus Width/Density(17:12)	100100	010100	110100	Defines width and density
Cypress JEDEC ID Code (11:1)	00000110100	00000110100	00000110100	Allows unique identification of SRAM vendor
ID Register Presence Indicator (0)	1	1	1	Indicates the presence of an ID register

Table 7. Scan Register Sizes

Register Name	Bit Size (x36)	Bit Size (x18)	Bit Size (x72)
Instruction	3	3	3
Bypass	1	1	1
ID	32	32	32
Boundary Scan Order–165FBGA	71	52	–
Boundary Scan Order–209BGA	–	–	110

Note
11. All voltages refer to V_{SS} (GND).

Table 8. Identification Codes

Instruction	Code	Description
EXTEST	000	Captures IO ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to High-Z state. This instruction is not 1149.1-compliant.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures IO ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures IO ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation. This instruction does not implement 1149.1 preload function and is therefore not 1149.1-compliant.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

Table 9. Boundary Scan Exit Order (2M x 36)

Bit #	165-Ball ID	Bit #	165-Ball ID	Bit #	165-Ball ID	Bit #	165-Ball ID
1	C1	21	R3	41	J11	61	B7
2	D1	22	P2	42	K10	62	B6
3	E1	23	R4	43	J10	63	A6
4	D2	24	P6	44	H11	64	B5
5	E2	25	R6	45	G11	65	A5
6	F1	26	R8	46	F11	66	A4
7	G1	27	P3	47	E11	67	B4
8	F2	28	P4	48	D10	68	B3
9	G2	29	P8	49	D11	69	A3
10	J1	30	P9	50	C11	70	A2
11	K1	31	P10	51	G10	71	B2
12	L1	32	R9	52	F10		
13	J2	33	R10	53	E10		
14	M1	34	R11	54	A9		
15	N1	35	N11	55	B9		
16	K2	36	M11	56	A10		
17	L2	37	L11	57	B10		
18	M2	38	M10	58	A8		
19	R1	39	L10	59	B8		
20	R2	40	K11	60	A7		

Boundary Scan Exit Order (4M x 18)

Bit #	165-Ball ID
1	D2
2	E2
3	F2
4	G2
5	J1
6	K1
7	L1
8	M1
9	N1
10	R1
11	R2
12	R3
13	P2
14	R4
15	P6
16	R6
17	R8
18	P3
19	P4
20	P8
21	P9
22	P10
23	R9
24	R10
25	R11
26	M10
27	L10
28	K10
29	J10
30	H11
31	G11
32	F11
33	E11
34	D11
35	C11
36	A11
37	A9
38	B9
39	A10
40	B10
41	A8
42	B8
43	A7
44	B7
45	B6
46	A6
47	B5
48	A4
49	B3
50	A3
51	A2
52	B2

Boundary Scan Exit Order (1M x 72)

Bit #	209-Ball ID
1	A1
2	A2
3	B1
4	B2
5	C1
6	C2
7	D1
8	D2
9	E1
10	E2
11	F1
12	F2
13	G1
14	G2
15	H1
16	H2
17	J1
18	J2
19	L1
20	L2
21	M1
22	M2
23	N1
24	N2
25	P1
26	P2
27	R2
28	R1
29	T1
30	T2
31	U1
32	U2
33	V1
34	V2
35	W1
36	W2
37	T6
38	V3
39	V4
40	U4
41	W5
42	V6
43	W6
44	V5
45	U5
46	U6
47	W7
48	V7
49	U7
50	V8
51	V9
52	W11
53	W10
54	V11
55	V10
56	U11
57	U10
58	T11
59	T10
60	R11
61	R10
62	P11
63	P10
64	N11
65	N10
66	M11
67	M10
68	L11
69	L10
70	P6
71	J11
72	J10
73	H11
74	H10
75	G11
76	G10
77	F11
78	F10
79	E10
80	E11
81	D11
82	D10
83	C11
84	C10
85	B11
86	B10
87	A11
88	A10
89	A7
90	A5
91	A9
92	U8
93	A6
94	D6
95	K6
96	B6
97	K3
98	A8
99	B4
100	B3
101	C3
102	C4
103	C8
104	C9
105	B9
106	B8
107	A4
108	C6
109	B7
110	A3

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature .... –65°C to +150°C

Ambient Temperature with
Power Applied .... –55°C to +125°C

Supply Voltage on V_{DD} Relative to GND ....–0.5V to +3.6V

Supply Voltage on V_{DDQ} Relative to GND ....–0.5V to $+V_{DD}$

DC to Outputs in Tri-State...................–0.5V to V_{DDQ} + 0.5V

DC Input Voltage .... –0.5V to V_{DD} + 0.5V

Current into Outputs (LOW) .... 20 mA

Static Discharge Voltage... > 2001V
(MIL-STD-883, Method 3015)

Latch up Current.. > 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	2.5V –5%/+5%	2.5V–5% to V_{DD}
Industrial	–40°C to +85°C		

Electrical Characteristics

Over the Operating Range[12, 13]

Parameter	Description	Test Conditions		Min	Max	Unit
V_{DD}	Power Supply Voltage			2.375	2.625	V
V_{DDQ}	IO Supply Voltage	For 2.5V IO		2.375	V_{DD}	V
V_{OH}	Output HIGH Voltage	For 2.5V IO, $I_{OH}= -1.0$ mA		2.0		V
V_{OL}	Output LOW Voltage	For 2.5V IO, $I_{OL}= 1.0$ mA			0.4	V
V_{IH}	Input HIGH Voltage[12]	For 2.5V IO		1.7	V_{DD} + 0.3V	V
V_{IL}	Input LOW Voltage[12]	For 2.5V IO		–0.3	0.7	V
I_X	Input Leakage Current except ZZ and MODE	$GND \le V_I \le V_{DDQ}$		–5	5	µA
	Input Current of MODE	Input = V_{SS}		–30		µA
		Input = V_{DD}			5	µA
	Input Current of ZZ	Input = V_{SS}		–5		µA
		Input = V_{DD}			30	µA
I_{OZ}	Output Leakage Current	$GND \le V_I \le V_{DDQ,}$ Output Disabled		–5	5	µA
I_{DD} [14]	V_{DD} Operating Supply	V_{DD} = Max, I_{OUT} = 0 mA, $f = f_{MAX} = 1/t_{CYC}$	4.0-ns cycle, 250 MHz		450	mA
			5.0-ns cycle, 200 MHz		450	mA
			6.0-ns cycle, 167 MHz		400	mA
I_{SB1}	Automatic CE Power Down Current—TTL Inputs	Max. V_{DD}, Device Deselected, $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$, $f = f_{MAX} = 1/t_{CYC}$	4.0-ns cycle, 250MHz		200	mA
			5.0-ns cycle, 200 MHz		200	mA
			6.0-ns cycle, 167 MHz		200	mA
I_{SB2}	Automatic CE Power Down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, $V_{IN} \le 0.3V$ or $V_{IN} \ge V_{DDQ} - 0.3V$, f = 0	All speed grades		120	mA

Notes
12. Overshoot: $V_{IH}(AC) < V_{DD}$ +1.5V (pulse width less than $t_{CYC}/2$). Undershoot: $V_{IL}(AC) > -2V$ (pulse width less than $t_{CYC}/2$).
13. $T_{Power-up}$: assumes a linear ramp from 0V to V_{DD} (min.) within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \le V_{DD}$.
14. The operation current is calculated with 50% read cycle and 50% write cycle.

Electrical Characteristics

Over the Operating Range[12, 13] (continued)

Parameter	Description	Test Conditions		Min	Max	Unit
I_{SB3}	Automatic CE Power Down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, $V_{IN} \leq 0.3V$ or $V_{IN} \geq V_{DDQ} - 0.3V$, $f = f_{MAX} = 1/t_{CYC}$	4.0-ns cycle, 250 MHz		200	mA
			5.0-ns cycle, 200 MHz		200	mA
			6.0-ns cycle, 167 MHz		200	mA
I_{SB4}	Automatic CE Power Down Current—TTL Inputs	Max. V_{DD}, Device Deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = 0	All speed grades		135	mA

Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	100 TQFP Max	165 FBGA Max	209 FBGA Max	Unit
$C_{ADDRESS}$	Address Input Capacitance	$T_A = 25°C$, f = 1 MHz, $V_{DD} = 2.5V$ $V_{DDQ} = 2.5V$	6	6	6	pF
C_{DATA}	Data Input Capacitance		5	5	5	pF
C_{CTRL}	Control Input Capacitance		8	8	8	pF
C_{CLK}	Clock Input Capacitance		6	6	6	pF
C_{IO}	Input/Output Capacitance		5	5	5	pF

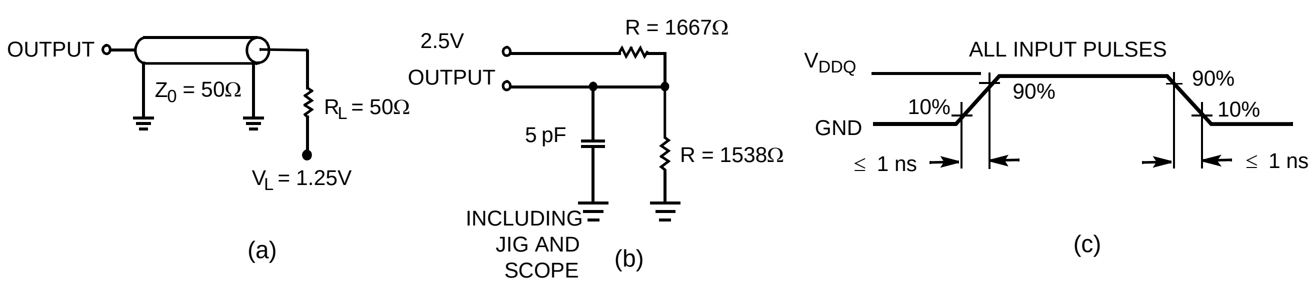
Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	100 TQFP Package	165 FBGA Package	209 FBGA Package	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	24.63	16.3	15.2	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		2.28	2.1	1.7	°C/W

AC Test Loads and Waveforms

2.5V IO Test Load



Switching Characteristics

Over the Operating Range. Timing reference is 1.25V when V_{DDQ} = 2.5V. Test conditions shown in (a) of "AC Test Loads and Waveforms" on page 20 unless otherwise noted.

Parameter	Description	–250		–200		–167		Unit
		Min	Max	Min	Max	Min	Max	
t_{Power}[15]	V_{CC} (typical) to the First Access Read or Write	1		1		1		ms
Clock								
t_{CYC}	Clock Cycle Time	4.0		5.0		6.0		ns
F_{MAX}	Maximum Operating Frequency		250		200		167	MHz
t_{CH}	Clock HIGH	2.0		2.0		2.2		ns
t_{CL}	Clock LOW	2.0		2.0		2.2		ns
Output Times								
t_{CO}	Data Output Valid After CLK Rise		3.0		3.0		3.4	ns
t_{OEV}	$\overline{OE}$ LOW to Output Valid		3.0		3.0		3.4	ns
t_{DOH}	Data Output Hold After CLK Rise	1.3		1.3		1.5		ns
t_{CHZ}	Clock to High-Z[16, 17, 18]		3.0		3.0		3.4	ns
t_{CLZ}	Clock to Low-Z[16, 17, 18]	1.3		1.3		1.5		ns
t_{EOHZ}	$\overline{OE}$ HIGH to Output High-Z[16, 17, 18]		3.0		3.0		3.4	ns
t_{EOLZ}	$\overline{OE}$ LOW to Output Low-Z[16, 17, 18]	0		0		0		ns
Setup Times								
t_{AS}	Address Setup Before CLK Rise	1.4		1.4		1.5		ns
t_{DS}	Data Input Setup Before CLK Rise	1.4		1.4		1.5		ns
t_{CENS}	$\overline{CEN}$ Setup Before CLK Rise	1.4		1.4		1.5		ns
t_{WES}	$\overline{WE}$, $\overline{BW}_X$ Setup Before CLK Rise	1.4		1.4		1.5		ns
t_{ALS}	ADV/$\overline{LD}$ Setup Before CLK Rise	1.4		1.4		1.5		ns
t_{CES}	Chip Select Setup	1.4		1.4		1.5		ns
Hold Times								
t_{AH}	Address Hold After CLK Rise	0.4		0.4		0.5		ns
t_{DH}	Data Input Hold After CLK Rise	0.4		0.4		0.5		ns
t_{CENH}	$\overline{CEN}$ Hold After CLK Rise	0.4		0.4		0.5		ns
t_{WEH}	$\overline{WE}$, $\overline{BW}_X$ Hold After CLK Rise	0.4		0.4		0.5		ns
t_{ALH}	ADV/$\overline{LD}$ Hold after CLK Rise	0.4		0.4		0.5		ns
t_{CEH}	Chip Select Hold After CLK Rise	0.4		0.4		0.5		ns

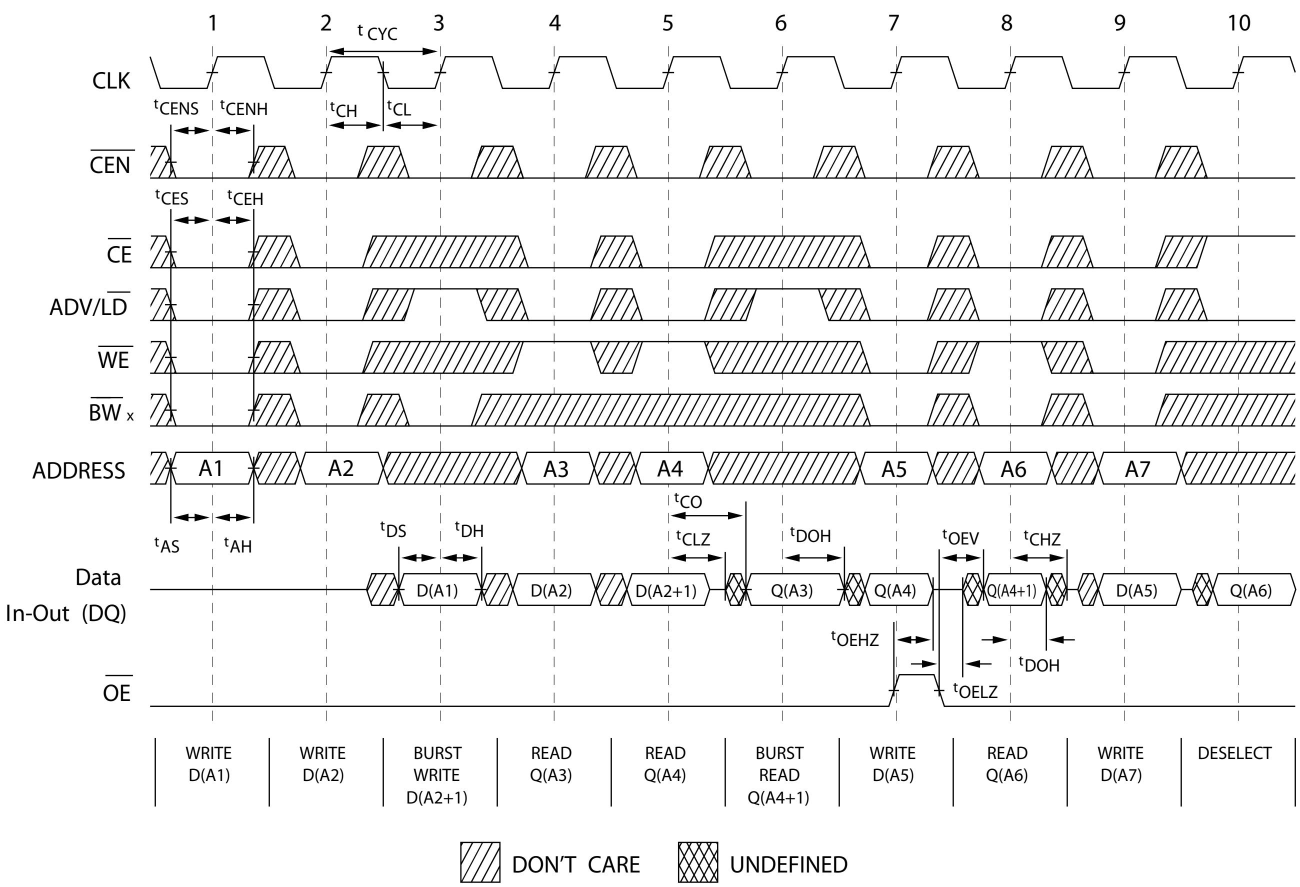
Notes

15. This part has a voltage regulator internally; t_{power} is the time power is supplied above V_{DD} minimum initially, before a read or write operation can be initiated.
16. t_{CHZ}, t_{CLZ}, t_{EOLZ}, and t_{EOHZ} are specified with AC test conditions shown in (b) of "AC Test Loads and Waveforms" on page 20. Transition is measured ±200 mV from steady-state voltage.
17. At any supplied voltage and temperature, t_{EOHZ} is less than t_{EOLZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High-Z before Low-Z under the same system conditions.
18. This parameter is sampled and not 100% tested.

Switching Waveforms

Figure 6 shows read-write timing waveform.[19, 20, 21]

Figure 6. Read/Write Timing



Notes

19. For this waveform ZZ is tied LOW.
20. When $\overline{CE}$ is LOW, $\overline{CE}_1$ is LOW, CE_2 is HIGH, and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH, $\overline{CE}_1$ is HIGH, CE_2 is LOW, or $\overline{CE}_3$ is HIGH.
21. Order of the Burst sequence is determined by the status of the MODE (0 = Linear, 1 = Interleaved).Burst operations are optional.

Switching Waveforms (continued)

Figure 7 shows NOP, STALL and DESELECT Cycles waveform.[19, 20, 22]

Figure 7. NOP, STALL and DESELECT Cycles

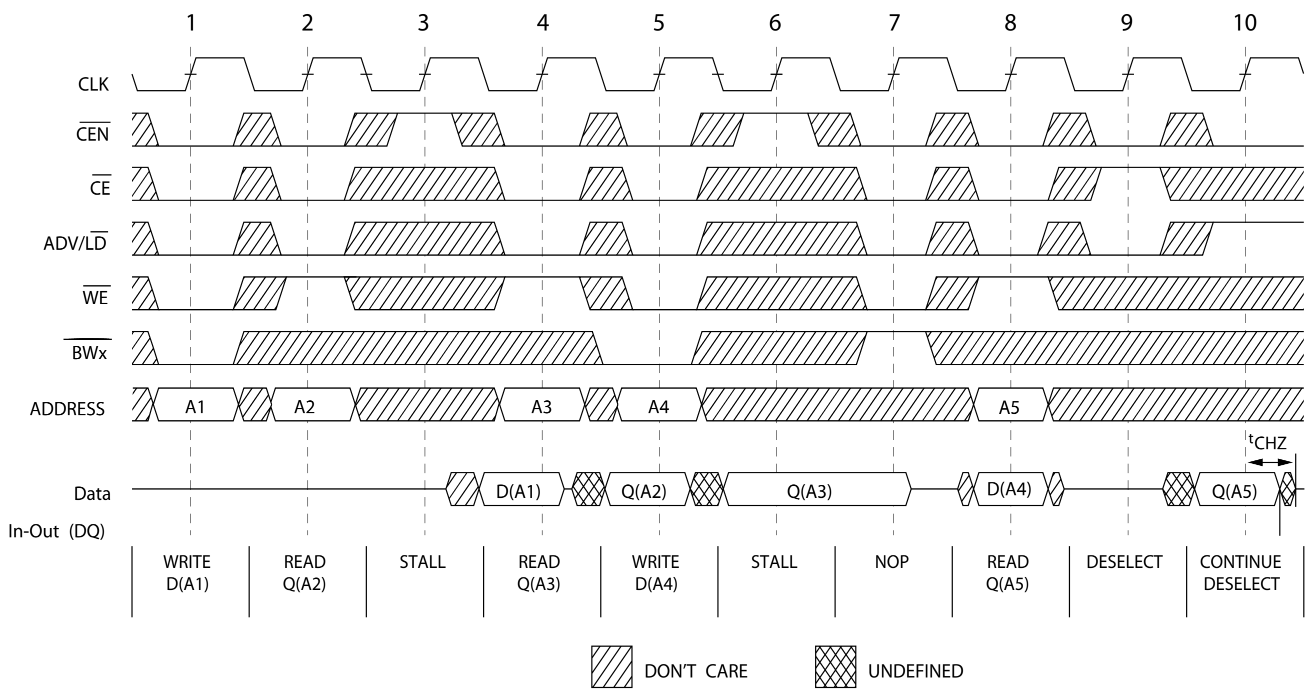
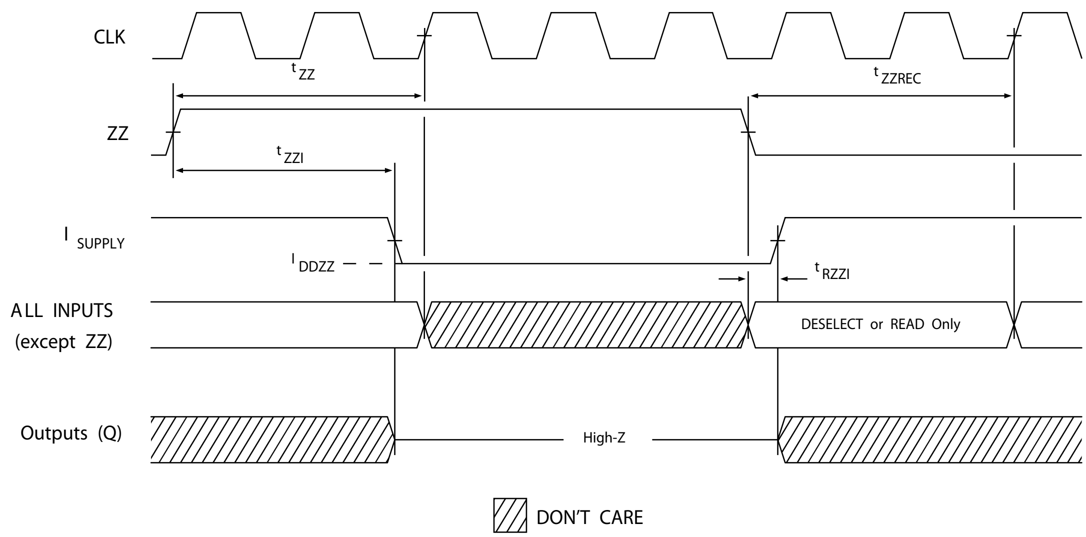


Figure 8 shows ZZ Mode timing waveform.[23, 24]

Figure 8. ZZ Mode Timing



Notes
22. The IGNORE CLOCK EDGE or STALL cycle (Clock 3) illustrated CEN being used to create a pause. A write is not performed during this cycle.
23. Device must be deselected when entering ZZ mode. See "Truth Table" on page 10 for all possible signal conditions to deselect the device.
24. IOs are in High-Z when exiting ZZ sleep mode.

Ordering Information

Not all of the speed, package and temperature ranges are available. Please contact your local sales representative or visit www.cypress.com for actual products offered.

Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
167	CY7C1470BV25-167AXC	51-85050	100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Commercial
	CY7C1472BV25-167AXC			
	CY7C1470BV25-167BZC	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm)	
	CY7C1472BV25-167BZC			
	CY7C1470BV25-167BZXC	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1472BV25-167BZXC			
	CY7C1474BV25-167BGC	51-85167	209-ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm)	
	CY7C1474BV25-167BGXC		209-ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm) Pb-Free	
	CY7C1470BV25-167AXI	51-85050	100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Industrial
	CY7C1472BV25-167AXI			
	CY7C1470BV25-167BZI	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm)	
	CY7C1472BV25-167BZI			
	CY7C1470BV25-167BZXI	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1472BV25-167BZXI			
	CY7C1474BV25-167BGI	51-85167	209-ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm)	
	CY7C1474BV25-167BGXI		209-ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm) Pb-Free	
200	CY7C1470BV25-200AXC	51-85050	100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Commercial
	CY7C1472BV25-200AXC			
	CY7C1470BV25-200BZC	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm)	
	CY7C1472BV25-200BZC			
	CY7C1470BV25-200BZXC	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1472BV25-200BZXC			
	CY7C1474BV25-200BGC	51-85167	209-ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm)	
	CY7C1474BV25-200BGXC		209-ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm) Pb-Free	
	CY7C1470BV25-200AXI	51-85050	100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Industrial
	CY7C1472BV25-200AXI			
	CY7C1470BV25-200BZI	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm)	
	CY7C1472BV25-200BZI			
	CY7C1470BV25-200BZXI	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1472BV25-200BZXI			
	CY7C1474BV25-200BGI	51-85167	209-ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm)	
	CY7C1474BV25-200BGXI		209-ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm) Pb-Free	

[+] Feedback

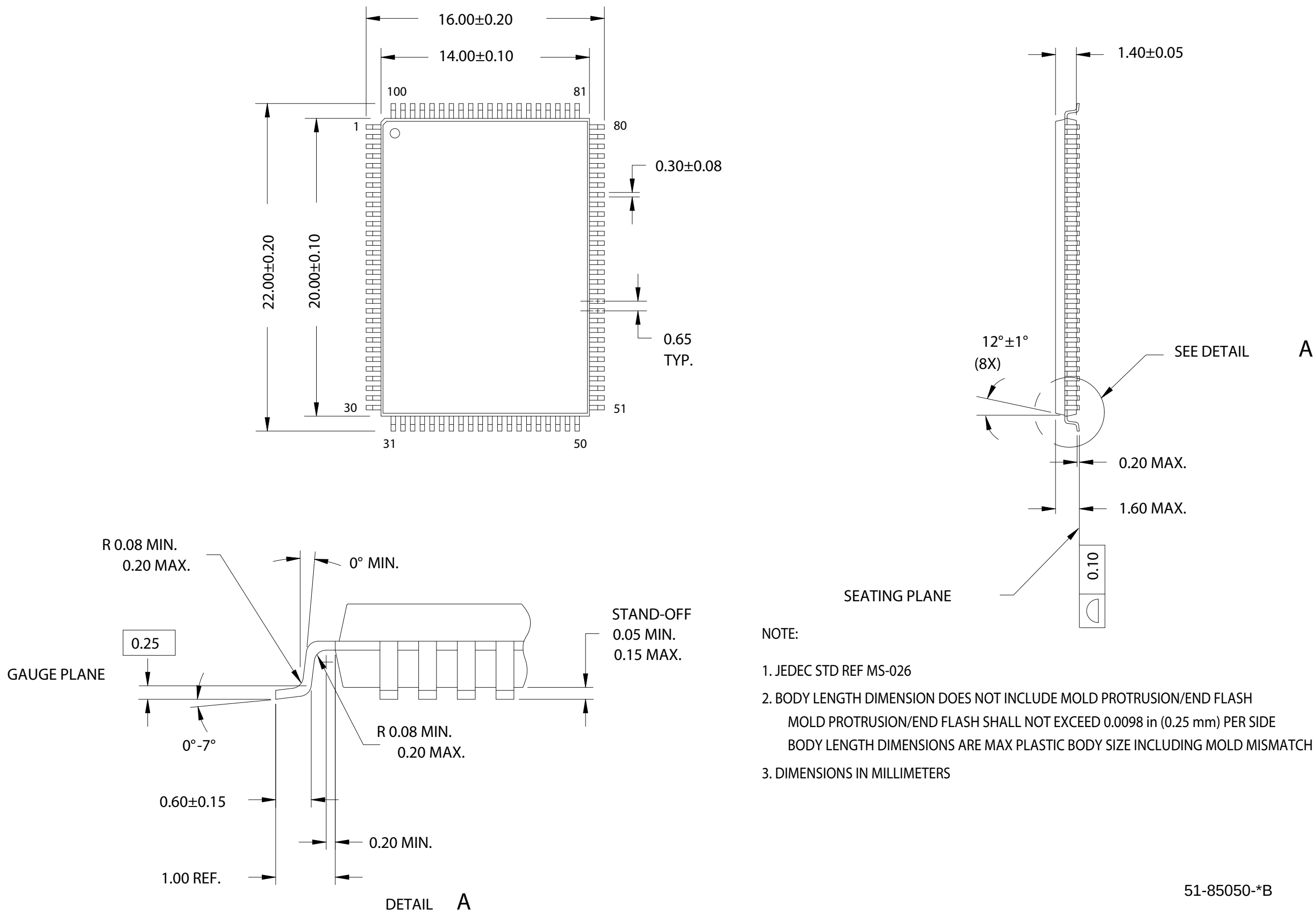
Ordering Information (continued)

Not all of the speed, package and temperature ranges are available. Please contact your local sales representative or visit www.cypress.com for actual products offered.

Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
250	CY7C1470BV25-250AXC	51-85050	100-pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Commercial
	CY7C1472BV25-250AXC			
	CY7C1470BV25-250BZC	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm)	
	CY7C1472BV25-250BZC			
	CY7C1470BV25-250BZXC	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1472BV25-250BZXC			
	CY7C1474BV25-250BGC	51-85167	209-ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm)	
	CY7C1474BV25-250BGXC		209-ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm) Pb-Free	
	CY7C1470BV25-250AXI	51-85050	100-Pin Thin Quad Flat Pack (14 x 20 x 1.4 mm) Pb-Free	Industrial
	CY7C1472BV25-250AXI			
	CY7C1470BV25-250BZI	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm)	
	CY7C1472BV25-250BZI			
	CY7C1470BV25-250BZXI	51-85165	165-ball Fine-Pitch Ball Grid Array (15 x 17 x 1.4 mm) Pb-Free	
	CY7C1472BV25-250BZXI			
	CY7C1474BV25-250BGI	51-85167	209-ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm)	
	CY7C1474BV25-250BGXI		209-ball Fine-Pitch Ball Grid Array (14 × 22 × 1.76 mm) Pb-Free	

Package Diagrams

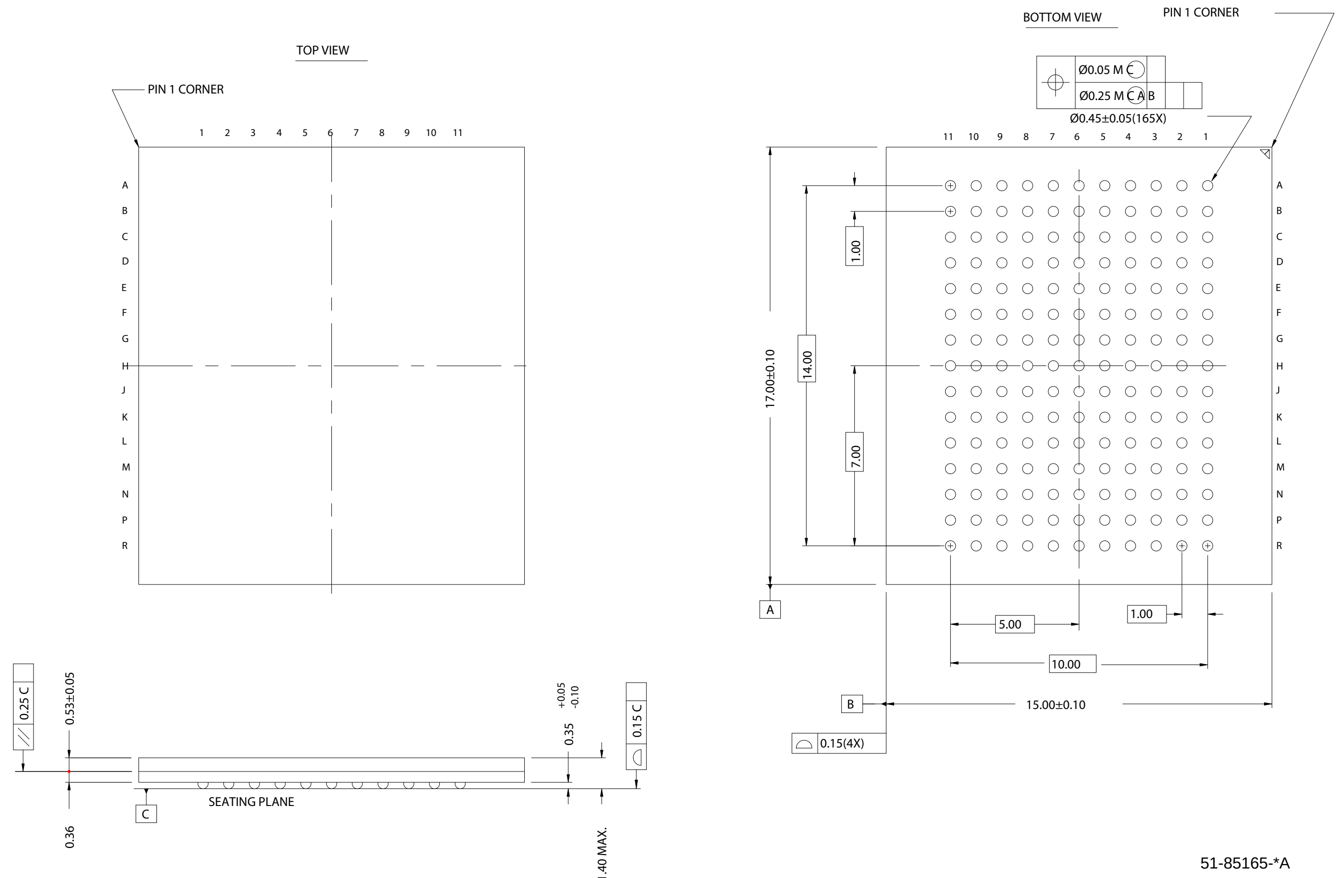
Figure 9. 100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm), 51-85050



[+] Feedback

Package Diagrams (continued)

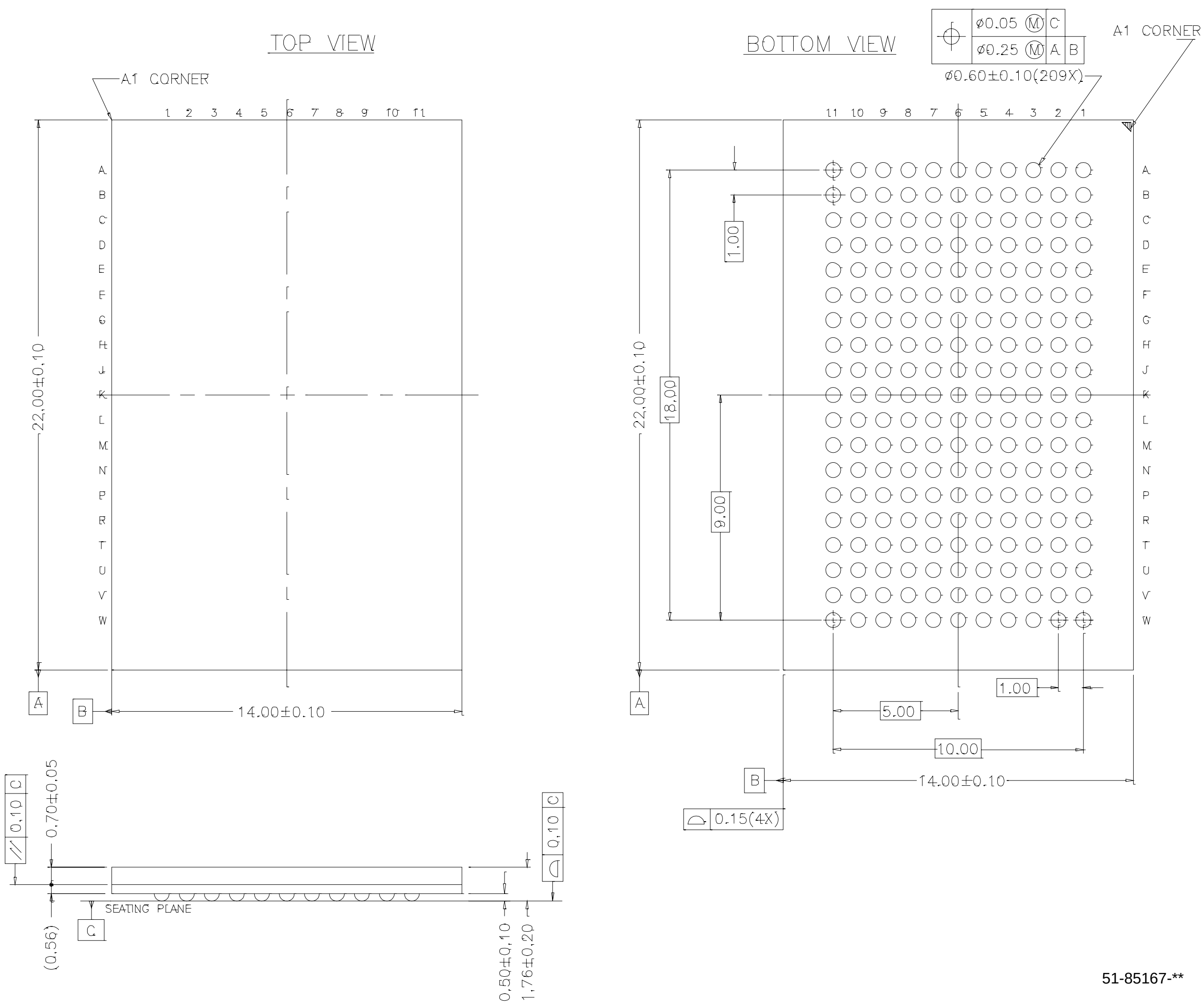
Figure 10. 165-Ball FBGA (15 x 17 x 1.4 mm), 51-85165



[+] Feedback

Package Diagrams (continued)

Figure 11. 209-Ball FBGA (14 x 22 x 1.76 mm), 51-85167



Document History Page

Document Title: CY7C1470BV25/CY7C1472BV25/CY7C1474BV25, 72-Mbit (2M x 36/4M x 18/1M x 72) Pipelined SRAM with NoBL™ Architecture Document Number: 001-15032				
REV.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	1032642	See ECN	VKN/KKVTMP	New data sheet
*A	1562503	See ECN	VKN/AESA	Removed 1.8V IO offering from the data sheet
*B	1897447	See ECN	VKN/AESA	Added footnote 14 related to IDD
*C	2082487	See ECN	VKN	Converted from preliminary to final
*D	2159486	See ECN	VKN/PYRS	Minor Change-Moved to the external web