

36-Mbit (1 M × 36/2 M × 18/512 K × 72) Flow-Through SRAM with NoBL™ Architecture

Features

- No Bus Latency™ (NoBL™) architecture eliminates dead cycles between write and read cycles
- Supports up to 133 MHz bus operations with zero wait states
 - Data is transferred on every clock
- Pin compatible and functionally equivalent to ZBT™ devices
- Internally self timed output buffer control to eliminate the need to use OE
- Registered inputs for flow through operation
- Byte write capability
- 3.3 V and 2.5 V IO power supply
- Fast clock-to-output times
 - 6.5 ns (for 133 MHz device)
- Clock Enable (\overline{CEN}) pin to enable clock and suspend operation
- Synchronous self timed writes
- Asynchronous Output Enable
- CY7C1461AV33, CY7C1463AV33 available in JEDEC-standard Pb-free 100-pin TQFP package, Pb-free and non Pb-free 165-ball FBGA package. CY7C1465AV33 available in Pb-free and non-Pb-free 209-ball FBGA package
- Three chip enables for simple depth expansion
- Automatic power down feature available using ZZ mode or CE deselect
- IEEE 1149.1 JTAG-compatible boundary scan
- Burst capability — linear or interleaved burst order
- Low standby power

Selection Guide

	133 MHz	100 MHz	Unit
Maximum Access Time	6.5	8.5	ns
Maximum Operating Current	310	290	mA
Maximum CMOS Standby Current	120	120	mA

Functional Description

The CY7C1461AV33/CY7C1463AV33/CY7C1465AV33^[1] are 3.3 V, 1 M × 36/2 M × 18/512 K × 72 Synchronous Flow-Through Burst SRAMs designed specifically to support unlimited true back-to-back read and write operations without the insertion of wait states. The CY7C1461AV33/CY7C1463AV33/CY7C1465AV33 is equipped with the advanced NoBL logic required to enable consecutive read and write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data through the SRAM, especially in systems that require frequent write-read transitions.

All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock input is qualified by the Clock Enable (\overline{CEN}) signal, which when deasserted suspends operation and extends the previous clock cycle. Maximum access delay from the clock rise is 6.5 ns (133 MHz device).

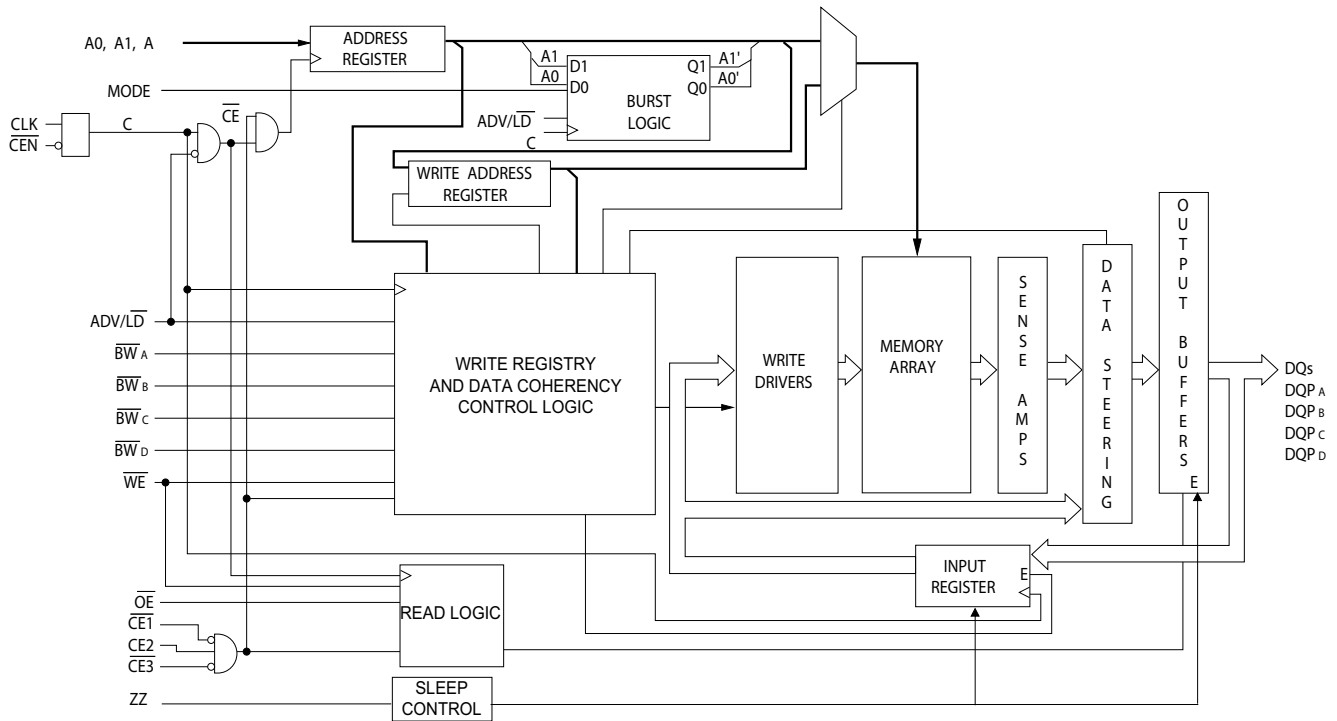
Write operations are controlled by the two or four Byte Write Select (\overline{BW}_x) and a Write Enable (\overline{WE}) input. All writes are conducted with on-chip synchronous self timed write circuitry.

Three synchronous Chip Enables (\overline{CE}_1 , \overline{CE}_2 , \overline{CE}_3) and an asynchronous Output Enable (\overline{OE}) provide for easy bank selection and output tri-state control. To avoid bus contention, the output drivers are synchronously tri-stated during the data portion of a write sequence.

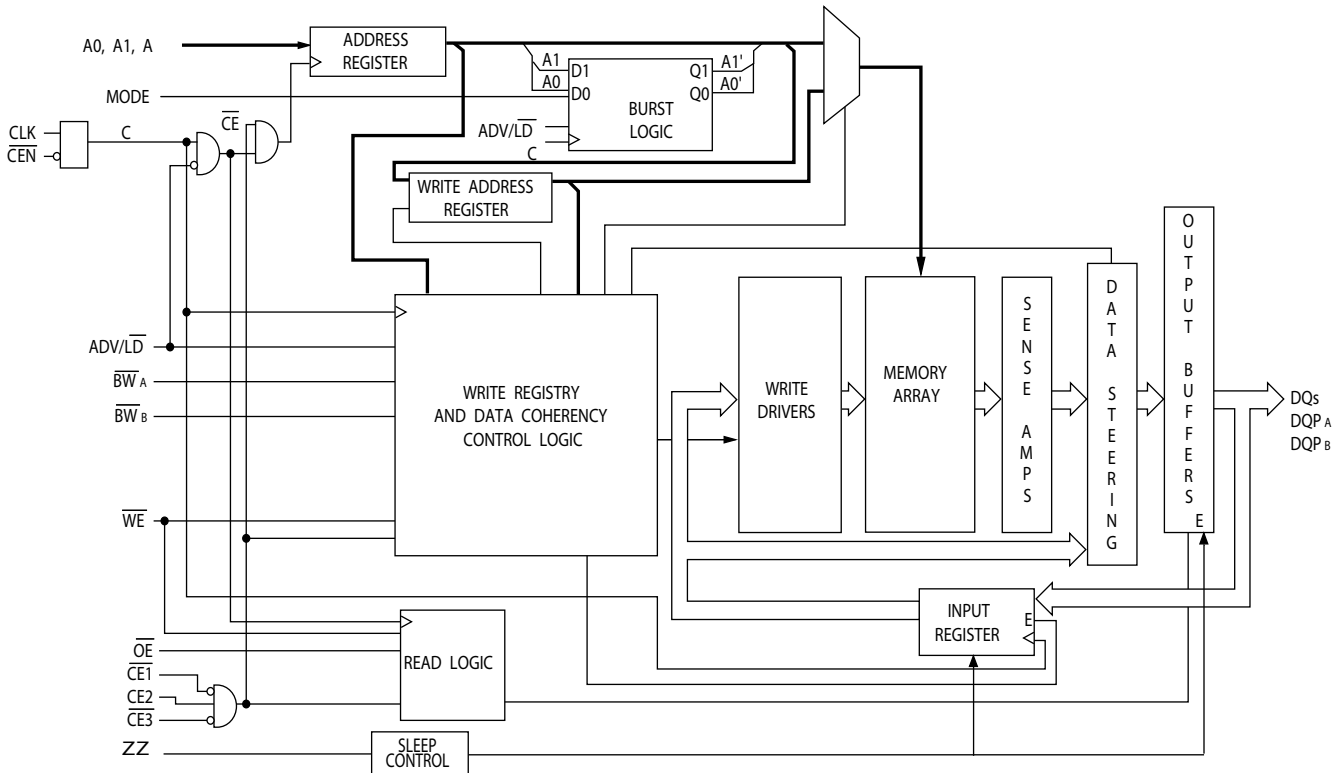
Note

1. For best practices recommendations, refer to the Cypress application note *System Design Guidelines* on www.cypress.com.

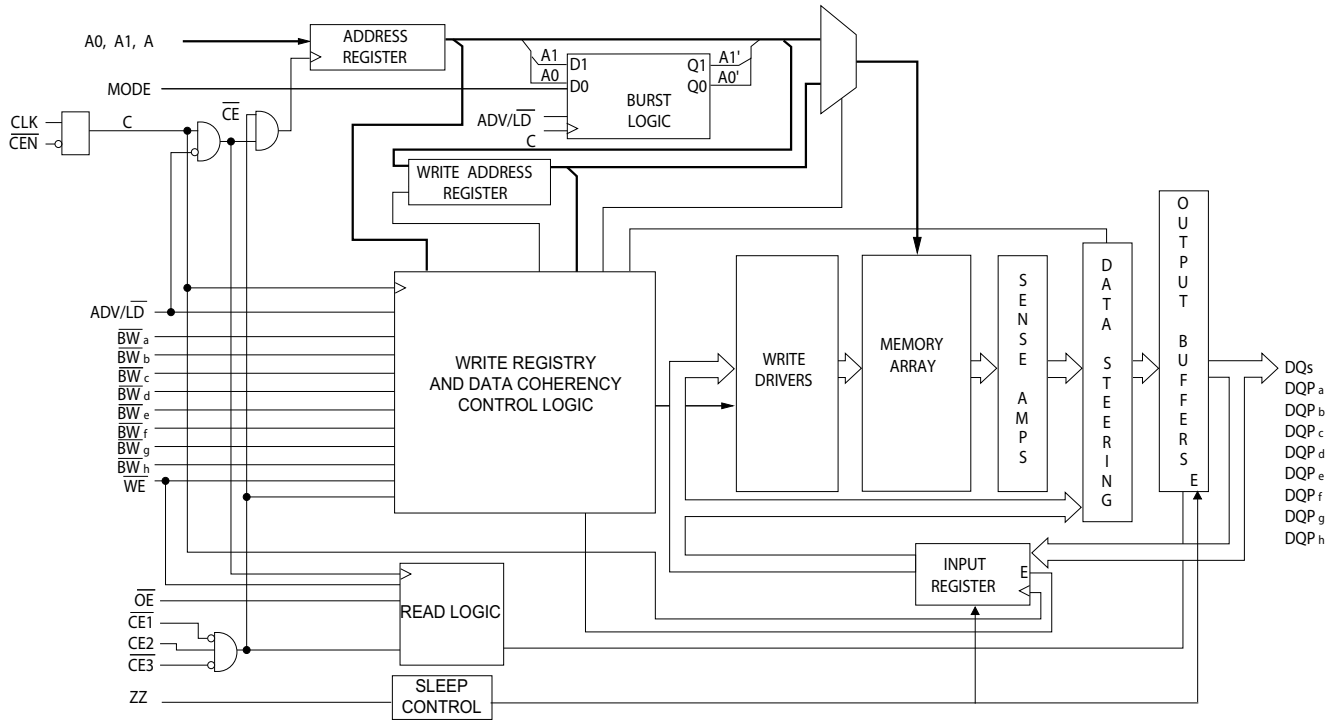
Logic Block Diagram – CY7C1461AV33 (1 M × 36)



Logic Block Diagram – CY7C1463AV33 (2 M × 18)



Logic Block Diagram – CY7C1465AV33 (512 K × 72)

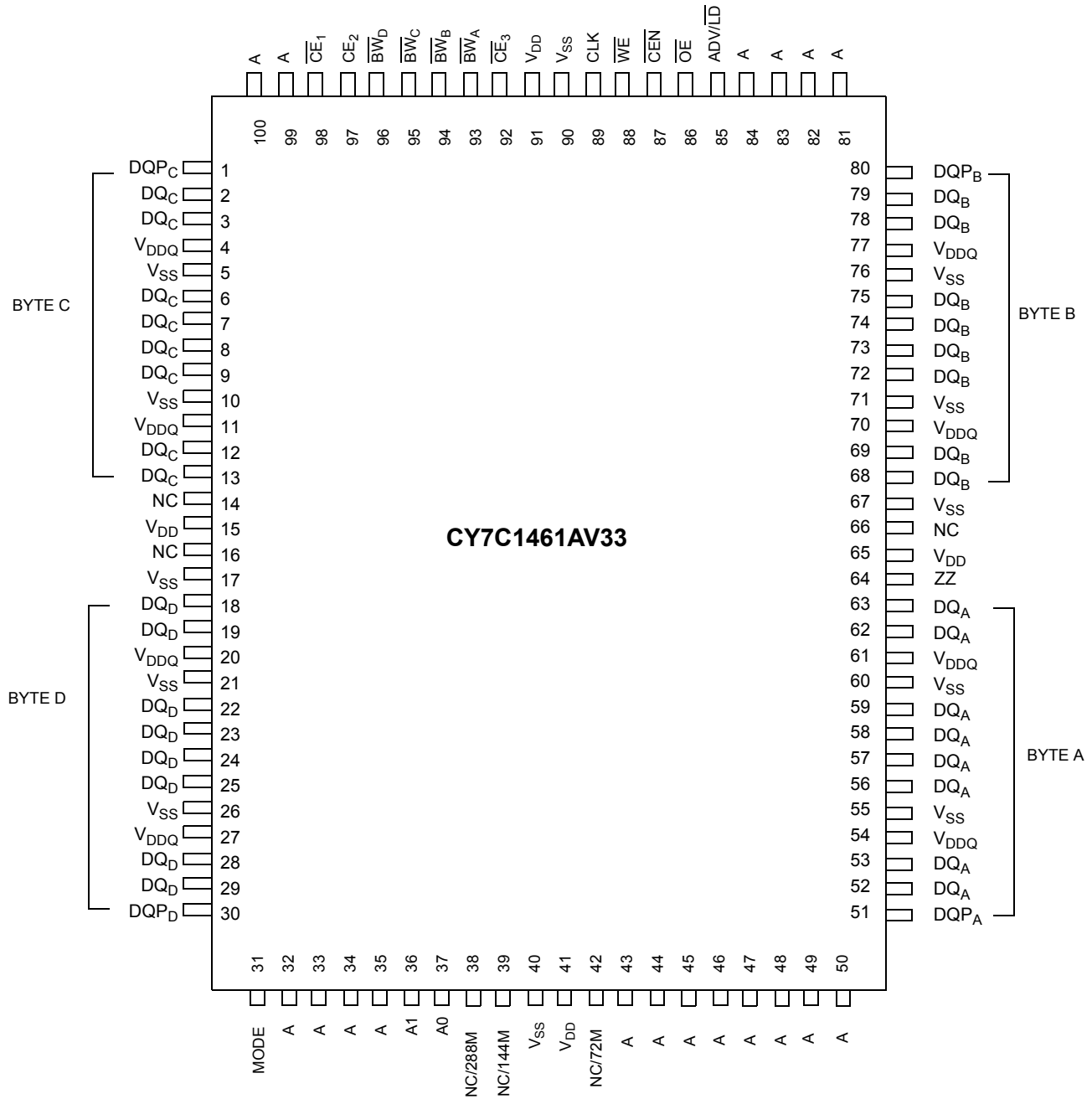


Contents

Pin Configurations	5	3.3 V TAP AC Test Conditions	18
Pin Definitions	9	3.3 V TAP AC Output Load Equivalent	18
Functional Overview	10	2.5 V TAP AC Test Conditions	18
Single Read Accesses	10	2.5 V TAP AC Output Load Equivalent	18
Burst Read Accesses	10	TAP DC Electrical Characteristics and	
Single Write Accesses	11	Operating Conditions	18
Burst Write Accesses	11	Identification Register Definitions	19
Interleaved Burst Address Table		Scan Register Sizes	19
(MODE = Floating or VDD)	11	Identification Codes	19
Linear Burst Address Table (MODE = GND)	11	165-ball FBGA Boundary Scan Order	20
Sleep Mode	11	209-ball FBGA Boundary Scan Order	21
ZZ Mode Electrical Characteristics	11	Maximum Ratings	22
Truth Table	12	Operating Range	22
Truth Table for Read/Write	13	Electrical Characteristics	22
Truth Table for Read/Write	13	Capacitance	23
Truth Table for Read/Write	13	Thermal Resistance	23
IEEE 1149.1 Serial Boundary Scan (JTAG)	14	Switching Characteristics	24
Disabling the JTAG Feature	14	Switching Waveforms	25
TAP Controller State Diagram	14	Ordering Information	28
Test Access Port (TAP)	14	Ordering Code Definitions	28
TAP Controller Block Diagram	14	Package Diagrams	29
PERFORMING A TAP RESET	14	Document History Page	32
TAP REGISTERS	14	Sales, Solutions, and Legal Information	34
TAP Instruction Set	15	Worldwide Sales and Design Support	34
TAP Timing	16	Products	34
TAP AC Switching Characteristics	17	PSoC Solutions	34

Pin Configurations

100-pin TQFP Pinout



Pin Configurations (continued)

165-ball FBGA (15 × 17 × 1.4 mm) Pinout

CY7C1461AV33 (1 M × 36)

	1	2	3	4	5	6	7	8	9	10	11
A	NC/576M	A	\overline{CE}_1	\overline{BW}_C	\overline{BW}_B	\overline{CE}_3	\overline{CEN}	ADV/LD	A	A	NC
B	NC/1G	A	CE2	\overline{BW}_D	\overline{BW}_A	CLK	\overline{WE}	\overline{OE}	A	A	NC
C	DQ _C	NC	V _{DDQ}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{DDQ}	NC	DQ _P _B
D	DQ _C	DQ _C	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQ _B	DQ _B
E	DQ _C	DQ _C	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQ _B	DQ _B
F	DQ _C	DQ _C	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQ _B	DQ _B
G	DQ _C	DQ _C	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQ _B	DQ _B
H	NC	NC	NC	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	NC	NC	ZZ
J	DQ _D	DQ _D	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQ _A	DQ _A
K	DQ _D	DQ _D	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQ _A	DQ _A
L	DQ _D	DQ _D	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQ _A	DQ _A
M	DQ _D	DQ _D	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQ _A	DQ _A
N	DQ _P _D	NC	V _{DDQ}	V _{SS}	NC	NC	NC	V _{SS}	V _{DDQ}	NC	DQ _P _A
P	NC/144M	NC/72M	A	A	TDI	A1	TDO	A	A	A	NC/288M
R	MODE	A	A	A	TMS	A0	TCK	A	A	A	A

CY7C1463AV33 (2 M × 18)

	1	2	3	4	5	6	7	8	9	10	11
A	NC/576M	A	\overline{CE}_1	\overline{BW}_B	NC	\overline{CE}_3	\overline{CEN}	ADV/LD	A	A	A
B	NC/1G	A	CE2	NC	\overline{BW}_A	CLK	\overline{WE}	\overline{OE}	A	A	NC
C	NC	NC	V _{DDQ}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{DDQ}	NC	DQ _P _A
D	NC	DQ _B	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	NC	DQ _A
E	NC	DQ _B	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	NC	DQ _A
F	NC	DQ _B	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	NC	DQ _A
G	NC	DQ _B	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	NC	DQ _A
H	NC	NC	NC	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	NC	NC	ZZ
J	DQ _B	NC	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQ _A	NC
K	DQ _B	NC	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQ _A	NC
L	DQ _B	NC	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQ _A	NC
M	DQ _B	NC	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQ _A	NC
N	DQ _P _B	NC	V _{DDQ}	V _{SS}	NC	NC	NC	V _{SS}	V _{DDQ}	NC	NC
P	NC/144M	NC/72M	A	A	TDI	A1	TDO	A	A	A	NC/288M
R	MODE	A	A	A	TMS	A0	TCK	A	A	A	A

Pin Configurations (continued)

209-ball FBGA (14 × 22 × 1.76 mm) Pinout

CY7C1465AV33 (512 K × 72)

	1	2	3	4	5	6	7	8	9	10	11
A	DQg	DQg	A	CE ₂	A	ADV/LD	A	\overline{CE}_3	A	DQb	DQb
B	DQg	DQg	\overline{BWS}_c	\overline{BWS}_g	NC	\overline{WE}	A	\overline{BWS}_b	\overline{BWS}_f	DQb	DQb
C	DQg	DQg	\overline{BWS}_h	\overline{BWS}_d	NC/576M	\overline{CE}_1	NC	\overline{BWS}_e	\overline{BWS}_a	DQb	DQb
D	DQg	DQg	V _{SS}	NC	NC/1G	\overline{OE}	NC	NC	V _{SS}	DQb	DQb
E	DQPg	DQPc	V _{DDQ}	V _{DDQ}	V _{DD}	V _{DD}	V _{DD}	V _{DDQ}	V _{DDQ}	DQPf	DQPb
F	DQc	DQc	V _{SS}	V _{SS}	V _{SS}	NC	V _{SS}	V _{SS}	V _{SS}	DQf	DQf
G	DQc	DQc	V _{DDQ}	V _{DDQ}	V _{DD}	NC	V _{DD}	V _{DDQ}	V _{DDQ}	DQf	DQf
H	DQc	DQc	V _{SS}	V _{SS}	V _{SS}	NC	V _{SS}	V _{SS}	V _{SS}	DQf	DQf
J	DQc	DQc	V _{DDQ}	V _{DDQ}	V _{DD}	NC	V _{DD}	V _{DDQ}	V _{DDQ}	DQf	DQf
K	NC	NC	CLK	NC	V _{SS}	\overline{CEN}	V _{SS}	NC	NC	NC	NC
L	DQh	DQh	V _{DDQ}	V _{DDQ}	V _{DD}	NC	V _{DD}	V _{DDQ}	V _{DDQ}	DQa	DQa
M	DQh	DQh	V _{SS}	V _{SS}	V _{SS}	NC	V _{SS}	V _{SS}	V _{SS}	DQa	DQa
N	DQh	DQh	V _{DDQ}	V _{DDQ}	V _{DD}	NC	V _{DD}	V _{DDQ}	V _{DDQ}	DQa	DQa
P	DQh	DQh	V _{SS}	V _{SS}	V _{SS}	ZZ	V _{SS}	V _{SS}	V _{SS}	DQa	DQa
R	DQPd	DQPh	V _{DDQ}	V _{DDQ}	V _{DD}	V _{DD}	V _{DD}	V _{DDQ}	V _{DDQ}	DQPa	DQPe
T	DQd	DQd	V _{SS}	NC	NC	MODE	NC	NC	V _{SS}	DQe	DQe
U	DQd	DQd	NC/144M	A	NC/72M	A	A	A	NC/288M	DQe	DQe
V	DQd	DQd	A	A	A	A1	A	A	A	DQe	DQe
W	DQd	DQd	TMS	TDI	A	A0	A	TDO	TCK	DQe	DQe

Pin Definitions

Pin Name	IO	Description
A ₀ , A ₁ , A	Input-Synchronous	Address Inputs. Used to select one of the address locations. Sampled at the rising edge of the CLK. A _[1:0] are fed to the two-bit burst counter.
\overline{BW}_A , \overline{BW}_B , \overline{BW}_C , \overline{BW}_D , \overline{BW}_E , \overline{BW}_F , \overline{BW}_G , \overline{BW}_H	Input-Synchronous	Byte Write Inputs, Active LOW. Qualified with \overline{WE} to conduct writes to the SRAM. Sampled on the rising edge of CLK.
\overline{WE}	Input-Synchronous	Write Enable Input, Active LOW. Sampled on the rising edge of CLK if \overline{CEN} is active LOW. This signal must be asserted LOW to initiate a write sequence.
ADV/LD	Input-Synchronous	Advance or Load Input. Used to advance the on-chip address counter or load a new address. When HIGH (and \overline{CEN} is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After deselecting, drive ADV/LD LOW to load a new address.
CLK	Input-Clock	Clock Input. Used to capture all synchronous inputs to the device. CLK is qualified with \overline{CEN} . CLK is only recognized if \overline{CEN} is active LOW.
\overline{CE}_1	Input-Synchronous	Chip Enable 1 Input, Active LOW. Sampled on the rising edge of CLK. Used in conjunction with \overline{CE}_2 and \overline{CE}_3 to select or deselect the device.
\overline{CE}_2	Input-Synchronous	Chip Enable 2 Input, Active HIGH. Sampled on the rising edge of CLK. Used in conjunction with \overline{CE}_1 and \overline{CE}_3 to select or deselect the device.
\overline{CE}_3	Input-Synchronous	Chip Enable 3 Input, Active LOW. Sampled on the rising edge of CLK. Used in conjunction with \overline{CE}_1 and \overline{CE}_2 to select or deselect the device.
\overline{OE}	Input-Asynchronous	Output Enable, Asynchronous Input, Active LOW. Combined with the synchronous logic block inside the device to control the direction of the IO pins. When LOW, the IO pins are allowed to behave as outputs. When deasserted HIGH, IO pins are tri-stated and act as input data pins. OE is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected.
\overline{CEN}	Input-Synchronous	Clock Enable Input, Active LOW. When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the clock signal is masked. Because deasserting \overline{CEN} does not deselect the device, use \overline{CEN} to extend the previous cycle when required.
ZZ	Input-Asynchronous	ZZ "Sleep" Input. This active HIGH input places the device in a non time critical sleep condition with data integrity preserved. During normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull down.
DQ _s	IO-Synchronous	Bidirectional Data IO lines. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by \overline{OE} . When \overline{OE} is asserted LOW, the pins behave as outputs. When HIGH, DQ _s and DQP _[A:D] are placed in a tri-state condition. The outputs are automatically tri-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of \overline{OE} .
DQP _x	IO-Synchronous	Bidirectional Data Parity IO Lines. Functionally, these signals are identical to DQ _s . During write sequences, DQP _x is controlled by \overline{BW}_x correspondingly.
MODE	Input Strap Pin	Mode Input. Selects the burst order of the device. When tied to Gnd selects linear burst sequence. When tied to V _{DD} or left floating selects interleaved burst sequence.
V _{DD}	Power Supply	Power Supply Inputs to the Core of the Device.
V _{DDQ}	IO Power Supply	Power Supply for IO Circuitry.
V _{SS}	Ground	Ground for the Device.

Pin Definitions (continued)

Pin Name	IO	Description
TDO	JTAG Serial Output Synchronous	Serial Data-Out to the JTAG Circuit. Delivers data on the negative edge of TCK. If the JTAG feature is not used, leave this pin unconnected. This pin is not available on TQFP packages.
TDI	JTAG Serial Input Synchronous	Serial Data-In to the JTAG Circuit. Sampled on the rising edge of TCK. If the JTAG feature is not used, this pin can be left floating or connected to V_{DD} through a pull up resistor. This pin is not available on TQFP packages.
TMS	JTAG Serial Input Synchronous	Serial Data-In to the JTAG Circuit. Sampled on the rising edge of TCK. If the JTAG feature is not used, this pin can be disconnected or connected to V_{DD} . This pin is not available on TQFP packages.
TCK	JTAG-Clock	Clock Input to the JTAG Circuitry. If the JTAG feature is not used, this pin must be connected to V_{SS} . This pin is not available on TQFP packages.
NC	N/A	No Connects. Not internally connected to the die.
NC/72M	N/A	Not Connected to the Die. Can be tied to any voltage level.
NC/144M	N/A	Not Connected to the Die. Can be tied to any voltage level.
NC/288M	N/A	Not Connected to the Die. Can be tied to any voltage level.
NC/576M	N/A	Not Connected to the Die. Can be tied to any voltage level.
NC/1G	N/A	Not Connected to the Die. Can be tied to any voltage level.

Functional Overview

The CY7C1461AV33/CY7C1463AV33/CY7C1465AV33 is a synchronous flow through burst SRAM designed specifically to eliminate wait states during Write-Read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the clock enable input signal (\overline{CEN}). If \overline{CEN} is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with \overline{CEN} . Maximum access delay from the clock rise (t_{CDV}) is 6.5 ns (133 MHz device).

Accesses can be initiated by asserting all three chip enables (\overline{CE}_1 , \overline{CE}_2 , \overline{CE}_3) active at the rising edge of the clock. If \overline{CEN} is active LOW and $\overline{ADV/LD}$ is asserted LOW, the address presented to the device is latched. The access can either be a read or write operation, depending on the status of the write enable (\overline{WE}). \overline{BW}_X can be used to conduct byte write operations.

Write operations are qualified by the Write Enable (\overline{WE}). All writes are simplified with on-chip synchronous self timed write circuitry.

Three synchronous chip enables (\overline{CE}_1 , \overline{CE}_2 , \overline{CE}_3) and an asynchronous output enable (\overline{OE}) simplify depth expansion. All operations (reads, writes, and deselections) are pipelined. $\overline{ADV/LD}$ must be driven LOW after the device is deselected to load a new address for the next operation.

Single Read Accesses

A read access is initiated when these conditions are satisfied at clock rise:

- \overline{CEN} is asserted LOW

- \overline{CE}_1 , \overline{CE}_2 , and \overline{CE}_3 are ALL asserted active

- The write enable input signal \overline{WE} is deasserted HIGH

- $\overline{ADV/LD}$ is asserted LOW

The address presented to the address inputs is latched into the address register and presented to the memory array and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the output buffers. The data is available within 6.5 ns (133 MHz device) provided \overline{OE} is active LOW. After the first clock of the read access, the output buffers are controlled by \overline{OE} and the internal control logic. \overline{OE} must be driven LOW for the device to drive out the requested data. On the subsequent clock, another operation (Read/Write/Deselect) can be initiated. When the SRAM is deselected at clock rise by one of the chip enable signals, its output is tri-stated immediately.

Burst Read Accesses

The CY7C1461AV33/CY7C1463AV33/CY7C1465AV33 has an on-chip burst counter that provides the ability to supply a single address and conduct up to four reads without reasserting the address inputs. $\overline{ADV/LD}$ must be driven LOW to load a new address into the SRAM, as described in the [Single Read Accesses](#) section. The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and wraps around when incremented sufficiently. A HIGH input on $\overline{ADV/LD}$ increments the internal burst counter regardless of the state of chip enable inputs or \overline{WE} . \overline{WE} is latched at the beginning of a burst cycle. Therefore, the type of access (read or write) is maintained throughout the burst sequence.

Single Write Accesses

Write access are initiated when the following conditions are satisfied at clock rise: (1) \overline{CEN} is asserted LOW, (2) \overline{CE}_1 , \overline{CE}_2 , and \overline{CE}_3 are ALL asserted active, and (3) the write signal \overline{WE} is asserted LOW. The address presented to the address bus is loaded into the address register. The write signals are latched into the control logic block. The data lines are automatically tri-stated regardless of the state of the \overline{OE} input signal. This allows the external logic to present the data on DQs and DQP_X .

On the next clock rise the data presented to DQs and DQP_X (or a subset for byte write operations, see [Truth Table](#) for details) inputs is latched into the device and the write is complete. Additional accesses (read/write/deselect) can be initiated on this cycle.

The data written during the write operation is controlled by \overline{BW}_X signals. The CY7C1461AV33/CY7C1463AV33/CY7C1465AV33 provides byte write capability that is described in the truth table. Asserting the (\overline{WE}) with the selected byte write select input selectively writes to only the desired bytes. Bytes not selected during a byte write operation remains unaltered. A synchronous self timed write mechanism is provided to simplify the write operations. Byte write capability is included to greatly simplify Read/Modify/Write sequences, which can be reduced to simple byte write operations.

Because the CY7C1461AV33/CY7C1463AV33/CY7C1465AV33 is a common IO device, data must not be driven into the device when the outputs are active. The \overline{OE} can be deasserted HIGH before presenting data to the DQs and DQP_X inputs. This tri-states the output drivers. As a safety precaution, DQs and DQP_X are automatically tri-stated during the data portion of a write cycle, regardless of the state of \overline{OE} .

Burst Write Accesses

The CY7C1461AV33/CY7C1463AV33/CY7C1465AV33 has an on-chip burst counter that provides the ability to supply a single address and conduct up to four write operations without reasserting the address inputs. $\overline{ADV/LD}$ must be driven LOW to load the initial address, as described in the [Single Write Accesses](#) section. When $\overline{ADV/LD}$ is driven HIGH on the

subsequent clock rise, the chip enables (\overline{CE}_1 , \overline{CE}_2 , and \overline{CE}_3) and \overline{WE} inputs are ignored and the burst counter is incremented. The correct \overline{BW}_X inputs must be driven in each cycle of the burst write, to write the correct bytes of data.

Interleaved Burst Address Table (MODE = Floating or V_{DD})

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table (MODE = GND)

First Address A1: A0	Second Address A1: A0	Third Address A1: A0	Fourth Address A1: A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation sleep mode. Two clock cycles are required to enter into or exit from this sleep mode. When in this mode, data integrity is guaranteed. Accesses pending when entering the sleep mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the sleep mode. \overline{CE}_1 , \overline{CE}_2 , and \overline{CE}_3 , must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	$ZZ \geq V_{DD} - 0.2 V$	–	100	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2 V$	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2 V$	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit sleep current	This parameter is sampled	0	–	ns

Truth Table

The truth table for CY7C1461AV33/CY7C1463AV33/CY7C1465AV33 follows. [2, 3, 4, 5, 6, 7, 8]

Operation	Address Used	\overline{CE}_1	CE_2	\overline{CE}_3	ZZ	ADV/LD	\overline{WE}	\overline{BW}_x	\overline{OE}	\overline{CEN}	CLK	DQ
Deselect Cycle	None	H	X	X	L	L	X	X	X	L	L->H	Tri-State
Deselect Cycle	None	X	X	H	L	L	X	X	X	L	L->H	Tri-State
Deselect Cycle	None	X	L	X	L	L	X	X	X	L	L->H	Tri-State
Continue Deselect Cycle	None	X	X	X	L	H	X	X	X	L	L->H	Tri-State
Read Cycle (Begin Burst)	External	L	H	L	L	L	H	X	L	L	L->H	Data Out (Q)
Read Cycle (Continue Burst)	Next	X	X	X	L	H	X	X	L	L	L->H	Data Out (Q)
NOP/Dummy Read (Begin Burst)	External	L	H	L	L	L	H	X	H	L	L->H	Tri-State
Dummy Read (Continue Burst)	Next	X	X	X	L	H	X	X	H	L	L->H	Tri-State
Write Cycle (Begin Burst)	External	L	H	L	L	L	L	L	X	L	L->H	Data In (D)
Write Cycle (Continue Burst)	Next	X	X	X	L	H	X	L	X	L	L->H	Data In (D)
NOP/Write Abort (Begin Burst)	None	L	H	L	L	L	L	H	X	L	L->H	Tri-State
Write Abort (Continue Burst)	Next	X	X	X	L	H	X	H	X	L	L->H	Tri-State
Ignore Clock Edge (Stall)	Current	X	X	X	L	X	X	X	X	H	L->H	-
Sleep Mode	None	X	X	X	H	X	X	X	X	X	X	Tri-State

Notes

2. X = "Don't Care." H = logic HIGH, L = logic LOW. $\overline{BW}_x = L$ signifies at least one byte write select is active, $\overline{BW}_x = Valid$ signifies that the desired byte write selects are asserted, see truth table for details.
3. Write is defined by \overline{BW}_x and \overline{WE} . See truth table for read or write.
4. When a write cycle is detected, all IOs are tri-stated, even during byte writes.
5. The DQs and DQP_x pins are controlled by the current cycle and the \overline{OE} signal. \overline{OE} is asynchronous and is not sampled with the clock.
6. $CEN = H$, inserts wait states.
7. Device powers up deselected and the IOs in a tri-state condition, regardless of \overline{OE} .
8. \overline{OE} is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQs and $DQP_x = Tri-state$ when \overline{OE} is inactive or when the device is deselected, and DQs and $DQP_x = data$ when \overline{OE} is active.

Truth Table for Read/Write^[9, 10]

Function (CY7C1461AV33)	\overline{WE}	\overline{BW}_A	\overline{BW}_B	\overline{BW}_C	\overline{BW}_D
Read	H	X	X	X	X
Write – No Bytes Written	L	H	H	H	H
Write Byte A – (DQ _A and DQP _A)	L	L	H	H	H
Write Byte B – (DQ _B and DQP _B)	L	H	L	H	H
Write Byte C – (DQ _C and DQP _C)	L	H	H	L	H
Write Byte D – (DQ _D and DQP _D)	L	H	H	H	L
Write All Bytes	L	L	L	L	L

Truth Table for Read/Write^[9, 10]

Function (CY7C1463AV33)	\overline{WE}	\overline{BW}_b	\overline{BW}_a
Read	H	X	X
Write – No Bytes Written	L	H	H
Write Byte a – (DQ _a and DQP _a)	L	H	L
Write Byte b – (DQ _b and DQP _b)	L	L	H
Write Both Bytes	L	L	L

Truth Table for Read/Write^[9, 10]

Function (CY7C1465AV33)	\overline{WE}	\overline{BW}_x
Read	H	X
Write – No Bytes Written	L	H
Write Byte X – (DQ _x and DQP _x)	L	L
Write All Bytes	L	All $\overline{BW} = L$

Notes

9. X = "Don't Care." H = logic HIGH, L = logic LOW. $\overline{BW}_x = L$ signifies at least one byte write select is active, $\overline{BW}_x = \text{Valid}$ signifies that the desired byte write selects are asserted, see truth table for details.
10. Table only lists a partial listing of the byte write combinations. Any combination of \overline{BW}_x is valid. Appropriate write is done based on which byte write is active

IEEE 1149.1 Serial Boundary Scan (JTAG)

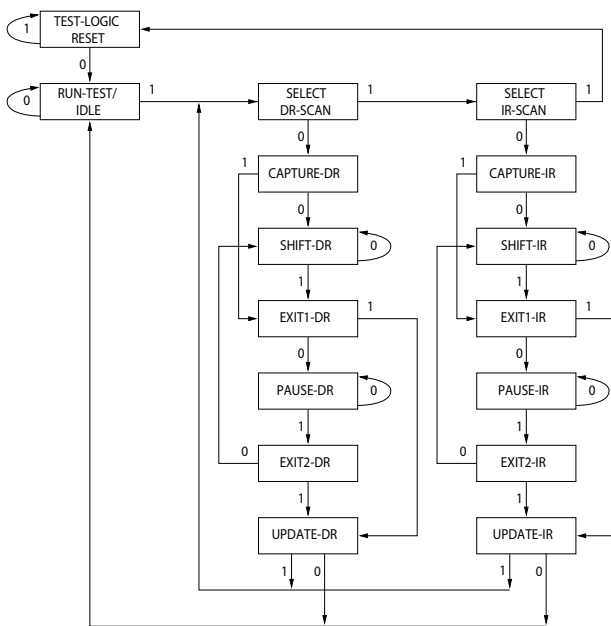
The CY7C1461AV33/CY7C1463AV33/CY7C1465AV33 incorporates a serial boundary scan test access port (TAP). This part is fully compliant with 1149.1. The TAP operates using JEDEC-standard 3.3 V and 2.5 V IO logic level.

The CY7C1461AV33/CY7C1463AV33/CY7C1465AV33 contains a TAP controller, instruction register, boundary scan register, bypass register, and ID register.

Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (V_{SS}) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to V_{DD} through a pull up resistor. TDO must be left unconnected. On power up, the device is up in a reset state which does not interfere with the operation of the device.

TAP Controller State Diagram



The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

Test Access Port (TAP)

Test Clock (TCK)

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this ball unconnected if the TAP is not used. The ball is pulled up internally, resulting in a logic HIGH level.

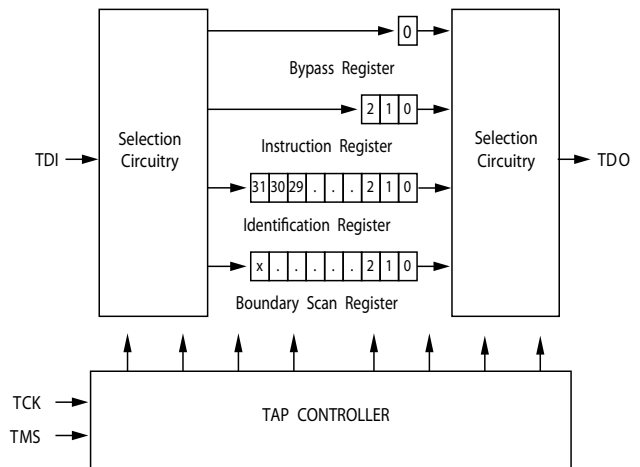
Test Data-In (TDI)

The TDI ball is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. TDI is internally pulled up and can be unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) of any register (see [TAP Controller Block Diagram](#)).

Test Data-Out (TDO)

The TDO output ball is used to serially clock data-out from the registers. The output is active depending on the current state of the TAP state machine. The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register (see [TAP Controller State Diagram](#)).

TAP Controller Block Diagram



Performing a TAP Reset

A RESET is performed by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power up, the TAP is reset internally to ensure that TDO comes up in a High Z state.

TAP Registers

Registers are connected between the TDI and TDO balls and enable data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI ball on the rising edge of TCK. Data is output on the TDO ball on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO balls as shown in the [TAP Controller Block Diagram](#). On power up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary “01” pattern to enable fault isolation of the board level serial test data path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO balls. This enables data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all the input and bidirectional balls on the SRAM. The length of the boundary scan register for the SRAM in different packages is listed in the [Scan Register Sizes](#) table.

The boundary scan register is loaded with the contents of the RAM IO ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO balls when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions can be used to capture the contents of the IO ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the [Identification Register Definitions](#) table.

TAP Instruction Set

Overview

Eight different instructions are possible with the three bit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are listed as RESERVED and must not be used. The other five instructions are described in the following section in detail.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO balls. To execute the instruction after it is shifted in, the TAP controller must be moved into the Update-IR state.

IDCODE

The IDCODE instruction causes a vendor specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO balls and enables the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state.

The IDCODE instruction is loaded into the instruction register on power up or whenever the TAP controller is supplied a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. The SAMPLE Z command puts the output bus into a High Z state until the next command is supplied during the Update IR state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

The TAP controller clock can only operate at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output undergoes a transition. The TAP may then try to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that is captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller’s capture setup plus hold times (t_{CS} and t_{CH}). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD enables an initial data pattern to be placed at the latched parallel outputs of the boundary scan register cells prior to the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases can occur concurrently when required—that is, while data captured is shifted out, the preloaded data can be shifted in.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

EXTEST

The EXTEST instruction enables the preloaded data to be driven out through the system output pins. This instruction also selects the boundary scan register to be connected for serial access between the TDI and TDO in the Shift-DR controller state.

EXTEST OUTPUT BUS TRI-STATE

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tri-state mode.

The boundary scan register has a special bit located at bit #89 (for 165-ball FBGA package) or bit #138 (for 209-ball FBGA package). When this scan cell, called the “extest output bus tri-state”, is latched into the preload register during the “Update-DR” state in the TAP controller, it directly controls the state of the output (Q-bus) pins when the EXTEST is entered as the current instruction. When HIGH, it enables the output buffers to drive the output bus. When LOW, this bit places the output bus into a High Z condition.

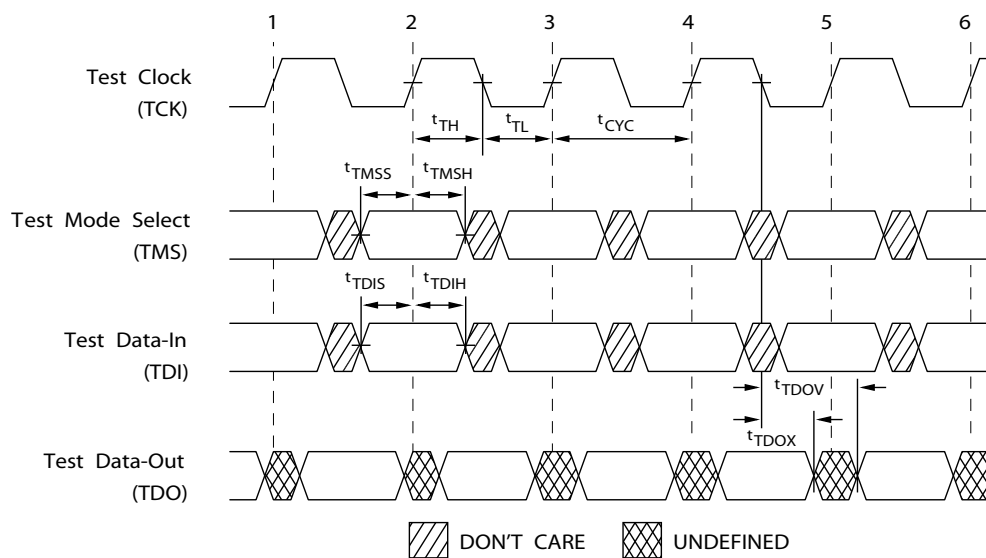
This bit can be set by entering the SAMPLE/PRELOAD or EXTEST command and then shifting the desired bit into that cell,

during the Shift-DR state. During Update-DR, the value loaded into that shift register cell latches into the preload register. When the EXTEST instruction is entered, this bit directly controls the output Q-bus pins. Note that this bit is pre-set HIGH to enable the output when the device is powered-up, and also when the TAP controller is in the Test-Logic-Reset state.

Reserved

These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP Timing



TAP AC Switching Characteristics

Over the Operating Range^[11, 12]

Parameter	Description	Min	Max	Unit
Clock				
t_{TCYC}	TCK Clock Cycle Time	50	–	ns
t_{TF}	TCK Clock Frequency	–	20	MHz
t_{TH}	TCK Clock HIGH time	20	–	ns
t_{TL}	TCK Clock LOW time	20	–	ns
Output Times				
t_{TDOV}	TCK Clock LOW to TDO Valid	–	10	ns
t_{TDOX}	TCK Clock LOW to TDO Invalid	0	–	ns
Setup Times				
t_{TMSS}	TMS Setup to TCK Clock Rise	5	–	ns
t_{TDIS}	TDI Setup to TCK Clock Rise	5	–	ns
t_{CS}	Capture Setup to TCK Rise	5	–	ns
Hold Times				
t_{TMSh}	TMS Hold after TCK Clock Rise	5	–	ns
t_{TDIH}	TDI Hold after Clock Rise	5	–	ns
t_{CH}	Capture Hold after Clock Rise	5	–	ns

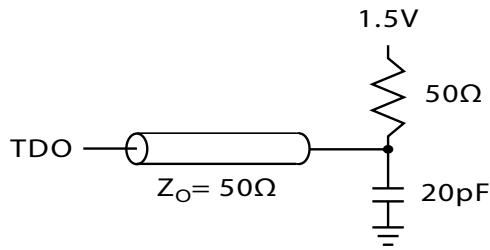
Notes

11. t_{CS} and t_{CH} refer to the setup and hold time requirements of latching data from the boundary scan register.
 12. Test conditions are specified using the load in TAP AC test Conditions. $t_R/t_F = 1$ ns.

3.3 V TAP AC Test Conditions

Input pulse levels V_{SS} to 3.3 V
 Input rise and fall times 1 ns
 Input timing reference levels 1.5 V
 Output reference levels 1.5 V
 Test load termination supply voltage 1.5 V

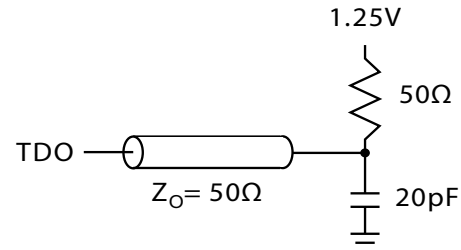
3.3 V TAP AC Output Load Equivalent



2.5 V TAP AC Test Conditions

Input pulse levels V_{SS} to 2.5 V
 Input rise and fall time 1 ns
 Input timing reference levels 1.25 V
 Output reference levels 1.25 V
 Test load termination supply voltage 1.25 V

2.5 V TAP AC Output Load Equivalent



TAP DC Electrical Characteristics and Operating Conditions

($0\text{ }^{\circ}\text{C} < T_A < +70\text{ }^{\circ}\text{C}$; $V_{DD} = 3.135$ to 3.6 V unless otherwise noted)^[13]

Parameter	Description	Test Conditions	Min	Max	Unit	
V _{OH1}	Output HIGH Voltage	I _{OH} = -4.0 mA, V _{DDQ} = 3.3 V	2.4	-	V	
		I _{OH} = -1.0 mA, V _{DDQ} = 2.5 V	2.0	-	V	
V _{OH2}	Output HIGH Voltage	I _{OH} = -100 μA	V _{DDQ} = 3.3 V	2.9	-	V
			V _{DDQ} = 2.5 V	2.1	-	V
V _{OL1}	Output LOW Voltage	I _{OL} = 8.0 mA	V _{DDQ} = 3.3 V	-	0.4	V
		I _{OL} = 1.0 mA	V _{DDQ} = 2.5 V	-	0.4	V
V _{OL2}	Output LOW Voltage	I _{OL} = 100 μA	V _{DDQ} = 3.3 V	-	0.2	V
			V _{DDQ} = 2.5 V	-	0.2	V
V _{IH}	Input HIGH Voltage		V _{DDQ} = 3.3 V	2.0	V _{DD} + 0.3	V
			V _{DDQ} = 2.5 V	1.7	V _{DD} + 0.3	V
V _{IL}	Input LOW Voltage		V _{DDQ} = 3.3 V	-0.3	0.8	V
			V _{DDQ} = 2.5 V	-0.3	0.7	V
I _X	Input Load Current	GND ≤ V _{IN} ≤ V _{DDQ}	-5	5	μA	

Note

13. All voltages referenced to V_{SS} (GND).

Identification Register Definitions

Instruction Field	CY7C1461AV33 (1 M × 36)	CY7C1463AV33 (2 M × 18)	CY7C1465AV33 (512 K × 72)	Description
Revision Number (31:29)	000	000	000	Describes the version number
Device Depth (28:24) ^[14]	01011	01011	01011	Reserved for internal use
Architecture and Memory Type (23:18)	001001	001001	001001	Defines memory type and architecture
Bus Width and Density(17:12)	100111	010111	110111	Defines width and density
Cypress JEDEC ID Code (11:1)	00000110100	00000110100	00000110100	Allows unique identification of SRAM vendor
ID Register Presence Indicator (0)	1	1	1	Indicates the presence of an ID register

Scan Register Sizes

Register Name	Bit Size (× 36)	Bit Size (× 18)	Bit Size (× 72)
Instruction	3	3	3
Bypass	1	1	1
ID	32	32	32
Boundary Scan Order (165-ball FBGA Package)	89	89	–
Boundary Scan Order (209-ball FBGA Package)	–	–	138

Identification Codes

Instruction	Code	Description
EXTEST	000	Captures IO ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM outputs to High Z state.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures IO ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures IO ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

Note

14. Bit #24 is "1" in the ID Register Definitions for both 2.5 V and 3.3 V versions of this device.

209-ball FBGA Boundary Scan Order ^[16]

CY7C1465AV33 (512 K × 72)

Bit#	Ball ID
1	W6
2	V6
3	U6
4	W7
5	V7
6	U7
7	T7
8	V8
9	U8
10	T8
11	V9
12	U9
13	P6
14	W11
15	W10
16	V11
17	V10
18	U11
19	U10
20	T11
21	T10
22	R11
23	R10
24	P11
25	P10
26	N11
27	N10
28	M11
29	M10
30	L11
31	L10
32	K11
33	M6
34	L6
35	J6

Bit#	Ball ID
36	F6
37	K8
38	K9
39	K10
40	J11
41	J10
42	H11
43	H10
44	G11
45	G10
46	F11
47	F10
48	E10
49	E11
50	D11
51	D10
52	C11
53	C10
54	B11
55	B10
56	A11
57	A10
58	C9
59	B9
60	A9
61	D8
62	C8
63	B8
64	A8
65	D7
66	C7
67	B7
68	A7
69	D6
70	G6

Bit#	Ball ID
71	H6
72	C6
73	B6
74	A6
75	A5
76	B5
77	C5
78	D5
79	D4
80	C4
81	A4
82	B4
83	C3
84	B3
85	A3
86	A2
87	A1
88	B2
89	B1
90	C2
91	C1
92	D2
93	D1
94	E1
95	E2
96	F2
97	F1
98	G1
99	G2
100	H2
101	H1
102	J2
103	J1
104	K1
105	N6

Bit#	Ball ID
106	K3
107	K4
108	K6
109	K2
110	L2
111	L1
112	M2
113	M1
114	N2
115	N1
116	P2
117	P1
118	R2
119	R1
120	T2
121	T1
122	U2
123	U1
124	V2
125	V1
126	W2
127	W1
128	T6
129	U3
130	V3
131	T4
132	T5
133	U4
134	V4
135	W5
136	V5
137	U5
138	Internal

Note
16. Bit# 138 is preset HIGH.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature -65 °C to +150 °C
 Ambient Temperature with Power Applied -55 °C to +125 °C
 Supply Voltage on V_{DD} Relative to GND -0.5 V to +4.6 V
 Supply Voltage on V_{DDQ} Relative to GND -0.5 V to +V_{DD}
 DC Voltage Applied to Outputs in Tri-State -0.5 V to V_{DDQ} + 0.5 V

DC Input Voltage -0.5 V to V_{DD} + 0.5 V
 Current into Outputs (LOW) 20 mA
 Static Discharge Voltage > 2001 V (MIL-STD-883, Method 3015)
 Latch Up Current > 200 mA

Operating Range

Range	Ambient Temperature	V _{DD}	V _{DDQ}
Commercial	0 °C to +70 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V _{DD}
Industrial	-40 °C to +85 °C		

Electrical Characteristics

Over the Operating Range^[17, 18]

Parameter	Description	Test Conditions	Min	Max	Unit	
V _{DD}	Power Supply Voltage		3.135	3.6	V	
V _{DDQ}	IO Supply Voltage	for 3.3 V IO	3.135	V _{DD}	V	
		for 2.5 V IO	2.375	2.625	V	
V _{OH}	Output HIGH Voltage	for 3.3 V IO, I _{OH} = -4.0 mA	2.4	-	V	
		for 2.5 V IO, I _{OH} = -1.0 mA	2.0	-	V	
V _{OL}	Output LOW Voltage	for 3.3 V IO, I _{OL} = 8.0 mA	-	0.4	V	
		for 2.5 V IO, I _{OL} = 1.0 mA	-	0.4	V	
V _{IH}	Input HIGH Voltage ^[17]	for 3.3 V IO	2.0	V _{DD} + 0.3 V	V	
		for 2.5 V IO	1.7	V _{DD} + 0.3 V	V	
V _{IL}	Input LOW Voltage ^[17]	for 3.3 V IO	-0.3	0.8	V	
		for 2.5 V IO	-0.3	0.7	V	
I _X	Input Leakage Current except ZZ and MODE	GND ≤ V _I ≤ V _{DDQ}	-5	5	μA	
	Input Current of MODE	Input = V _{SS}	-30	-	μA	
		Input = V _{DD}	-	5	μA	
	Input Current of ZZ	Input = V _{SS}	-5	-	μA	
Input = V _{DD}		-	30	μA		
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{DDQ} , Output Disabled	-5	5	μA	
I _{DD}	V _{DD} Operating Supply Current	V _{DD} = Max, I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{CYC}	7.5 ns cycle, 133 MHz	-	310	mA
			10 ns cycle, 100 MHz	-	290	mA
I _{SB1}	Automatic CE Power Down Current—TTL Inputs	V _{DD} = Max, Device Deselected, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} ; f = f _{MAX} , Inputs Switching	7.5 ns cycle, 133 MHz	-	180	mA
			10 ns cycle, 100 MHz	-	180	mA
I _{SB2}	Automatic CE Power Down Current—CMOS Inputs	V _{DD} = Max, Device Deselected, V _{IN} ≤ 0.3 V or V _{IN} ≥ V _{DD} - 0.3 V, f = 0, Inputs Static	-	120	mA	
I _{SB3}	Automatic CE Power Down Current—CMOS Inputs	V _{DD} = Max, Device Deselected, or V _{IN} ≤ 0.3 V or V _{IN} ≥ V _{DDQ} - 0.3 V, f = f _{MAX} , Inputs Switching	7.5 ns cycle, 133 MHz	-	180	mA
			10 ns cycle, 100 MHz	-	180	mA
I _{SB4}	Automatic CE Power Down Current—TTL Inputs	V _{DD} = Max, Device Deselected, V _{IN} ≥ V _{DD} - 0.3 V or V _{IN} ≤ 0.3 V, f = 0, Inputs Static	-	135	mA	

Notes

17. Overshoot: V_{IH}(AC) < V_{DD} + 1.5 V (Pulse width less than t_{CYC}/2), undershoot: V_{IL}(AC) > -2 V (Pulse width less than t_{CYC}/2).
 18. T_{Power-up}: Assumes a linear ramp from 0 V to V_{DD}(min.) within 200 ms. During this time V_{IH} < V_{DD} and V_{DDQ} ≤ V_{DD}.

Capacitance

In the following table, the capacitance parameters are listed.^[19]

Parameter	Description	Test Conditions	100-pin TQFP Max	165-ball FBGA Max	209-ball FBGA Max	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{DD} = 3.3V V _{DDQ} = 2.5V	6.5	7	5	pF
C _{CLK}	Clock Input Capacitance		3	7	5	pF
C _{IO}	Input/Output Capacitance		5.5	6	7	pF

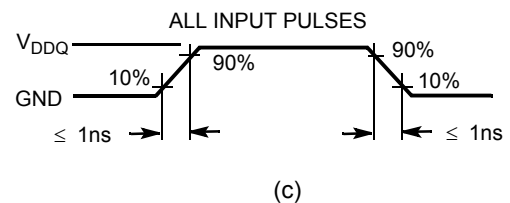
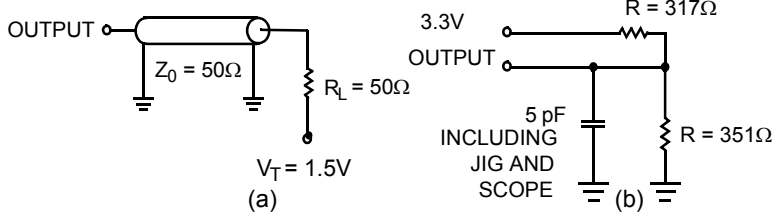
Thermal Resistance

In the following table, the thermal resistance parameters are listed^[19]

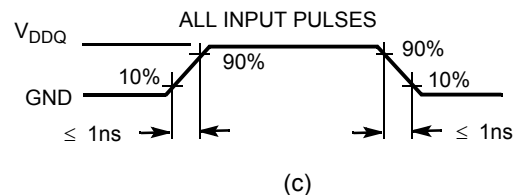
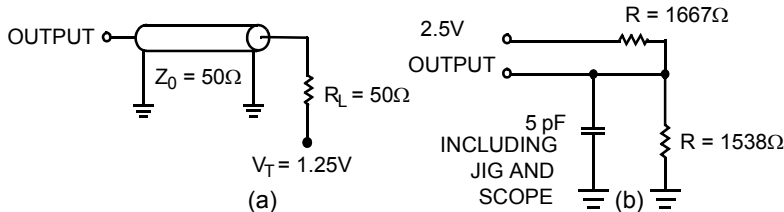
Parameter	Description	Test Conditions	100-pin TQFP Package	165-ball FBGA Package	209-ball FBGA Package	Unit
Θ _{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, according to EIA/JESD51.	25.21	20.8	25.31	°C/W
Θ _{JC}	Thermal Resistance (Junction to Case)		2.28	3.2	4.48	°C/W

Figure 1. AC Test Loads and Waveforms

3.3V IO Test Load



2.5V IO Test Load



Note

19. Tested initially and after any design or process change that may affect these parameters.

Switching Characteristics

 Over the Operating Range^[20, 21]

Parameter	Description	133 MHz		100 MHz		Unit
		Min	Max	Min	Max	
$t_{POWER}^{[22]}$		1	–	1	–	ms
Clock						
t_{CYC}	Clock Cycle Time	7.5	–	10	–	ns
t_{CH}	Clock HIGH	2.5	–	3.0	–	ns
t_{CL}	Clock LOW	2.5	–	3.0	–	ns
Output Times						
t_{CDV}	Data Output Valid After CLK Rise	–	6.5	–	8.5	ns
t_{DOH}	Data Output Hold After CLK Rise	2.5	–	2.5	–	ns
t_{CLZ}	Clock to Low Z ^[23, 24, 25]	2.5	–	2.5	–	ns
t_{CHZ}	Clock to High Z ^[23, 24, 25]	–	3.8	0	4.5	ns
t_{OEV}	\overline{OE} LOW to Output Valid	–	3.0	–	3.8	ns
t_{OELZ}	\overline{OE} LOW to Output Low Z ^[23, 24, 25]	0	–	0	–	ns
t_{OEZH}	\overline{OE} HIGH to Output High Z ^[23, 24, 25]	–	3.0	–	4.0	ns
Setup Times						
t_{AS}	Address Setup Before CLK Rise	1.5	–	1.5	–	ns
t_{ALS}	$\overline{ADV}/\overline{LD}$ Setup Before CLK Rise	1.5	–	1.5	–	ns
t_{WES}	\overline{WE} , \overline{BW}_X Setup Before CLK Rise	1.5	–	1.5	–	ns
t_{CENS}	\overline{CEN} Setup Before CLK Rise	1.5	–	1.5	–	ns
t_{DS}	Data Input Setup Before CLK Rise	1.5	–	1.5	–	ns
t_{CES}	Chip Enable Setup Before CLK Rise	1.5	–	1.5	–	ns
Hold Times						
t_{AH}	Address Hold After CLK Rise	0.5	–	0.5	–	ns
t_{ALH}	$\overline{ADV}/\overline{LD}$ Hold After CLK Rise	0.5	–	0.5	–	ns
t_{WEH}	\overline{WE} , \overline{BW}_X Hold After CLK Rise	0.5	–	0.5	–	ns
t_{CENH}	\overline{CEN} Hold After CLK Rise	0.5	–	0.5	–	ns
t_{DH}	Data Input Hold After CLK Rise	0.5	–	0.5	–	ns
t_{CEH}	Chip Enable Hold After CLK Rise	0.5	–	0.5	–	ns

Notes

20. Timing reference level is 1.5 V when $V_{DDQ} = 3.3$ V and is 1.25 V when $V_{DDQ} = 2.5$ V.

21. Test conditions shown in (a) of Figure 1 on page 23 unless otherwise noted.

22. This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied above V_{DD} (minimum) initially, before a read or write operation can be initiated.

23. t_{CHZ} , t_{CLZ} , t_{OELZ} , and t_{OEZH} are specified with AC test conditions shown in part (b) of Figure 1 on page 23. Transition is measured ± 200 mV from steady-state voltage.

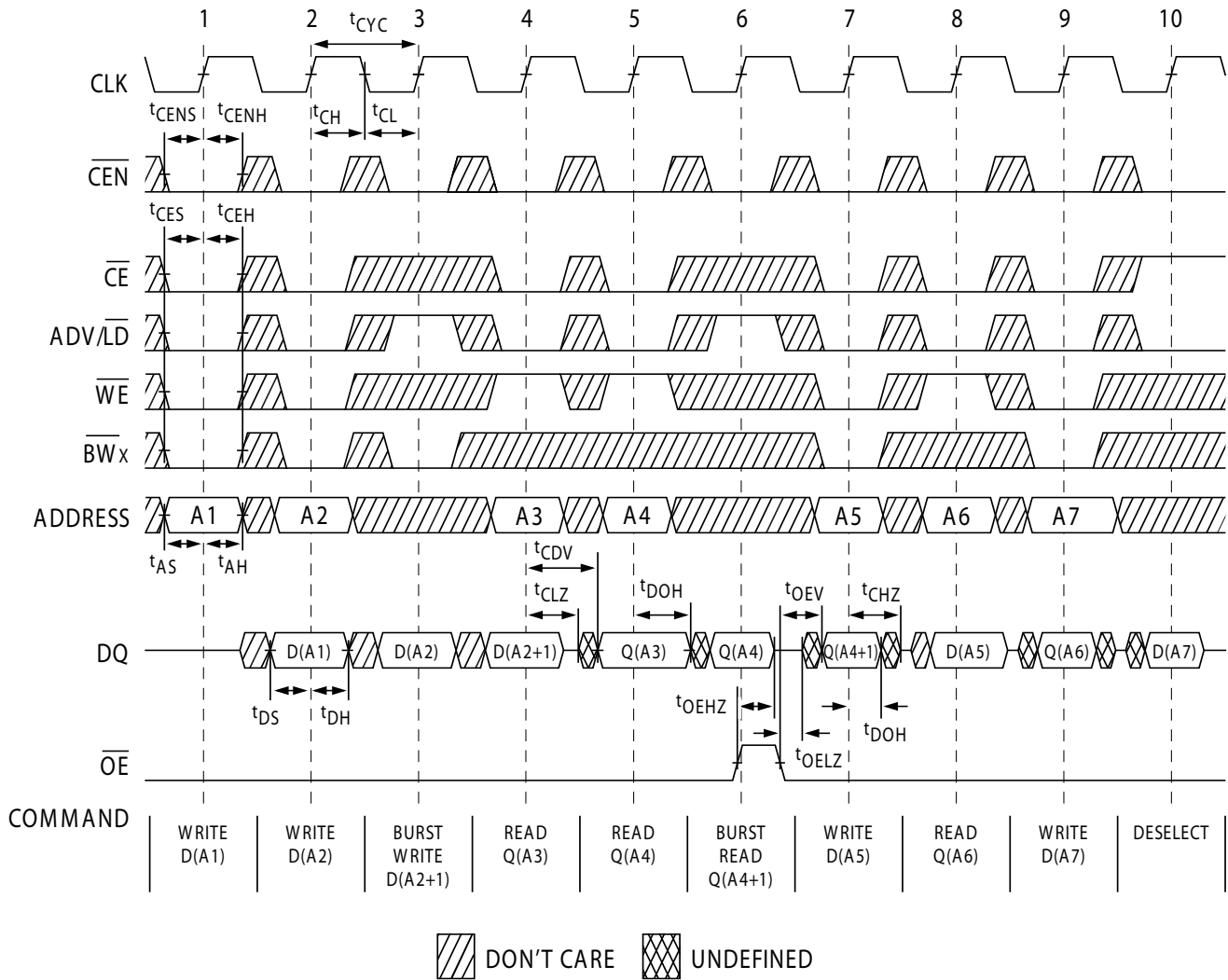
24. At any voltage and temperature, t_{OEZH} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus.

These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High Z prior to Low Z under the same system conditions.

25. This parameter is sampled and not 100% tested.

Switching Waveforms

Figure 2. Read/Write Waveforms^[26, 27, 28]



Notes

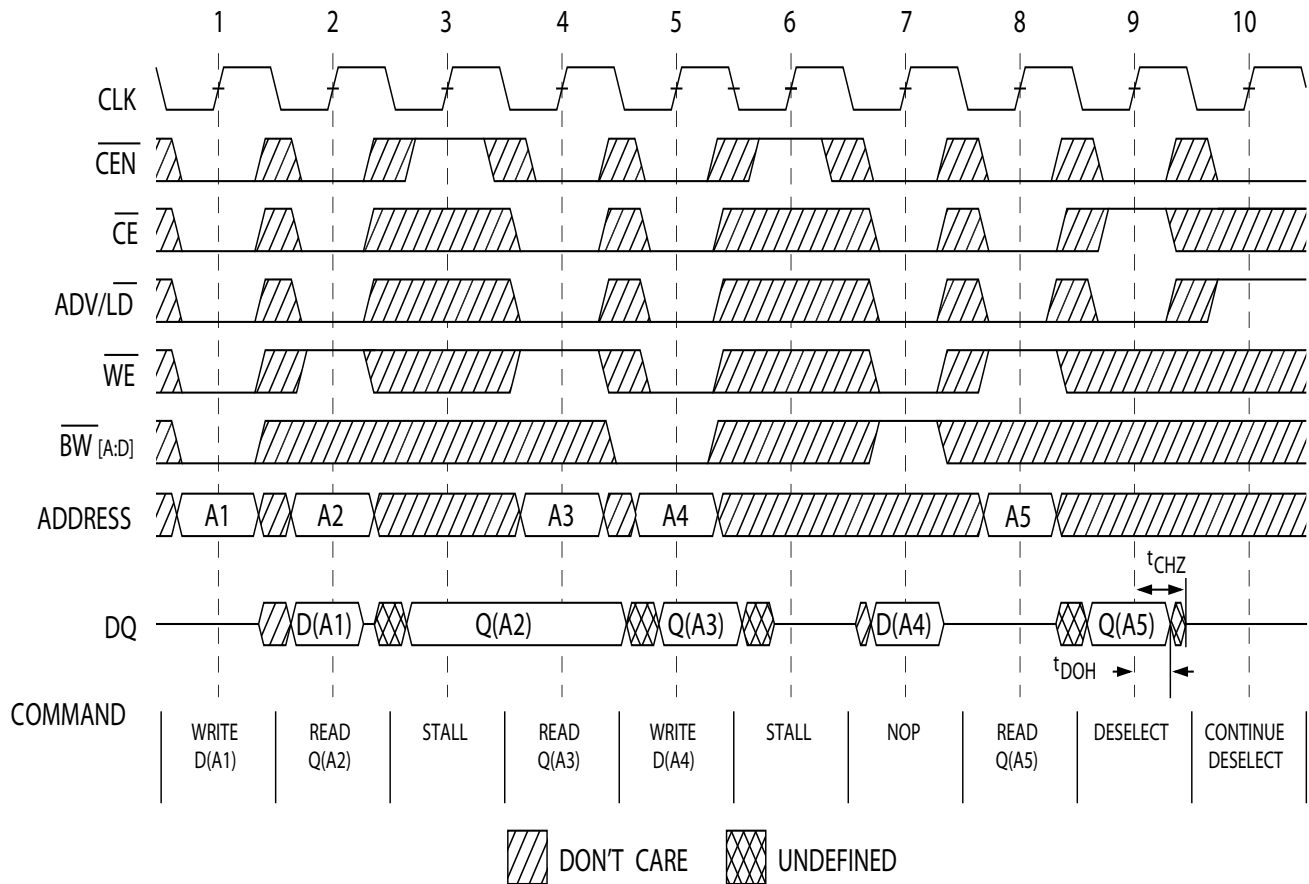
26. For this waveform ZZ is tied LOW.

27. When \overline{CE} is LOW, \overline{CE}_1 is LOW, \overline{CE}_2 is HIGH and \overline{CE}_3 is LOW. When \overline{CE} is HIGH, \overline{CE}_1 is HIGH or \overline{CE}_2 is LOW or \overline{CE}_3 is HIGH.

28. Order of the burst sequence is determined by the status of the MODE (0 = Linear, 1 = Interleaved). Burst operations are optional.

Switching Waveforms (continued)

Figure 3. NOP, STALL, and DESELECT Cycles^[29, 30, 31]



Notes

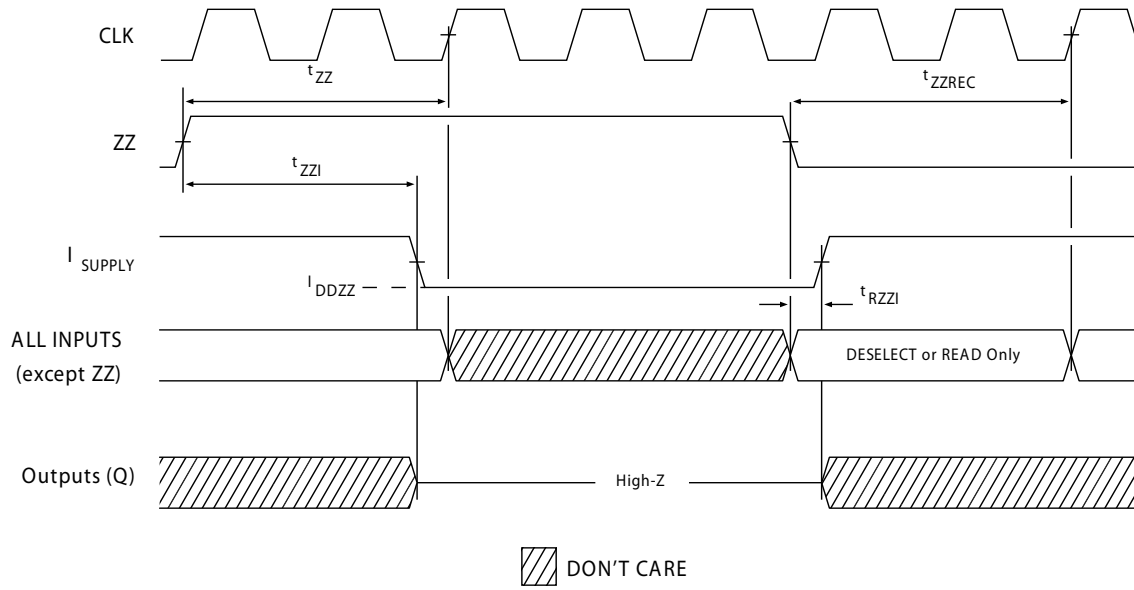
29. For this waveform ZZ is tied LOW.

30. When \overline{CE} is LOW, \overline{CE}_1 is LOW, \overline{CE}_2 is HIGH and \overline{CE}_3 is LOW. When \overline{CE} is HIGH, \overline{CE}_1 is HIGH or \overline{CE}_2 is LOW or \overline{CE}_3 is HIGH.

31. The IGNORE CLOCK EDGE or STALL cycle (Clock 3) illustrates \overline{CEN} being used to create a pause. A write is not performed during this cycle.

Switching Waveforms (continued)

Figure 4. ZZ Mode Timing^[32, 33]



Notes

- 32. Device must be deselected when entering ZZ mode. See truth table for all possible signal conditions to deselect the device.
- 33. DQs are in High Z when exiting ZZ sleep mode.

Ordering Information

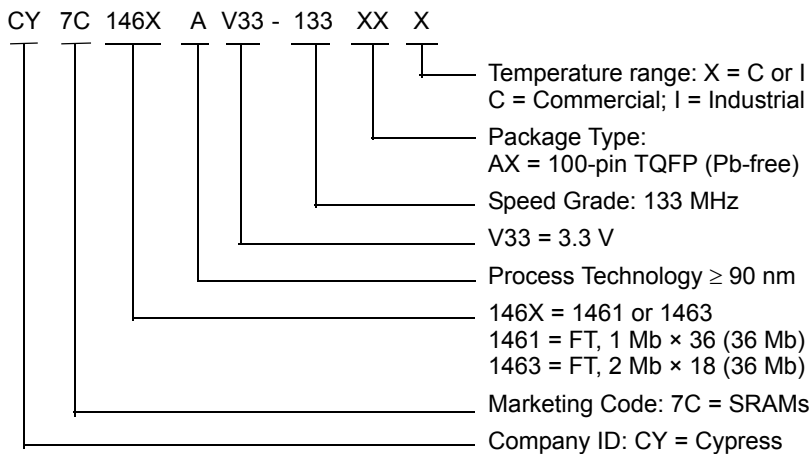
Cypress offers other versions of this type of product in different configurations and features. The following table contains only the list of parts that are currently available.

For a complete listing of all options, visit the Cypress website at www.cypress.com and refer to the product summary page at <http://www.cypress.com/products>, or contact your local sales representative.

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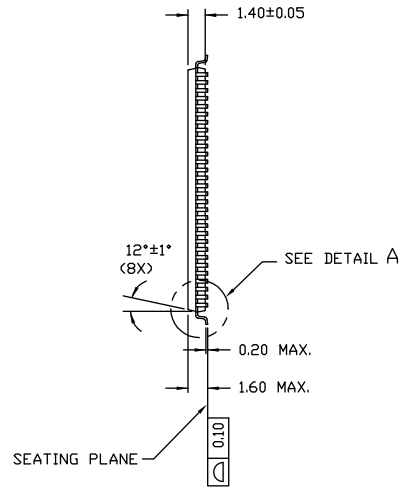
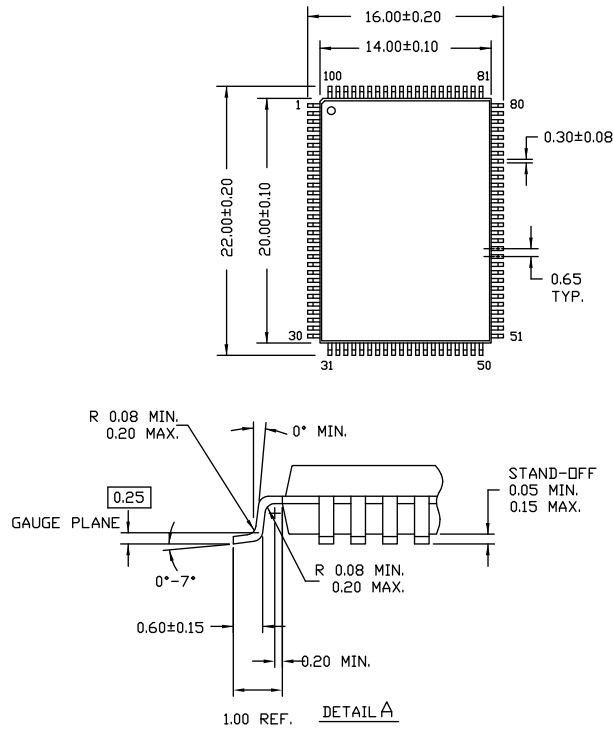
Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
133	CY7C1461AV33-133AXC	51-85050	100-pin Thin Quad Flat Pack (14 × 20 × 1.4 mm) Pb-free	Commercial
	CY7C1463AV33-133AXC			
	CY7C1461AV33-133AXI	51-85050	100-pin Thin Quad Flat Pack (14 × 20 × 1.4 mm) Pb-free	Industrial

Ordering Code Definitions



Package Diagrams

Figure 5. 100-pin TQFP (14 × 20 × 1.4 mm), 51-85050

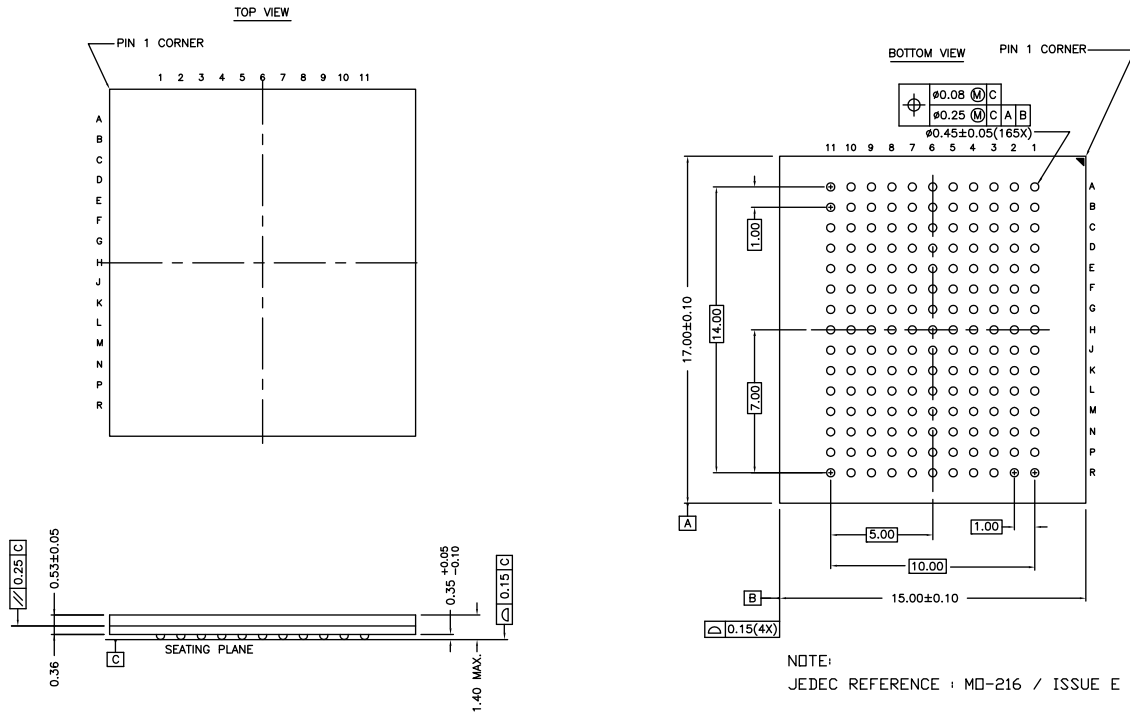


- NOTE:
1. JEDEC STD REF MS-026
 2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
 3. DIMENSIONS IN MILLIMETERS

51-85050 *D

Package Diagrams (continued)

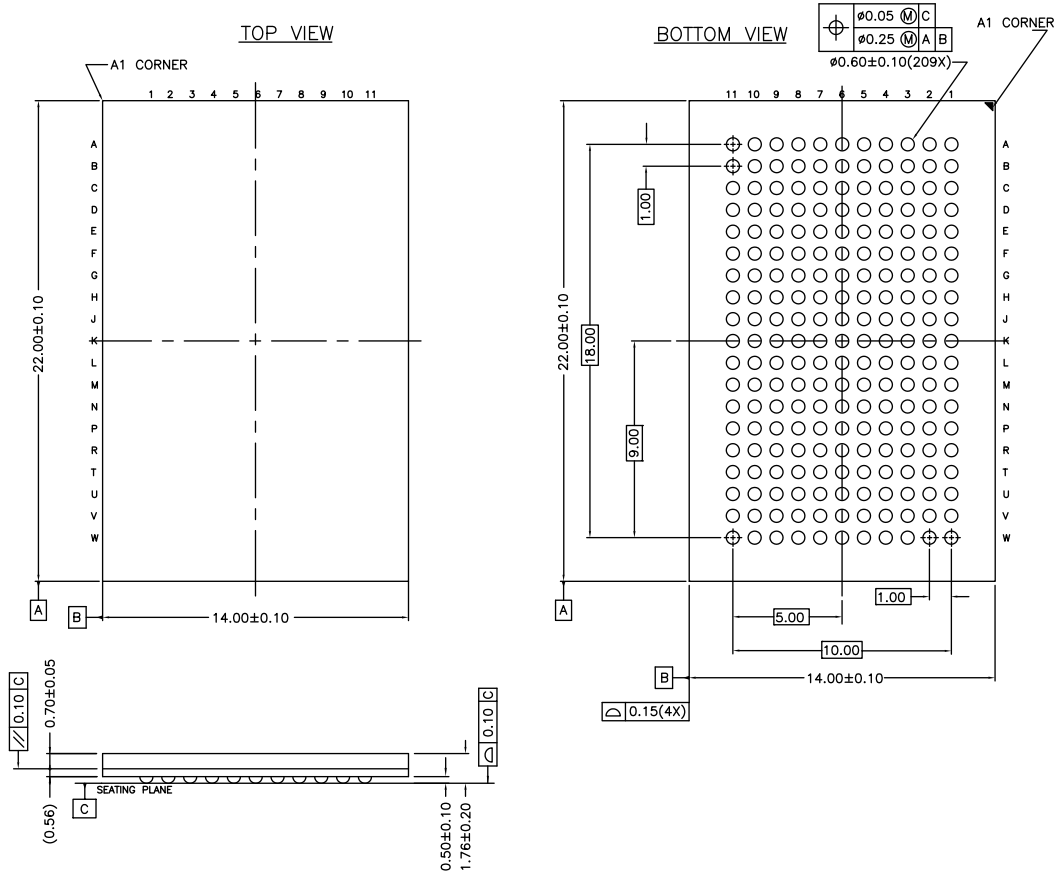
Figure 6. 165-ball FBGA (15 × 17 × 1.4 mm), 51-85165



51-85165 *B

Package Diagrams (continued)

Figure 7. 209-ball FBGA (14 × 22 × 1.76 mm), 51-85167



51-85167 *A

Document History Page

Document Title: CY7C1461AV33/CY7C1463AV33/CY7C1465AV33 36-Mbit (1 M × 36/2 M × 18/512 K × 72) Flow-Through SRAM with NoBL™ Architecture Document Number: 38-05356				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	254911	See ECN	SYT	New data sheet Part number changed from previous revision. New and old part number differ by the letter "A"
*A	300131	See ECN	SYT	Removed 150- and 117-MHz Speed Bins Changed Θ_{JA} and Θ_{JC} from TBD to 25.21 and 2.58 °C/W, respectively, for TQFP package Added Pb-free information for 100-pin TQFP, 165 FBGA and 209 FBGA packages Added "Pb-free BG and BZ packages availability" below the Ordering Information
*B	320813	See ECN	SYT	Changed H9 pin from V_{SSQ} to V_{SS} on the Pin Configuration table for 209 FBGA Changed the test condition from $V_{DD} = \text{Min.}$ to $V_{DD} = \text{Max}$ for V_{OL} in the Electrical Characteristics table Replaced the TBD's for I_{DD} , I_{SB1} , I_{SB2} , I_{SB3} and I_{SB4} to their respective values Replaced TBD's for Θ_{JA} and Θ_{JC} to their respective values on the Thermal Resistance table for 165 FBGA and 209 FBGA Packages Changed C_{IN} , C_{CLK} and C_{IO} to 6.5, 3 and 5.5 pF from 5, 5 and 7 pF for TQFP Package Removed "Pb-free BG packages availability" comment below the Ordering Information
*C	331551	See ECN	SYT	Modified Address Expansion balls in the pinouts for 165 FBGA and 209 FBGA Packages according to JEDEC standards and updated the Pin Definitions accordingly Modified V_{OL} , V_{OH} test conditions Replaced TBD to 100 mA for I_{DDZZ} Changed C_{IN} , C_{CLK} and C_{IO} to 7, 7 and 6 pF from 5, 5 and 7 pF for 165 FBGA Package Added Industrial Temperature Grade Changed I_{SB2} and I_{SB4} from 100 and 110 mA to 120 and 135 mA respectively Updated the Ordering Information by shading and unshading MPNs according to availability
*D	417547	See ECN	R XU	Converted from Preliminary to Final Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Changed I_X current value in MODE from -5 & 30 μA to -30 & 5 μA respectively and also Changed I_X current value in ZZ from -30 & 5 μA to -5 & 30 μA respectively on page# 20 Modified test condition from $V_{IH} \leq V_{DD}$ to $V_{IH} < V_{DD}$ Modified "Input Load" to "Input Leakage Current except ZZ and MODE" in the Electrical Characteristics Table Replaced Package Name column with Package Diagram in the Ordering Information table Replaced Package Diagram of 51-85050 from *A to *B Updated the Ordering Information

Document History Page (continued)

Document Title: CY7C1461AV33/CY7C1463AV33/CY7C1465AV33 36-Mbit (1 M × 36/2 M × 18/512 K × 72) Flow-Through SRAM with NoBL™ Architecture Document Number: 38-05356				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
*E	473650	See ECN	VKN	Added the Maximum Rating for Supply Voltage on V _{DDQ} Relative to GND. Changed t _{TH} , t _{TL} from 25 ns to 20 ns and t _{TDOV} from 5 ns to 10 ns in TAP AC Switching Characteristics table. Updated the Ordering Information table.
*F	1274733	See ECN	VKN/AESA	Corrected typo in the “NOP, STALL and DESELECT Cycles” waveform
*G	2499107	See ECN	VKN/PYRS	Corrected typo in the CY7C1465AV33 's Logic Block diagram
*H	2897278	03/22/2010	NJY	Removed obsolete part numbers from Ordering Information table and updated package diagrams.
*I	3208774	03/29/2011	NJY	Updated Ordering Information and added Ordering Code Definitions . Updated Package Diagrams . Updated in new template.

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