CY7C1061DV33

16-Mbit (1 M x 16) Static RAM

Features

- High speed
  - t_{AA} = 10 ns
- Low active power
  - I_{CC} = 175 mA at 10 ns
- Low CMOS standby power
  - I_{SB2} = 25 mA
- Operating voltages of 3.3 ± 0.3V
- 2.0V data retention
- Automatic power down when deselected
- TTL compatible inputs and outputs
- Easy memory expansion with $\overline{CE}_1$ and CE_2 features
- Available in Pb-free 54-pin TSOP II and 48-ball VFBGA packages
- Offered in single CE and dual CE options

Functional Description

The CY7C1061DV33 is a high performance CMOS Static RAM organized as 1,048,576 words by 16 bits.

To write to the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{19}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{19}).

To read from the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appears on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See the Truth Table on page 12 for a complete description of Read and Write modes.

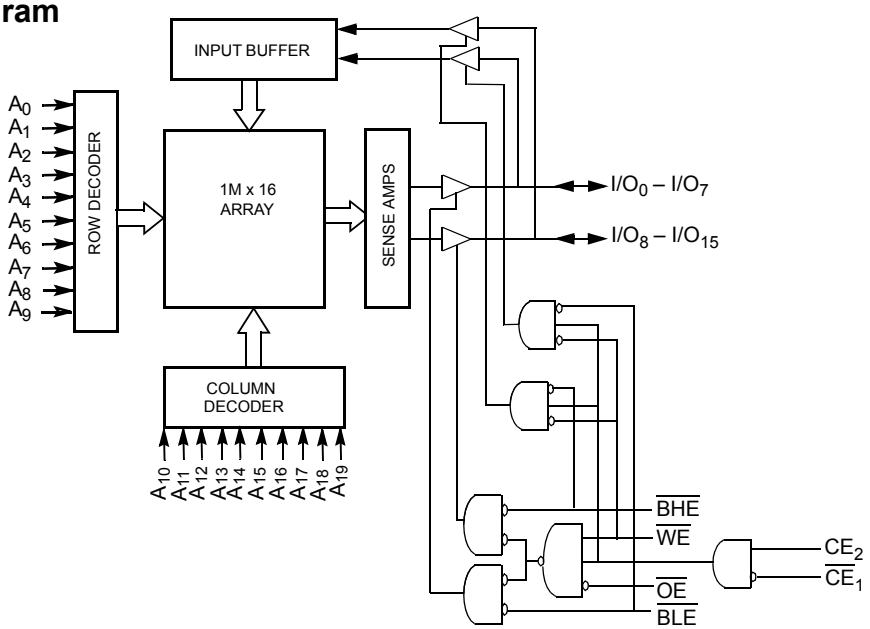
The input or output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$ HIGH/CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

The CY7C1061DV33 is available in a 54-pin TSOP II package with center power and ground (revolutionary) pinout, and 48-ball VFBGA packages.

Selection Guide

Description	–10	Unit
Maximum access time	10	ns
Maximum operating current	175	mA
Maximum CMOS standby current	25	mA

Logic Block Diagram



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Contents

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Pin Configuration

Figure 1. 48-Ball VFBGA Dual Chip Enable(-BVXI) (Top View) [1, 2]

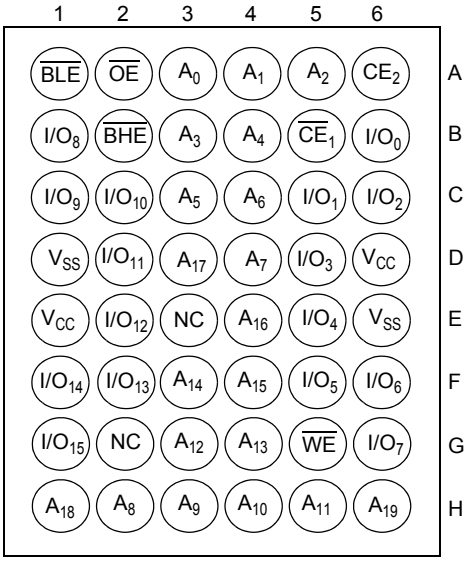
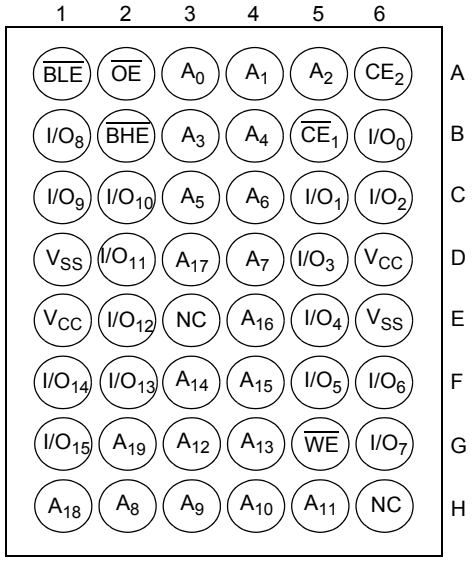


Figure 2. 48-Ball VFBGA Dual Chip Enable(-BVJXI) (Top View) [1, 2]



Notes
1. NC pins are not connected on the die.
2. In BVXI package, ball H6 is MSB address A19 and ball G2 is NC; in BVJXI package, ball H6 is NC and ball G2 is MSB address A19.

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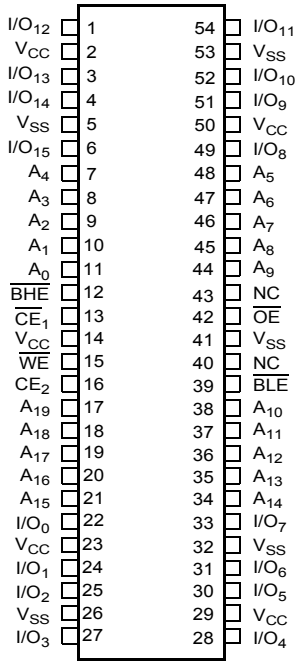
Figure 3. 54-Pin TSOP II (Top View) [3]



Note

3. NC pins are not connected on the die.

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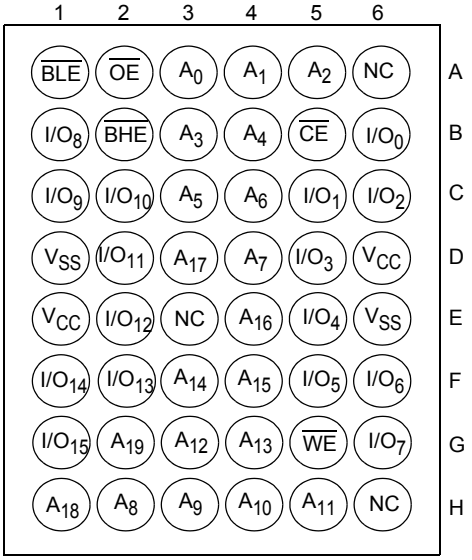
Figure 4. 48-Ball VFBGA Single Chip Enable (-BV1XI) (Top View) [4, 5]



Notes

4. NC pins are not connected on the die.
5. In BV1XI package, ball A6 is NC, ball H6 is NC and ball G2 is MSB address A19. BV1XI package has only single Chip Enable ($\overline{CE}$).

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Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage on V_{CC} Relative to GND[6]...–0.5 V to +4.6 V

DC Voltage Applied to Outputs in High Z State[6].....–0.5 V to V_{CC} + 0.5 V

DC Input Voltage[6] .....–0.5 V to V_{CC} + 0.5 V

Current into Outputs (LOW).....20 mA

Static Discharge Voltage..... .....>2001 V (MIL-STD-883, Method 3015)

Latch Up Current .....>200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	3.3 V ± 0.3 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	–10		Unit
			Min	Max	
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = –4.0 mA	2.4	–	V
V_{OL}	Output LOW voltage	V_{CC} = Min, I_{OL} = 8.0 mA	–	0.4	V
V_{IH}	Input HIGH voltage	–	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW voltage[6]	–	–0.3	0.8	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}	–1	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_{OUT} ≤ V_{CC}, Output disabled	–1	+1	µA
I_{CC}	V_{CC} operating supply current	V_{CC} = Max, f = f_{MAX} = $1/t_{RC}$, I_{OUT} = 0 mA CMOS levels		175	mA
I_{SB1}	Automatic CE power down current — TTL inputs	Max V_{CC}, $\overline{CE}_1$ ≥ V_{IH}, CE_2 ≤ V_{IL}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	–	30	mA
I_{SB2}	Automatic CE power down current —CMOS inputs	Max V_{CC}, $\overline{CE}_1$ ≥ V_{CC} – 0.3V, CE_2 ≤ 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0	–	25	mA

Note

6. V_{IL} (min) = –2.0 V and V_{IH}(max) = V_{CC} + 2 V for pulse durations of less than 20 ns.

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Capacitance

Tested initially and after any design or process changes that may affect these parameters.

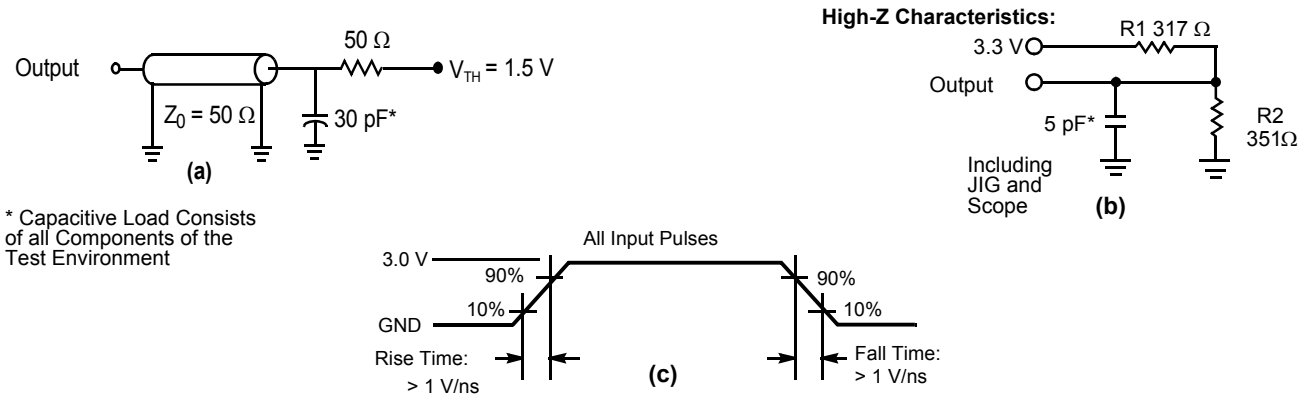
Parameter	Description	Test Conditions	TSOP II	VFBGA	Unit
C_{IN}	Input Capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 3.3 V	6	8	pF
C_{OUT}	I/O Capacitance		8	10	pF

Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	TSOP II	VFBGA	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	24.18	28.37	°C/W
Θ_{JC}	Thermal resistance (junction to case)		5.40	5.79	°C/W

Figure 5. AC Test Loads and Waveforms[7]



Note

7. Valid SRAM operation does not occur until the power supplies have reached the minimum operating V_{DD} (3.0 V). 100 µs (t_{power}) after reaching the minimum operating V_{DD}, normal SRAM operation begins including reduction in V_{DD} to the data retention (V_{CCDR}, 2.0 V) voltage.

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AC Switching Characteristics

Over the Operating Range[8]

Parameter	Description	–10		Unit
		Min	Max	
Read Cycle				
t_{power}	V_{CC}(Typical) to the First Access[9]	100	–	µs
t_{RC}	Read Cycle Time	10	–	ns
t_{AA}	Address to Data Valid	–	10	ns
t_{OHA}	Data Hold from Address Change	3	–	ns
t_{ACE}	$\overline{CE}_1$ LOW/CE_2 HIGH to Data Valid	–	10	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid	–	5	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	1	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [10]	–	5	ns
t_{LZCE}	$\overline{CE}_1$ LOW/CE_2 HIGH to Low Z[10]	3	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH/CE_2 LOW to High Z[10]	–	5	ns
t_{PU}	$\overline{CE}_1$ LOW/CE_2 HIGH to Power Up[11]	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH/CE_2 LOW to Power Down[11]	–	10	ns
t_{DBE}	Byte Enable to Data Valid	–	5	ns
t_{LZBE}	Byte Enable to Low Z	1	–	ns
t_{HZBE}	Byte Disable to High Z	–	5	ns
Write Cycle[12, 13]				
t_{WC}	Write Cycle Time	10	–	ns
t_{SCE}	$\overline{CE}_1$ LOW/CE_2 HIGH to Write End	7	–	ns
t_{AW}	Address Setup to Write End	7	–	ns
t_{HA}	Address Hold from Write End	0	–	ns
t_{SA}	Address Setup to Write Start	0	–	ns
t_{PWE}	$\overline{WE}$ Pulse Width	7	–	ns
t_{SD}	Data Setup to Write End	5.5	–	ns
t_{HD}	Data Hold from Write End	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[10]	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[10]	–	5	ns
t_{BW}	Byte Enable to End of Write	7	–	ns

Notes

8. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V. Test conditions for the read cycle use output loading shown in part a) of AC Test Loads and Waveforms[7], unless specified otherwise.
9. t_{POWER} gives the minimum amount of time that the power supply is at typical V_{CC} values until the first memory access is performed.
10. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{HZBE}, t_{LZOE}, t_{LZCE}, t_{LZWE}, and t_{LZBE} are specified with a load capacitance of 5 pF as in (b) of AC Test Loads and Waveforms[7]. Transition is measured ±200 mV from steady state voltage.
11. These parameters are guaranteed by design and are not tested.
12. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, and $CE_2 = V_{IH}$. Chip enables must be active and $\overline{WE}$ and byte enables must be LOW to initiate a write, and the transition of any of these signals can terminate. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
13. The minimum write cycle time for Write Cycle No. 2 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

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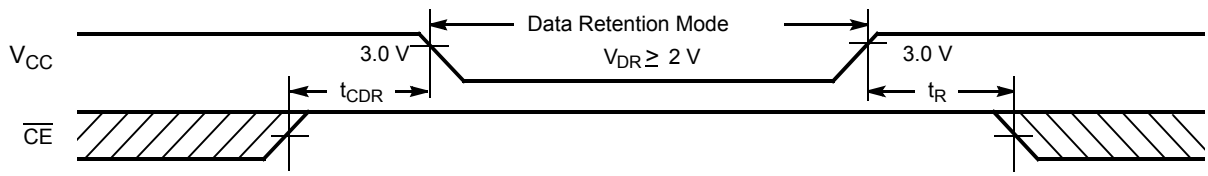
Data Retention Characteristics

Over the Operating Range

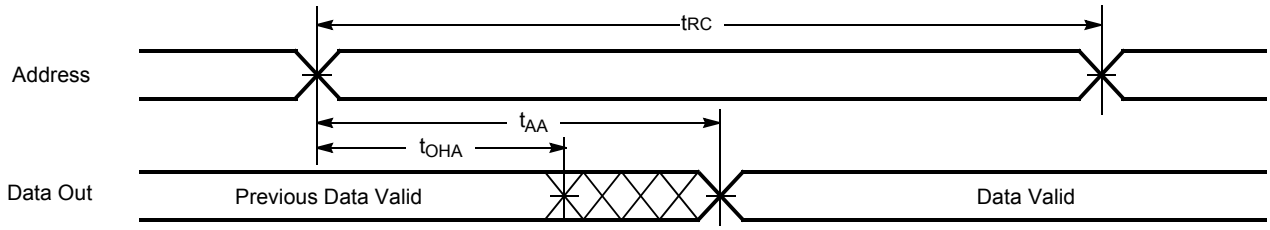
Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for data retention	–	2	–	V
I_{CCDR}	Data retention current	$V_{CC} = 2$ V, $\overline{CE}_1 \geq V_{CC} - 0.2$ V, $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	25	mA
t_{CDR} [14]	Chip deselect to data retention time	–	0	–	ns
t_R [15]	Operation recovery time	–	t_{RC}	–	ns

Figure 6. Data Retention Waveform[16]



Switching Waveforms

Figure 7. Read Cycle No. 1[17, 18]



Notes

14. Tested initially and after any design or process changes that may affect these parameters.
15. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 50$ µs or stable at $V_{CC(min.)} \geq 50$ µs.
16. For all packages except -BV1XI, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH. For -BV1XI package, $\overline{CE}$ refers to $\overline{CE}$.
17. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}.
18. $\overline{WE}$ is HIGH for read cycle.

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Switching Waveforms (continued)

Figure 8. Read Cycle No. 2 ($\overline{OE}$ Controlled) [19, 20, 21]

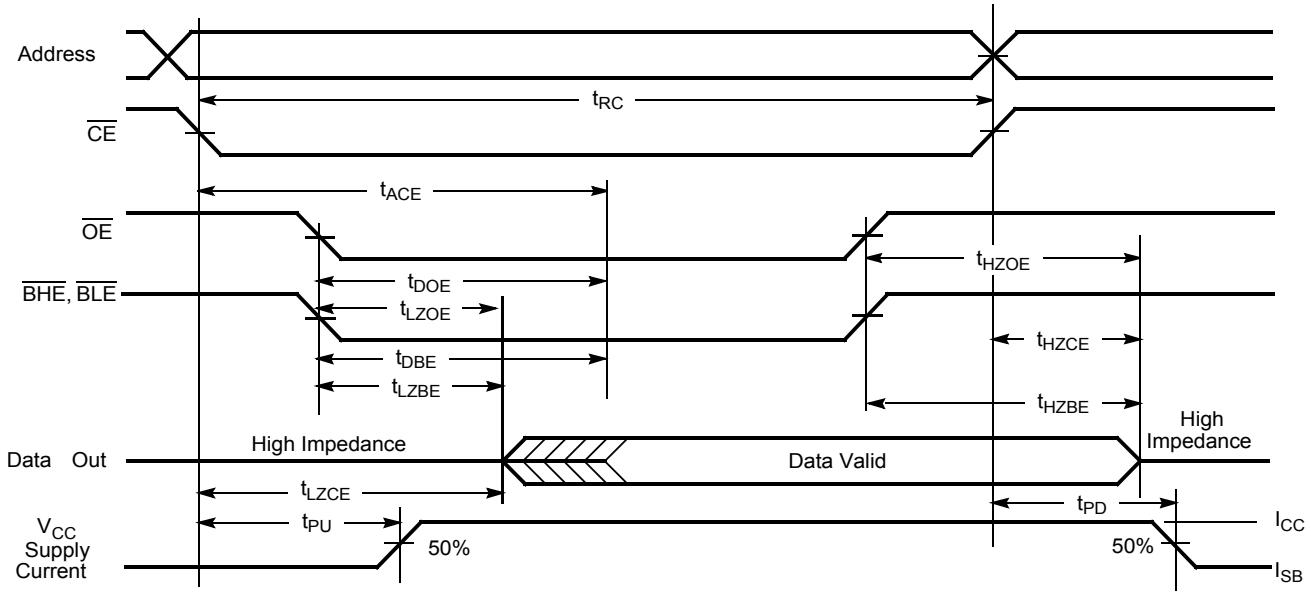
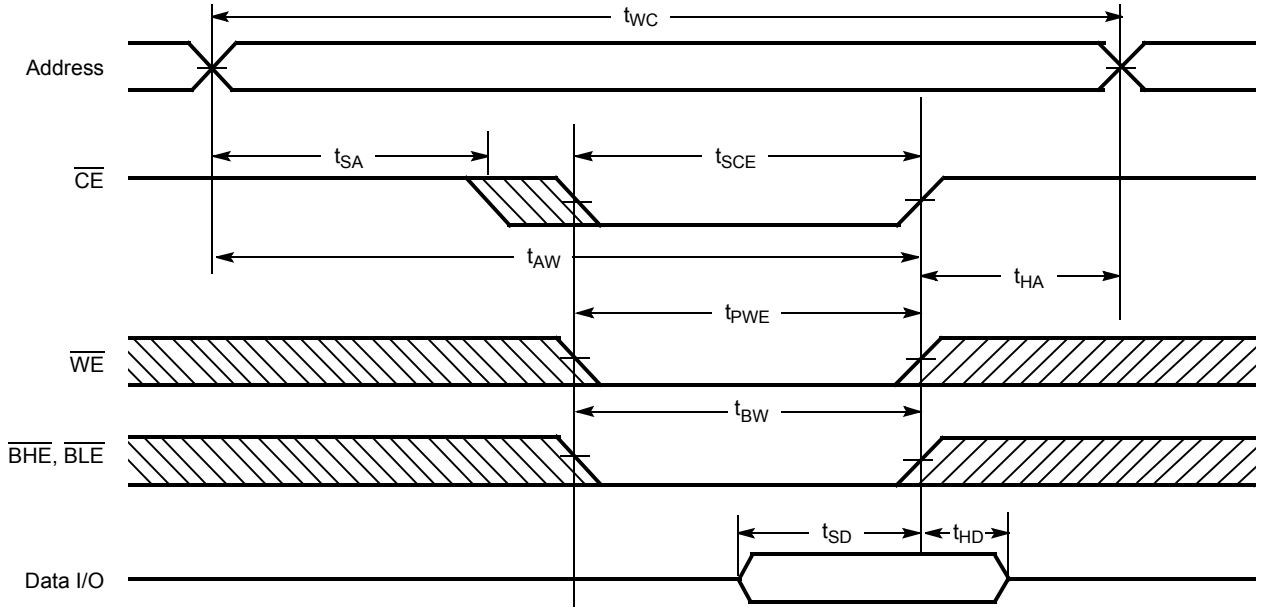


Figure 9. Write Cycle No. 1 ($\overline{CE}$ Controlled) [19, 22, 23]



Notes

19. For all packages except -BV1XI, $\overline{CE}$ is the logical combination of $\overline{CE_1}$ and CE_2. When $\overline{CE_1}$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE_1}$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH. For -BV1XI package, CE refers to CE.
20. $\overline{WE}$ is HIGH for read cycle.
21. Address valid before or similar to $\overline{CE}$ transition LOW.
22. Data I/O is high impedance if $\overline{OE}$, $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
23. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

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Switching Waveforms (continued)

Figure 10. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [24, 25, 26]

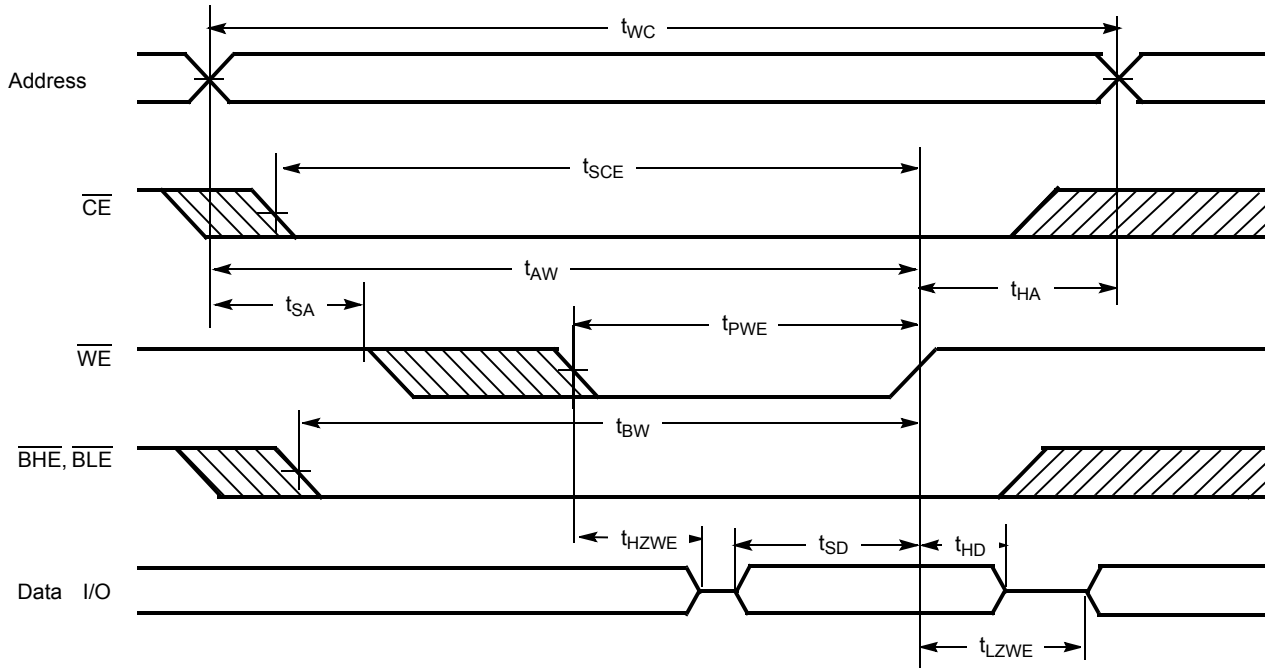
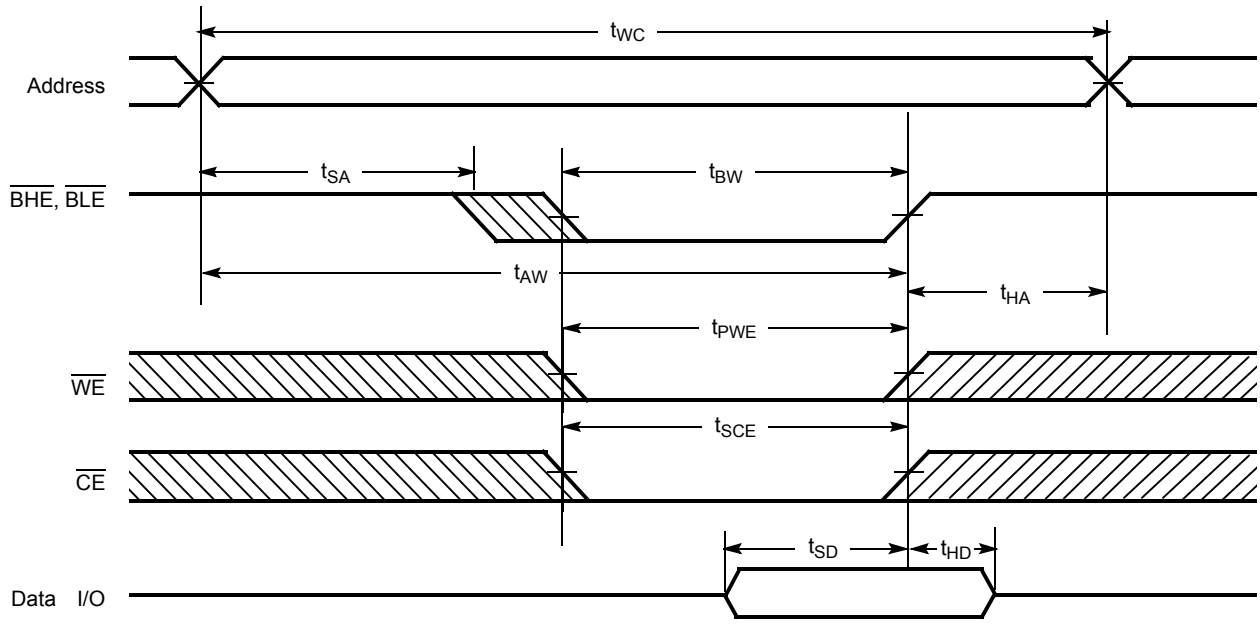


Figure 11. Write Cycle No. 3 ($\overline{BLE}$ or $\overline{BHE}$ Controlled) [24]



Notes

24. For all packages except -BV1XI, $\overline{CE}$ is the logical combination of $\overline{CE_1}$ and CE_2. When $\overline{CE_1}$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE_1}$ is HIGH or CE_2 is LOW, CE is HIGH. For -BV1XI package, CE refers to $\overline{CE}$.
25. Data I/O is high impedance if $\overline{OE}$, $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
26. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

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Truth Table

For all packages except -BV1XI

$\overline{CE}_1$	CE_2	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	$I/O_0 – IO_7$	$I/O_8 – I/O_{15}$	Mode	Power
H	X	X	X	X	X	High Z	High Z	Power down	Standby (I_{SB})
X	L	X	X	X	X	High Z	High Z	Power down	Standby (I_{SB})
L	H	L	H	L	L	Data out	Data out	Read all bits	Active (I_{CC})
L	H	L	H	L	H	Data out	High Z	Read lower bits only	Active (I_{CC})
L	H	L	H	H	L	High Z	Data out	Read upper bits only	Active (I_{CC})
L	H	X	L	L	L	Data in	Data in	Write all bits	Active (I_{CC})
L	H	X	L	L	H	Data in	High Z	Write lower bits only	Active (I_{CC})
L	H	X	L	H	L	High Z	Data in	Write upper bits only	Active (I_{CC})
L	H	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active (I_{CC})

Truth Table

For -BV1XI package only

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	$I/O_0 – I/O_7$	$I/O_8 – I/O_{15}$	Mode	Power
H	X	X	X	X	High Z	High Z	Power down	Standby (I_{SB})
L	L	H	L	L	Data out	Data out	Read all bits	Active (I_{CC})
L	L	H	L	H	Data out	High Z	Read lower bits only	Active (I_{CC})
L	L	H	H	L	High Z	Data out	Read upper bits only	Active (I_{CC})
L	X	L	L	L	Data in	Data in	Write all bits	Active (I_{CC})
L	X	L	L	H	Data in	High Z	Write lower bits only	Active (I_{CC})
L	X	L	H	L	High Z	Data in	Write upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active (I_{CC})

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Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1061DV33-10ZSXI	51-85160	54-pin TSOP II (Pb-free)	Industrial
	CY7C1061DV33-10BVXI	51-85178	48-ball VFBGA (8 × 9.5 × 1 mm) (Pb-free) (Dual Chip Enable)	
	CY7C1061DV33-10BVJXI		48-ball VFBGA (8 × 9.5 × 1 mm) (Pb-free) (Dual Chip Enable - JEDEC compatible)	
	CY7C1061DV33-10BV1XI		48-Ball VFBGA (8 × 9.5 × 1 mm) (Pb-free) (Single Chip Enable)	

Ordering Code Definitions

CY 7 C 1 06 1 D V33 - 10 XXX I

- I: Temperature Range: I = Industrial
- XXX: Package Type: XXX = ZSX or BVX or BVJX
  - ZSX = 54-pin TSOP II (Pb-free)
  - BVX = 48-ball VFBGA (Pb-free)
  - BVJX = 48-ball VFBGA (Pb-free)
- 10: Speed: 10 ns
- V33: V33 = Voltage range (3 V to 3.6 V)
- D: D = C9, 90 nm Technology
- 1: 1 = Data width × 16-bits
- 06: 06 = 16-Mbit density
- 1: 1 = Fast Asynchronous SRAM family
- C: Technology Code: C = CMOS
- 7: 7 = SRAM
- CY: CY = Cypress

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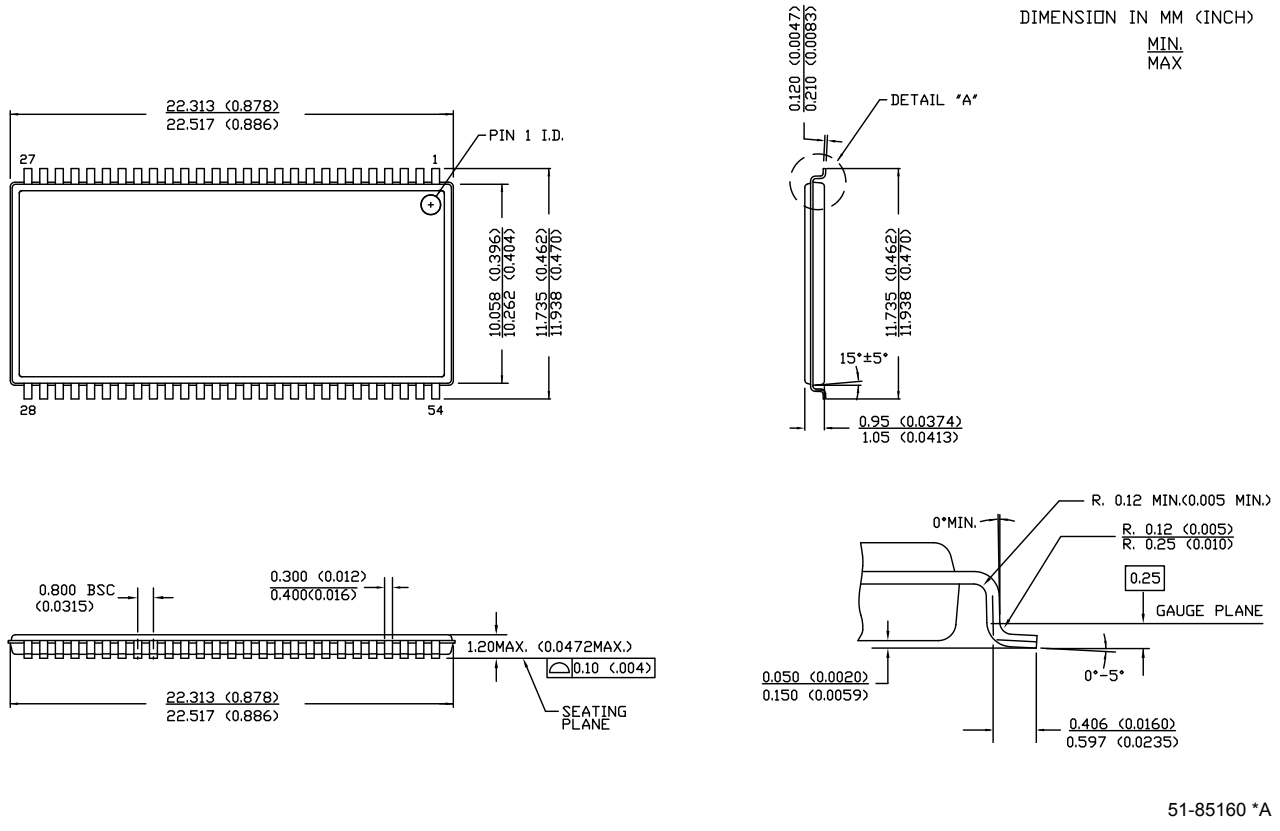
Package Diagrams

Figure 12. 54-Pin TSOP Type II



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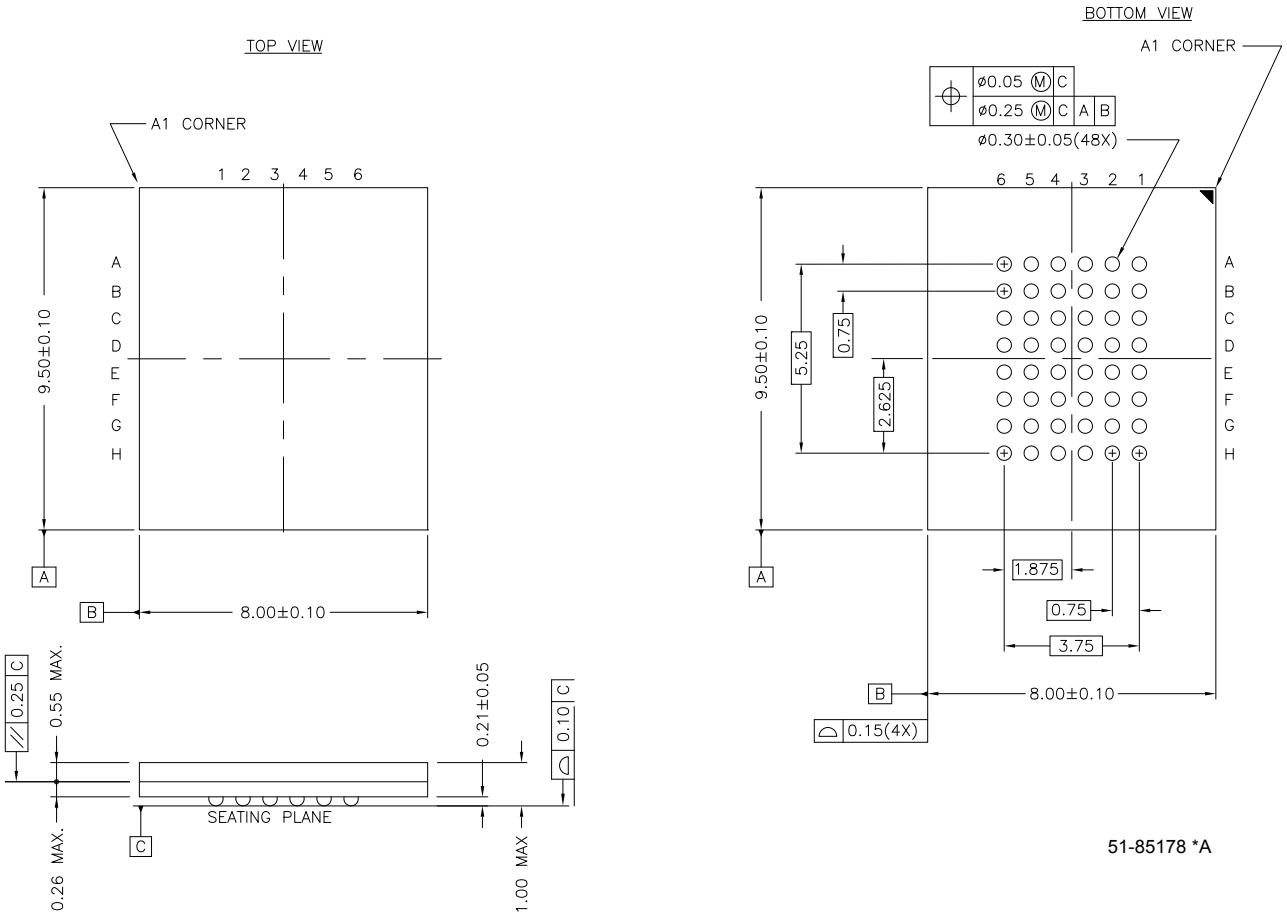
Package Diagrams (continued)

Figure 13. 48-Ball VFBGA (8 x 9.5 x 1 mm)



Acronyms

Acronym	Description
$\overline{BHE}$	byte high enable
$\overline{BLE}$	byte low enable
CMOS	complementary metal oxide semiconductor
$\overline{CE}$	chip enable
I/O	input/output
$\overline{OE}$	output enable
SRAM	static random access memory
TSOP	thin small outline package
VFBGA	very fine ball gird array
$\overline{WE}$	write enable

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Document History Page

Document Title: CY7C1061DV33 16-Mbit (1 M x 16) Static RAM Document Number: 38-05476				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	201560	SWI	See ECN	Advance data sheet for C9 IPP
*A	233748	RKF	See ECN	AC, DC parameters are modified as per EROS (Specification number 01-2165) Added Pb-free devices in the Ordering Information
*B	469420	NXR	See ECN	Converted from Advance Information to Preliminary Corrected typo in the Document Title Removed –8 and –12 speed bins from product offering Removed Commercial Operating Range Changed 2G-Ball of FBGA and pin 40 of TSOPII from DNU to NC Included the Maximum ratings for Static Discharge Voltage and Latch Up Current on page 3 Changed $I_{CC(Max)}$ from 220 mA to 125 mA Changed $I_{SB1(Max)}$ from 70 mA to 30 mA Changed $I_{SB2(Max)}$ from 40 mA to 25 mA Specified the Overshoot specification in footnote 1. Updated the Ordering Information Table
*C	499604	NXR	See ECN	Added note 1 for NC pins Updated Test Condition for I_{CC} in DC Electrical Characteristics table Updated the 48-Ball FBGA Package
*D	1462583	VKN/AESA	See ECN	Converted from preliminary to final Changed I_{CC} specification from 125 mA to 175 mA Updated thermal specs
*E	2704415	VKN/PYRS	05/11/09	Included 48 FBGA -BVJXI package Added footnote #2
*F	3109102	AJU	12/13/2010	Added Ordering Code Definitions. Updated Package Diagrams.
*G	3126531	PRAS	01/03/2011	Added 48-Ball VFBGA Single Chip Enable package. Updated Ordering Information. Added Acronyms.

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