

## CY7C1051DV33

# 8-Mbit (512 K × 16) Static RAM

### Features

- Temperature ranges
   □ Industrial: -40 °C to 85 °C
   □ Automotive-E: -40 °C to 125 °C<sup>[1]</sup>
- High speed
  □ t<sub>AA</sub> = 10 ns (Industrial)
- Low active power
   I<sub>CC</sub> = 110 mA at 10 ns (Industrial)
- Low CMOS standby power □ I<sub>SB2</sub> = 20 mA (Industrial)
- 2.0-V data retention
- Automatic power down when deselected
- Transistor-transistor logic (TTL)-compatible inputs and outputs
- Easy memory expansion with CE and OE features
- Available in Pb-free 48-ball fine ball grid array (FBGA) and 44-pin thin small outline package (TSOP) II packages

### **Functional Description**

The CY7C1051DV33<sup>[2]</sup> is a high performance CMOS Static RAM organized as 512 K words by 16 bits.

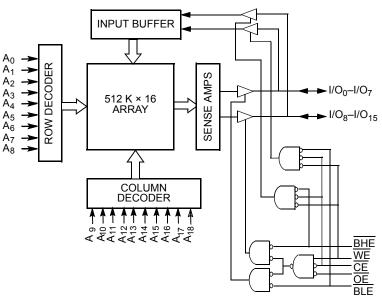
To write to the device, take Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte LOW Enable (BLE) is LOW, then data from I/O pins ( $I/O_0$ – $I/O_7$ ), is written into the location specified on the address pins ( $A_0$ – $A_{18}$ ). If Byte HIGH Enable (BHE) is LOW, then data from I/O pins ( $I/O_8$ – $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$ – $A_{18}$ ).

To read from the device, take Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte LOW Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins appears on I/O<sub>0</sub>–I/O<sub>7</sub>. If Byte HIGH Enable ( $\overline{BHE}$ ) is LOW, then data from memory appears on IO<sub>8</sub> to IO<sub>15</sub>. See the "Truth Table" on page 9 for a complete description of read and write modes.

The input/output pins  $(I/O_0-I/O_{15})$  are placed in <u>a</u> high-impedance state when the device is de<u>selected (CE</u> HIGH), the outputs are disabled (OE HIGH), the BHE and BLE are disabled (BHE, BLE HIGH), or a write operation (CE LOW, and WE LOW) is in progress.

The CY7C1051DV33 is available in a 44-pin TSOP II package with center power and ground (revolutionary) pinout and a 48-ball FBGA package.

### Logic Block Diagram



#### Notes

1. Automotive product information is preliminary.

2. For guidelines about SRAM system design, refer to the Cypress application note AN1064, SRAM System Guidelines available at www.cypress.com.

**Cypress Semiconductor Corporation** Document #: 001-00063 Rev. \*G 198 Champion Court

San Jose, CA 95134-1709 • 408-943-2600 Revised December 16, 2010



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### **Pin Configurations**

Figure 1. Pin Diagram - 48-ball FBGA (Top View)<sup>[3]</sup>

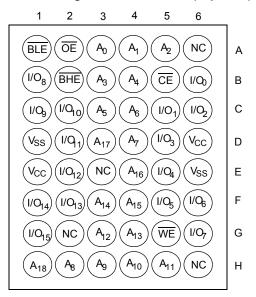


Figure 2. Pin Diagram - 44-Pin TSOP II (Top View)<sup>[3]</sup>

A <sub>0</sub> 🗖 1	44 🗆 A <sub>17</sub>
A <sub>1</sub> C 2	43 🗆 A <sub>16</sub>
A <sub>2</sub> 🗆 3	42 A15
A3 4	41 0 OF
A <sub>4</sub> 5	40 BHF
	39 1 BLE
1/0	38 I/O <sub>15</sub>
<b>u</b>	- "OI5
I/O <sub>2</sub> 🖸 9	
I/O3 🗖 10	35 I/O12
V <sub>CC</sub> 11	34 🗆 V <sub>SS</sub>
V <sub>SS</sub> □ 12	33 🗆 V <sub>CC</sub>
I/O4 🗖 13	32 🗖 I/O <sub>11</sub>
I/O <sub>5</sub> 🗆 14	31 ☐ I/O <sub>10</sub>
I/Q6 15	30 🗆 I/Qg
I/O7 16	29 🛛 I/Qš
WÉ 17	28 🗆 A <sub>18</sub>
A <sub>5</sub> □ <sup>18</sup>	27 🛛 A <sub>14</sub>
A <sub>6</sub> [ 19	26 🗆 A <sub>13</sub>
A7 20	25 🗆 A <sub>12</sub>
Ag 21	24 🗖 A11
A9 22	23 A10
° .	- 10

### **Selection Guide**

Description	–10 (Industrial)	-12 (Industrial)	–15 (Automotive-E) <sup>[4]</sup>	Unit
Maximum access time	10	12	15	ns
Maximum operating current	110	100	120	mA
Maximum CMOS standby current	20	20	20	mA

#### Notes

NC pins are not connected on the die.
 Automotive product information is preliminary.



## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature	–65 °C to +150 °C
Ambient temperature with power applied	–55 °C to +125 °C
Supply voltage on $V_{\mbox{\scriptsize CC}}$ to relative G	ND <sup>[5]</sup> –0.5 V to +4.6 V
DC voltage applied to outputs in high-Z state <sup>[5]</sup>	–0.3 V to V <sub>CC</sub> + 0.3 V
DC input voltage <sup>[5]</sup>	–0.3 V to $V_{CC}$ + 0.3 V
Current into outputs (LOW)	20 mA

Static discharge voltage.....>2001 V

(per MIL-STD-883, Method 3015)

Latch up current......>200 mA

### **Operating Range**

Range	Ambient Temperature	V <sub>cc</sub>	Speed
Industrial	–40 °C to +85 °C	$3.3~V\pm0.3~V$	10 ns
Industrial	–40 °C to +85 °C	$3.3~V\pm0.3~V$	12 ns
Auto-E <sup>[6]</sup>	–40 °C to +125 °C	$3.3~V\pm0.3~V$	15 ns

### DC Electrical Characteristics Over the Operating Range

Daramatar	Description	Test Conditions	-10(I	ndustrial)	–12(Industrial)		–15(Auto-E) <sup>[6]</sup>		Unit
Parameter	Description	rest conditions	Min	Max	Min	Max	Min	Max	Unit
V <sub>OH</sub>	Output HIGH voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 mA	2.4	-	2.4	-	2.4	-	V
V <sub>OL</sub>	Output LOW voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = 8.0 mA	-	0.4	_	0.4	-	0.4	V
V <sub>IH</sub>	Input HIGH voltage		2.0	$V_{CC} + 0.3$	2.0	$V_{CC} + 0.3$	2.0	$V_{CC} + 0.3$	V
V <sub>IL</sub> <sup>[5]</sup>	Input LOW voltage		-0.3	0.8	-0.3	0.8	-0.3	0.8	V
I <sub>IX</sub>	Input leakage current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	-5	+5	μA
I <sub>OZ</sub>	Output leakage current	$GND \le V_{OUT} \le V_{CC}$ , Output Disabled	-1	+1	–1	+1	-5	+5	μA
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	$V_{CC}$ = Max, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	_	110	-	100	_	120	mA
I <sub>SB1</sub>	Automatic CE power down current —TTL inputs	$\begin{array}{l} \text{Max } V_{CC}, \overline{CE} \geq V_{IH} \\ V_{IN} \geq V_{IH} \text{ or } V_{IN} \leq V_{IL}, f = f_{MAX} \end{array}$	-	40	_	35	-	60	mA
I <sub>SB2</sub>	Automatic CE Power Down Current —CMOS Inputs	$\begin{array}{l} \text{Max V}_{\text{CC}}, \overline{\text{CE}} \geq \text{V}_{\text{CC}} - 0.3 \text{ V}, \\ \text{V}_{\text{IN}} \geq \text{V}_{\text{CC}} - 0.3 \text{ V} \text{ or } \text{V}_{\text{IN}} \leq \\ 0.3 \text{ V}, \text{f} = 0 \end{array}$	-	20	_	20	-	20	mA

### Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	eter Description Test Conditions		Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = 3.3 V	12	pF
C <sub>OUT</sub>	I/O capacitance		12	pF

### **Thermal Resistance**

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	FBGA Package	TSOP II Package	Unit
Θ <sub>JA</sub>	Thermal resistance (Junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	28.31	51.43	°C/W
Θ <sub>JC</sub>	Thermal resistance (Junction to case)		11.4	15.8	°C/W

Notes

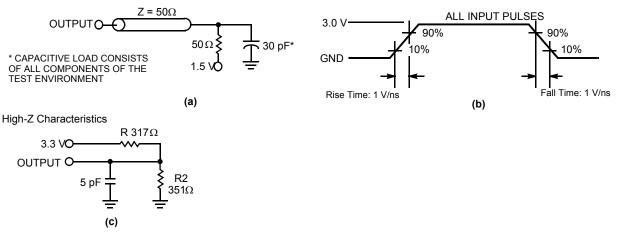
5.  $V_{IL(min)} = -2.0 \text{ V}$  and  $V_{IH(max)} = V_{CC} + 2.0 \text{ V}$  for pulse durations of less than 20 ns. 6. Automotive product information is preliminary.

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### AC Test Loads and Waveforms

AC characteristics (except High-Z) are tested using the load conditions shown in Figure 3 (a). High-Z characteristics are tested for all speeds using the test load shown in Figure 3 (c).



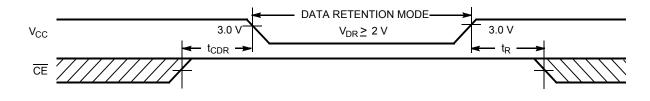
### Figure 3. AC Test Loads and Waveforms

### **Data Retention Characteristics**

Over the Operating Range

Parameter	Description	Conditions <sup>[7]</sup>	Min	Max	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention		2.0	-	V
ICCDR	Data Retention Current	$V_{CC} = V_{DR} = 2.0 \text{ V}, \overline{CE} \ge V_{CC} - 0.3 \text{ V},$ $V_{IN} \ge V_{CC} - 0.3 \text{ V} \text{ or } V_{IN} \le 0.3 \text{ V}$	-	20	mA
t <sub>CDR</sub> <sup>[8]</sup>	Chip Deselect to Data Retention Time	$V_{IN} \ge V_{CC} - 0.3 \text{ V or } V_{IN} \le 0.3 \text{ V}$	0	_	ns
t <sub>R</sub> <sup>[8]</sup>	Operation Recovery Time		t <sub>RC</sub>	Ι	ns

### **Data Retention Waveform**



#### Notes

7. No inputs may exceed  $V_{CC}$  + 0.3 V 8. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC}(min) \ge 50 \ \mu s$  or stable at  $V_{CC}(min) \ge 50 \ \mu s$ .



## **AC Switching Characteristics**

Over the Operating Range<sup>[9]</sup>

Demonster	Description	-10 (In	dustrial)	-12 (Industrial)		–15 (Auto-E) <sup>[1]</sup>		L Incié
Parameter	Description	Min	Max	Min	Max	Min	Max	Unit
Read Cycle					•	•	•	
t <sub>power</sub> <sup>[10]</sup>	V <sub>CC</sub> (typical) to the First Access	100	-	100	-	100	-	μS
t <sub>RC</sub>	Read Cycle Time	10	-	12	_	15	-	ns
t <sub>AA</sub>	Address to Data Valid	-	10	-	12		15	ns
t <sub>OHA</sub>	Data Hold from Address Change	2.5	-	2.5	_	3	-	ns
t <sub>ACE</sub>	CE LOW to Data Valid	-	10	-	12	_	15	ns
t <sub>DOE</sub>	OE LOW to Data Valid	-	5	-	6	_	7	ns
t <sub>LZOE</sub>	OE LOW to Low-Z	0	_	0	_	0	-	ns
t <sub>HZOE</sub>	OE HIGH to High-Z <sup>[11, 12]</sup>	_	5	_	6	_	7	ns
t <sub>LZCE</sub>	CE LOW to Low-Z <sup>[12]</sup>	3	-	3	-	3	-	ns
t <sub>HZCE</sub>	CE HIGH to High-Z <sup>[11, 12]</sup>	-	5	_	6	_	6	ns
t <sub>PU</sub>	CE LOW to Power Up	0	-	0	-	0	-	ns
t <sub>PD</sub>	CE HIGH to Power Down	-	10	-	12	_	15	ns
t <sub>DBE</sub>	Byte Enable to Data Valid	-	5	-	6	-	7	ns
t <sub>LZBE</sub>	Byte Enable to Low-Z	0	-	0	-	0	-	ns
t <sub>HZBE</sub>	Byte Disable to High-Z	-	5	_	6	_	7	ns
Write Cycle	[13, 14]				•	•		
t <sub>WC</sub>	Write Cycle Time	10	_	12	_	15	-	ns
t <sub>SCE</sub>	CE LOW to Write End	7	-	8	-	10	-	ns
t <sub>AW</sub>	Address Setup to Write End	7	-	8	-	10	-	ns
t <sub>HA</sub>	Address Hold from Write End	0	-	0	-	0	-	ns
t <sub>SA</sub>	Address Setup to Write Start	0	-	0	-	0	-	ns
t <sub>PWE</sub>	WE Pulse Width	7	-	8	-	10	-	ns
t <sub>SD</sub>	Data Setup to Write End	5	-	6	-	7	-	ns
t <sub>HD</sub>	Data Hold from Write End	0	-	0	_	0	_	ns
t <sub>LZWE</sub>	WE HIGH to Low-Z <sup>[12]</sup>	3	-	- 3 -		3	_	ns
t <sub>HZWE</sub>	WE LOW to High-Z <sup>[11, 12]</sup>	_	5		6	_	7	ns
t <sub>BW</sub>	Byte Enable to End of Write	7	-	8	-	10	-	ns

#### Notes

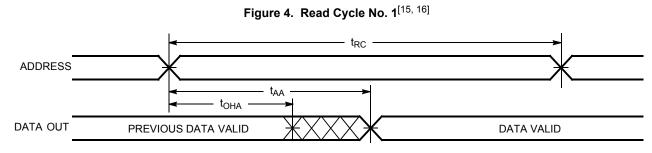
Notes
9. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
10. t<sub>POWER</sub> gives the minimum amount of time that the power supply must be at typical V<sub>CC</sub> values until the first memory access can be performed.
11. t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZBE</sub> and t<sub>HZWE</sub> are specified with a load capacitance of 5 pF as in part (d) of "AC Test Loads and Waveforms" on page 5.Transition is measured when the outputs enter a high impedance state.
12. At any temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZOE</sub> is less than t<sub>LZDE</sub>, t<sub>HZDE</sub> is less than t<sub>LZBE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any device.
13. The internal write time of the memory is defined by the overlap of CE LOW, and WE LOW. CE and WE must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data setup and hold timing must refer to the leading edge of the signal that terminates the write.
14. The minimum write cycle time for Write Cycle No. 3 (WE controlled, OE LOW) is the sum of t<sub>HZWE</sub> and t<sub>SD</sub>.

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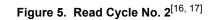


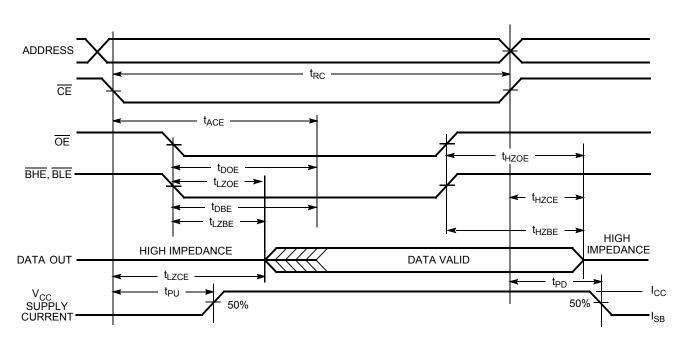
### **Switching Waveforms**

### **Read Cycle No. 1**



### Read Cycle No. 2 (OE Controlled)





#### Notes

15. <u>Device</u> is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$ , or both =  $V_{IL}$ .

16. WE is HIGH for Read cycle. 17. Address valid before or coincident with CE transition LOW.



### Switching Waveforms (continued)

Write Cycle No. 1 (CE Controlled)

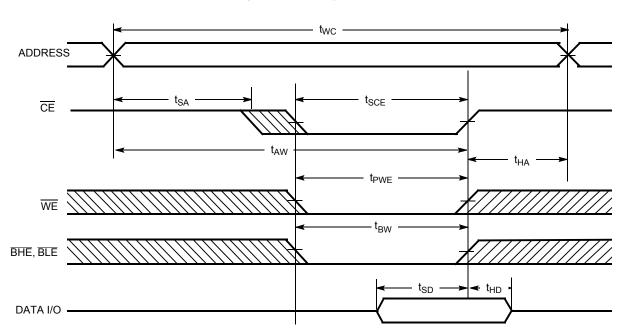
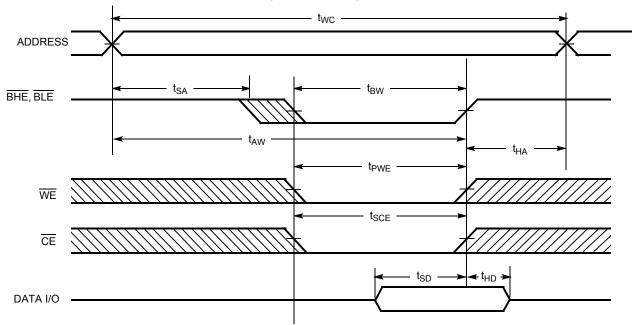


Figure 6. Write Cycle No. 1<sup>[18, 19]</sup>

## Write Cycle No. 2 (BLE or BHE Controlled)

Figure 7. Write Cycle No. 2



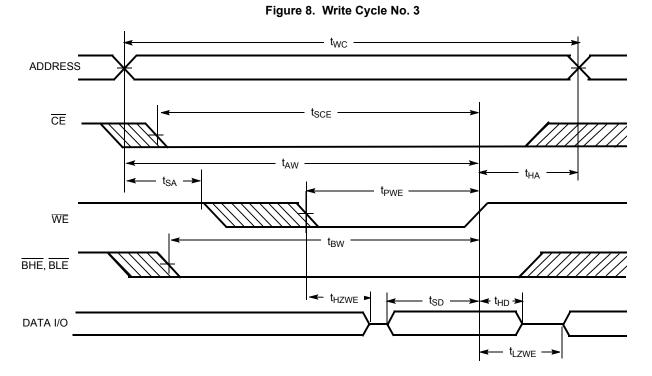
#### Notes

18. Data I/O is high-impedance if OE, or BHE, BLE, or both = V<sub>IH</sub>.
 19. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.



## Switching Waveforms (continued)





### Truth Table

CE	OE	WE	BLE	BHE	10 <sub>0</sub> –10 <sub>7</sub>	10 <sub>8</sub> –10 <sub>15</sub>	Mode	Power
Н	Х	Х	Х	Х	High-Z	High-Z	Power Down	Standby (I <sub>SB</sub> )
L	L	Н	L	L	Data Out	Data Out	Read All Bits	Active (I <sub>CC</sub> )
L	L	Н	L	Н	Data Out	High-Z	Read Lower Bits Only	Active (I <sub>CC</sub> )
L	L	Н	Н	L	High-Z	Data Out	Read Upper Bits Only	Active (I <sub>CC</sub> )
L	Х	L	L	L	Data In	Data In	Write All Bits	Active (I <sub>CC</sub> )
L	Х	L	L	Н	Data In	High-Z	Write Lower Bits Only	Active (I <sub>CC</sub> )
L	Х	L	Н	L	High-Z	Data In	Write Upper Bits Only	Active (I <sub>CC</sub> )
L	Н	Н	Х	Х	High-Z	High-Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )



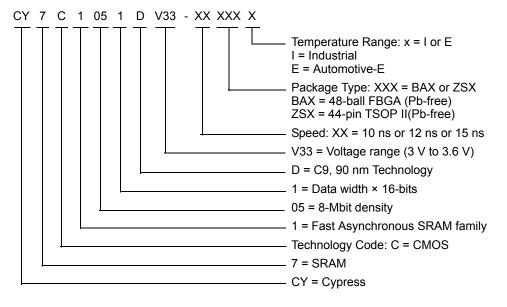
### **Ordering Information**

Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available. For a complete listing of all options, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products or contact your local sales representative. Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at http://www.cypress.com/go/datasheet/offices.

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1051DV33-10BAXI	51-85193	48-ball FBGA (Pb-free)	Industrial
	CY7C1051DV33-10ZSXI	51-85087	44-pin TSOP II (Pb-free)	
12	CY7C1051DV33-12BAXI	51-85193	48-ball FBGA (Pb-free)	Industrial
	CY7C1051DV33-12ZSXI	51-85087	44-pin TSOP II (Pb-free)	
15	CY7C1051DV33-15ZSXE	51-85087	44-pin TSOP II (Pb-free)	Auto-E <sup>[20]</sup>

Contact your local Cypress sales representative for availability of these parts.

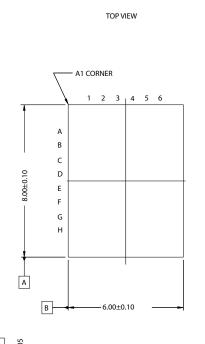
### **Ordering Code Definitions**

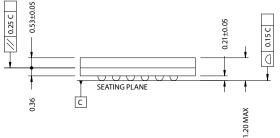


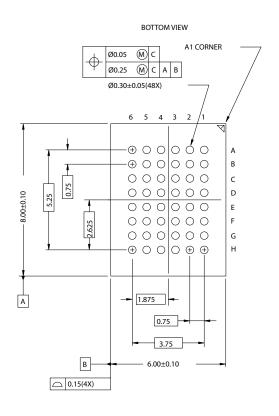


### **Package Diagrams**

Figure 9. 48-Ball FBGA (6 x 8 x 1.2 mm), 51-85193







REFERENCE JEDEC MO-207

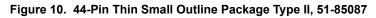
51-85193-\*B

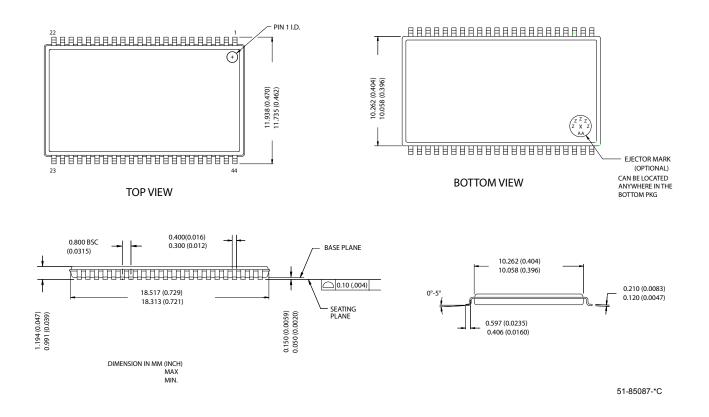
Note 20. Automotive product information is preliminary.

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## Package Diagrams (continued)









### Acronyms

Acronym	Description
CE	chip enable
CMOS	Complementary metal oxide semiconductor
I/O	Input/output
OE	output enable
SRAM	Static random access memory
SOJ	Small Outline J-Lead
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array

### **Document Conventions**

### Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	Volts
μA	microamperes
mA	milliamperes
mV	millivolts
mW	milliwatts
MHz	Megahertz
pF	pico Farad
°C	degree Celcius
W	Watts



## **Document History Page**

Document Title: CY7C1051DV33, 8-Mbit (512 K × 16) Static RAM Document Number: 001-00063						
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change		
**	342195	See ECN	PCI	New Data Sheet		
*A	380574	See ECN	SYT	Redefined I <sub>CC</sub> values for Com'l and Ind'l temperature ranges $I_{CC}$ (Com'l): Changed from 110, 90 and 80 mA to 110, 100 and 95 mA for 8, 10 and 12 ns speed bins respectively $I_{CC}$ (Ind'l): Changed from 110, 90 and 80 mA to 120, 110 and 105 mA for 8, 10 and 12 ns speed bins respectively Changed the Capacitance values from 8 pF to 10 pF on Page # 3		
*В	485796	See ECN	NXR	Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Removed -8 and -12 Speed bins from product offering, Removed Commercial Operating Range option, Modified Maximum Ratings for DC input voltage from -0.5 V to -0.3 V and $V_{CC}$ + 0.5 V to $V_{CC}$ + 0.3 V Changed the Description of I <sub>IX</sub> from Input Load Current to Input Leakage Current. Changed t <sub>HZBE</sub> from 5 ns to 6 ns Updated footnote #7 on High-Z parameter measurement Added footnote #11 Updated the Ordering Information table and Replaced Package Name column with Package Diagram.		
*C	866000	See ECN	NXR	Changed ball E3 from V <sub>SS</sub> to NC in FBGA pin configuration		
*D	1513285	See ECN	VKN/AESA	Converted from preliminary to final Changed t <sub>HZBE</sub> from 6 ns to 5 ns for 10 ns speed bin Added 12 ns speed bin Changed t <sub>OHA</sub> spec from 3 ns to 2.5 ns Updated Ordering information table		
*E	2911009	04/12/10	VKN	Replaced 48-Ball (7 x 8.5 x 1.2 mm) FBGA with 48-Ball (6 x 8 x 1.2mm) FBGA, Updated Package diagrams, Updated ordering information.		
*F	3086522	11/15/2010	PRAS	Included Auto-E information (preliminary) in Ordering Information.		
*G	3112625	12/16/2010	AJU	Added Ordering Code Definitions.		



### Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

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Interface	cypress.com/go/interface	
Lighting & Power Control	cypress.com/go/powerpsoc	
	cypress.com/go/plc	
Memory	cypress.com/go/memory	
Optical & Image Sensing	cypress.com/go/image	
PSoC	cypress.com/go/psoc	
Touch Sensing	cypress.com/go/touch	
USB Controllers	cypress.com/go/USB	
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