CY7C144 CY7C145

# 8K x 8/9 Dual-Port Static RAM with SEM, INT, BUSY

Features

- True dual-ported memory cells that enable simultaneous reads of the same memory location
- 8K x 8 organization (CY7C144)
- 8K x 9 organization (CY7C145)
- 0.65-micron complementary metal oxide semiconductor (CMOS) for optimum speed and power
- High speed access: 15 ns
- Low operating power: I_{CC} = 160 mA (max.)
- Fully asynchronous operation
- Automatic power-down
- Transision transistor logic (TTL) compatible
- Master/Slave select pin enables bus width expansion to 16/18 bits or more
- Busy arbitration scheme provided
- Semaphores included to permit software handshaking between ports
- $\overline{INT}$ flag for port-to-port communication
- Available in 68-pin plastic leaded chip carrier (PLCC), 64-pin and 80-pin thin quad plastic flatpack (TQFP)
- Pb-free packages available

Functional Description

The CY7C144 and CY7C145 are high speed CMOS 8K x 8 and 8K x 9 dual-port static RAMs. Various arbitration schemes are included on the CY7C144/5 to handle situations when multiple processors access the same piece of data. Two ports are provided permitting independent, asynchronous access for reads and writes to any location in memory. The CY7C144/5 can be used as a standalone 64/72-Kbit dual-port static RAM or multiple devices can be combined in order to function as a 16/18-bit or wider master/slave dual-port static RAM. An M/$\overline{S}$ pin is provided for implementing 16/18-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: chip enable ($\overline{CE}$), read or write enable (R/W), and output enable ($\overline{OE}$). Two flags, BUSY and INT, are provided on each port. BUSY signals that the port is trying to access the same location currently being accessed by the other port. The interrupt flag ($\overline{INT}$) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power down feature is controlled independently on each port by a chip enable ($\overline{CE}$) pin or $\overline{SEM}$ pin.

Logic Block Diagram
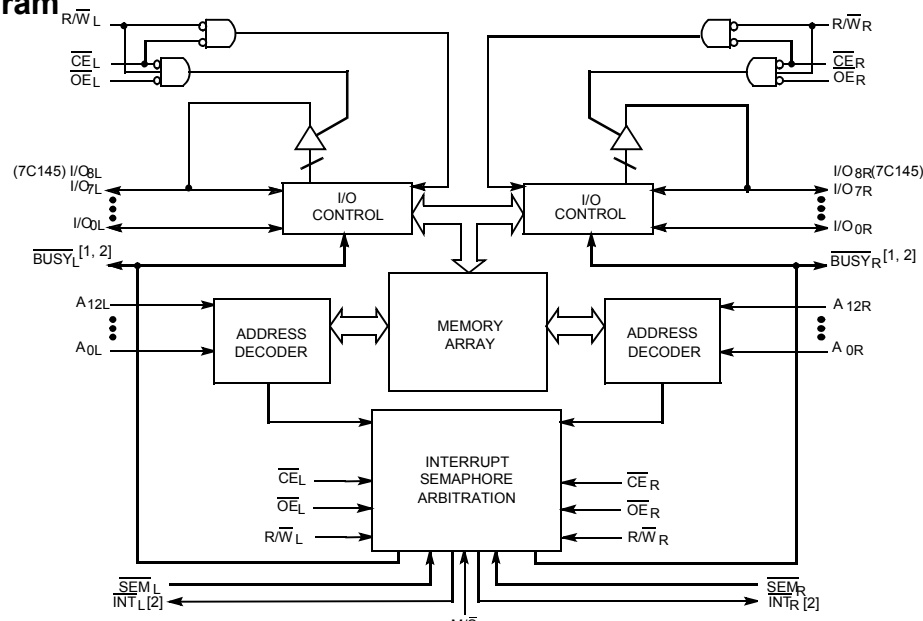
Notes
1. $\overline{BUSY}$ is an output in master mode and an input in slave mode.
2. Interrupt: push-pull output and requires no pull-up resistor.

[+] Feedback

Contents

Pin Configuration

Figure 1. 68-Pin PLCC (Top View)

Figure 2. 64-Pin TQFP (Top View)

Figure 3. 80-Pin TQFP (Top View)

Table 1. Selection Guide

Description	7C144-15 7C145-15	7C144-25	7C144-55	Unit
Maximum Access Time	15	25	55	ns
Maximum Operating Current	220	180	160	mA
Maximum Standby Current for I_{SB1}	60	40	30	mA

Table 2. Pin Definitions

Left Port	Right Port	Description
$I/O_{0L-7L(8L)}$	$I/O_{0R-7R(8R)}$	Data bus input/output
A_{0L-12L}	A_{0R-12R}	Address lines
$\overline{CE}_L$	$\overline{CE}_R$	Chip enable
$\overline{OE}_L$	$\overline{OE}_R$	Output enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write enable
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore enable. When asserted LOW, allows access to eight semaphores. The three least significant bits of the address lines will determine which semaphore to write or read. The I/O_0 pin is used when writing to a semaphore. Semaphores are requested by writing a 0 into the respective location.
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag. $\overline{INT}_L$ is set when right port writes location 1FFE and is cleared when left port reads location 1FFE. $\overline{INT}_R$ is set when left port writes location 1FFF and is cleared when right port reads location 1FFF.
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy flag
$M/\overline{S}$		Master or Slave select
V_{CC}		Power
GND		Ground

[+] Feedback

Architecture

The CY7C144/5 consists of a an array of 8 K words of 8/9 bits each of dual-port RAM cells, I/O and address lines, and control signals (CE, OE, R/W). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes or reads to the same location, a BUSY pin is provided on each port. Two interrupt (INT) pins can be used for port-to-port communication. Two semaphore (SEM) control pins are used for allocating shared resources. With the M/S pin, the CY7C144/5 can function as a Master (BUSY pins are outputs) or as a slave (BUSY pins are inputs). The CY7C144/5 has an automatic power down feature controlled by CE. Each port is provided with its own output enable control (OE), which allows data to be read from the device.

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/W to guarantee a valid write. A write operation is controlled by either the OE pin (see Figure 8 on page 12) or the R/W pin (see Write Cycle No. 2 waveform). Data can be written to the device t_{HZOE} after the OE is deasserted or t_{HZWE} after the falling edge of R/W. Required inputs for non-contention operations are summarized in Table 3.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must be met before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port t_{DDD} after the data is presented on the other port.

Read Operation

When reading the device, the user must assert both the OE and CE pins. Data will be available t_{ACE} after CE or t_{DOE} after OE are asserted. If the user of the CY7C144/5 wishes to access a semaphore flag, then the SEM pin must be asserted instead of the CE pin.

Interrupts

The interrupt flag (INT) permits communications between ports.When the left port writes to location 1FFF, the right port's interrupt flag (INT_R) is set. This flag is cleared when the right port reads that same location. Setting the left port's interrupt flag (INT_L) is accomplished when the right port writes to location 1FFE. This flag is cleared when the left port reads location 1FFE. The message at 1FFF or 1FFE is user-defined. See Table 4 for input requirements for INT. INT_R and INT_L are push-pull outputs and do not require pull-up resistors to operate.

Busy

The CY7C144/5 provides on-chip arbitration to alleviate simultaneous memory location access (contention). If both ports' CEs are asserted and an address match occurs within t_{PS} of each other the Busy logic determines which port has access. If t_{PS} is violated, one port will definitely gain permission to the location, but it is not guaranteed which one. BUSY will be asserted t_{BLA} after an address match or t_{BLC} after CE is taken LOW. $BUSY_L$ and $BUSY_R$ in master mode are push-pull outputs and do not require pull-up resistors to operate.

Master/Slave

An M/S pin is provided in order to expand the word width by configuring the device as either a master or a slave. The BUSY output of the master is connected to the BUSY input of the slave. This enables the device to interface to a master device with no external components.Writing of slave devices must be delayed until after the BUSY input has settled. Otherwise, the slave chip may begin a write cycle during a contention situation.When presented a HIGH input, the M/S pin allows the device to be used as a master and therefore the BUSY line is an output. BUSY can then be used to send the arbitration outcome to a slave.

Semaphore Operation

The CY7C144/5 provides eight semaphore latches which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports.The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a 0 to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, SEM or OE must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value is available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a 0), it assumes control over the shared resource, otherwise (reads a 1) it assumes the right port has control and continues to poll the semaphore.When the right side has relinquished control of the semaphore (by writing a 1), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a 1 is written to cancel its request.

Semaphores are accessed by asserting SEM LOW. The SEM pin functions as a chip enable for the semaphore latches (CE must remain HIGH during SEM LOW). A_{0-2} represents the semaphore address. OE and R/W are used in the same manner as a normal memory access.When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a 0 is written to the left port of an unused semaphore, a 1 appears at the same semaphore address on the right port. That semaphore can now only be modified by the side showing 0 (the left port in this case). If the left port now relinquishes control by writing a 1 to the semaphore, the semaphore will be set to 1 for both sides. However, if the right port had requested the semaphore (written a 0) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. Table 5 shows sample semaphore operations.

When reading a semaphore, all eight/nine data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore is definitely obtained by one side or the other, but there is no guarantee which side controls the semaphore.

Initialization of the semaphore is not automatic and must be reset during initialization program at power-up. All Semaphores on both sides should have a one written into them at initialization from both sides to assure that they are free when needed.

Table 3. Non-Contending Read/Write

Inputs				Outputs	Operation
$\overline{CE}$	R/W	$\overline{OE}$	$\overline{SEM}$	I/O$_{0-7/8}$	
H	X	X	H	High Z	Power-down
H	H	L	L	Data out	Read data in semaphore
X	X	H	X	High Z	I/O lines disabled
H	⌐	X	L	Data in	Write to semaphore
L	H	L	H	Data out	Read
L	L	X	H	Data in	Write
L	X	X	L		Illegal condition

Table 4. Interrupt Operation Example (assumes $\overline{BUSY_L} = \overline{BUSY_R}$ = HIGH)

Function	Left Port					Right Port				
	R/W	$\overline{CE}$	$\overline{OE}$	A$_{0-12}$	$\overline{INT}$	R/W	$\overline{CE}$	$\overline{OE}$	A$_{0-12}$	$\overline{INT}$
Set left $\overline{INT}$	X	X	X	X	L	L	L	X	1FFE	X
Reset left $\overline{INT}$	X	L	L	1FFE	H	X	L	L	X	X
Set right $\overline{INT}$	L	L	X	1FFF	X	X	X	X	X	L
Reset right $\overline{INT}$	X	X	X	X	X	X	L	L	1FFF	H

Table 5. Semaphore Operation Example

Function	I/O$_{0-7/8}$ Left	I/O$_{0-7/8}$ Right	Status
No action	1	1	Semaphore free
Left port writes semaphore	0	1	Left port obtains semaphore
Right port writes 0 to semaphore	0	1	Right side is denied access
Left port writes 1 to semaphore	1	0	Right port is granted access to semaphore
Left port writes 0 to semaphore	1	0	No change. Left port is denied access
Right port writes 1 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore address
Right port writes 0 to semaphore	1	0	Right port obtains semaphore
Right port writes 1 to semaphore	1	1	No port accessing semaphore
Left port writes 0 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.[3]

Storage temperature ....−65 °C to +150 °C

Ambient temperature with
power applied..−55 °C to +125 °C

Supply voltage to ground potential .... −0.5 V to +7.0 V

DC voltage applied to outputs
in High Z state.. −0.5 V to +7.0 V

DC input voltage[4]... −0.5 V to +7.0 V

Output current into outputs (LOW) .... 20 mA

Static discharge voltage... >2001 V
(per MIL-STD-883, Method 3015)

Latch-up current .... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	5 V $\pm$ 10%
Industrial	−40 °C to +85 °C	5 V $\pm$ 10%

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		7C144-15 7C145-15		7C144-25		Unit
				Min	Max	Min	Max	
V_{OH}	Output HIGH voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4	–	2.4	–	V
V_{OL}	Output LOW voltage	V_{CC} = Min., I_{OL} = 4.0 mA		–	0.4	–	0.4	V
V_{IH}	Input HIGH voltage			2.2	–	2.2	–	V
V_{IL}	Input LOW voltage			–	0.8	–	0.8	V
I_{IX}	Input leakage current	GND $\leq V_I \leq V_{CC}$		−10	+10	−10	+10	µA
I_{OZ}	Output leakage current	Outputs disabled, GND $\leq V_O \leq V_{CC}$		−10	+10	−10	+10	µA
I_{CC}	Operating current	V_{CC} = Max., I_{OUT} = 0 mA Outputs disabled	Commercial	–	220	–	180	mA
			Industrial	–	–	–	190	
I_{SB1}	Standby current (Both ports TTL levels)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}[5]	Commercial	–	60	–	40	mA
			Industrial	–	–	–	50	
I_{SB2}	Standby current (One port TTL level)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}[5]	Commercial	–	130	–	110	mA
			Industrial	–	–	–	120	
I_{SB3}	Standby current (Both ports CMOS levels)	Both ports $\overline{CE}$ and $\overline{CE}_R \geq V_{CC}$ − 0.2 V, $V_{IN} \geq V_{CC}$ − 0.2 V or $V_{IN} \leq 0.2$ V, f = 0[5]	Commercial	–	15	–	15	mA
			Industrial	–	–	–	30	
I_{SB4}	Standby current (One port CMOS level)	One port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC}$ − 0.2 V, $V_{IN} \geq V_{CC}$ − 0.2 V or $V_{IN} \leq 0.2$ V, Active Port outputs, f = f_{MAX}[5]	Commercial	–	125	–	100	mA
			Industrial	–	–	–	115	

Notes
3. The Voltage on any input or I/O pin cannot exceed the power pin during power-up.
4. Pulse width < 20 ns.
5. f_{MAX} = 1/t_{RC} = All inputs cycling at f = 1/t_{RC} (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}

Electrical Characteristics
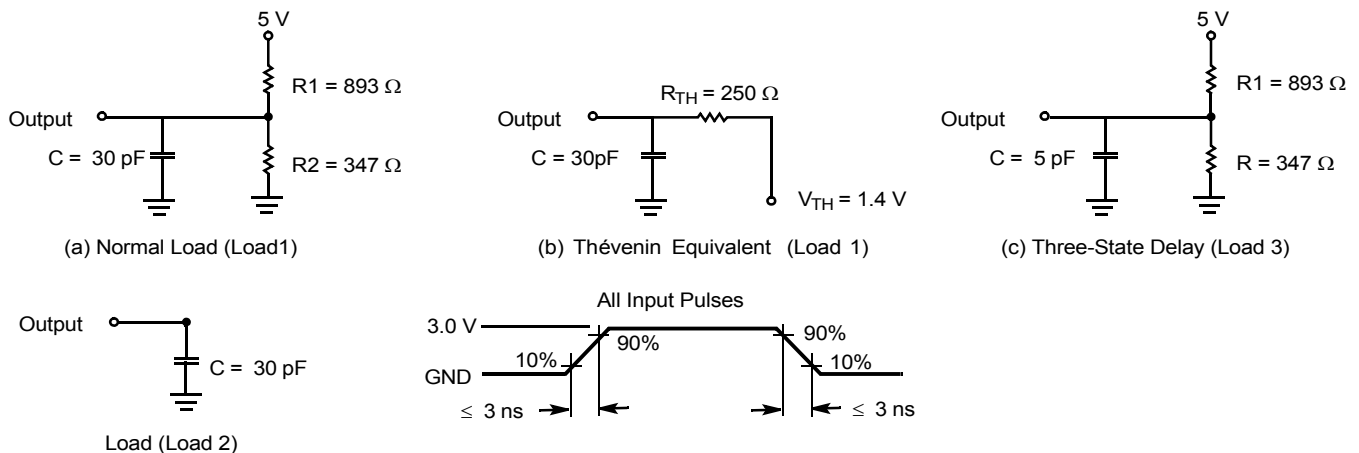
Over the Operating Range (continued)

Parameter	Description	Test Conditions		7C144-55 Min	7C144-55 Max	Unit
V_{OH}	Output HIGH voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4	–	V
V_{OL}	Output LOW voltage	V_{CC} = Min., I_{OL} = 4.0 mA		–	0.4	V
V_{IH}	Input HIGH voltage			2.2	–	V
V_{IL}	Input LOW voltage			–	0.8	V
I_{IX}	Input leakage vurrent	GND ≤ V_I ≤ V_{CC}		−10	+10	μA
I_{OZ}	Output leakage current	Outputs disabled, GND ≤ V_O ≤ V_{CC}		−10	+10	μA
I_{CC}	Operating current	V_{CC} = Max., I_{OUT} = 0 mA Outputs disabled	Commercial	–	160	mA
			Industrial	–	180	
I_{SB1}	Standby current (Both ports TTL levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[6]	Commercial	–	30	mA
			Industrial	–	40	
I_{SB2}	Standby current (One port TTL level)	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[6]	Commercial	–	100	mA
			Industrial	–	110	
I_{SB3}	Standby current (Both ports CMOS levels)	Both ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2 V, V_{IN} ≥ V_{CC} − 0.2 V or V_{IN} ≤ 0.2 V, f = 0[6]	Commercial	–	15	mA
			Industrial	–	30	–
I_{SB4}	Standby current (One port CMOS level)	One port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2 V, V_{IN} ≥ V_{CC} − 0.2 V or V_{IN} ≤ 0.2 V, Active Port outputs, f = f_{MAX}[6]	Commercial	–	90	mA
			Industrial	–	100	–

Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	10	pF
C_{OUT}	Output capacitance		15	pF

Figure 4. AC Test Loads and Waveforms

(a) Normal Load (Load1)   (b) Thévenin Equivalent (Load 1)   (c) Three-State Delay (Load 3)

Load (Load 2)

Note
6. f_{MAX} = 1/t_{RC} = All inputs cycling at f = 1/t_{RC} (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}

Switching Characteristics

Over the Operating Range[7]

Parameter	Description	7C144-15 7C145-15		7C144-25		7C144-55		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle								
t_{RC}	Read cycle time	15	–	25	–	55	–	ns
t_{AA}	Address to data valid	–	15	–	25	–	55	ns
t_{OHA}	Output hold from address change	3	–	3	–	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	15	–	25	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	10	–	15	–	25	ns
t_{LZOE}[8, 9,10]	$\overline{OE}$ Low to Low Z	3	–	3	–	3	–	ns
t_{HZOE}[8, 9,10]	$\overline{OE}$ HIGH to High Z	–	10	–	15	–	25	ns
t_{LZCE}[8, 9,10]	$\overline{CE}$ LOW to Low Z	3	–	3	–	3	–	ns
t_{HZCE}[8, 9,10]	$\overline{CE}$ HIGH to High Z	–	10	–	15	–	25	ns
t_{PU}[10]	$\overline{CE}$ LOW to power-up	0	–	0	–	0	–	ns
t_{PD}[10]	$\overline{CE}$ HIGH to power-down	–	15	–	25	–	55	ns
Write Cycle								
t_{WC}	Write cycle time	15	–	25	–	55	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	12	–	20	–	45	–	ns
t_{AW}	Address set-up to write end	12	–	20	–	45	–	ns
t_{HA}	Address hold from write end	2	–	2	–	2	–	ns
t_{SA}	Address set-up to write start	0	–	0	–	0	–	ns
t_{PWE}	Write pulse width	12	–	20	–	40	–	ns
t_{SD}	Data set-up to write end	10	–	15	–	25	–	ns
t_{HD}	Data hold from write end	0	–	0	–	0	–	ns
t_{HZWE}[9,10]	R/$\overline{W}$ LOW to High Z	–	10	–	15	–	25	ns
t_{LZWE}[9,10]	R/$\overline{W}$ HIGH to Low Z	3	–	3	–	3	–	ns
t_{WDD}[11]	Write pulse to data delay	–	30	–	50	–	70	ns
t_{DDD}[11]	Write data valid to read data valid	–	25	–	30	–	40	ns

Notes
7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OI}/I_{OH} and 30-pF load capacitance.
8. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
9. Test conditions used are Load 3.
10. This parameter is guaranteed but not tested.
11. For information on part-to-part delay through RAM cells from writing port to reading port, refer to Read timing with port-to-port delay waveform.

[+] Feedback

Switching Characteristics (continued)

Over the Operating Range[7]

Parameter	Description	7C144-15 7C145-15		7C144-25		7C144-55		Unit
		Min	Max	Min	Max	Min	Max	
Busy Timing[12]								
t_{BLA}	BUSY LOW from address match	–	15	–	20	–	30	ns
t_{BHA}	BUSY HIGH from address mismatch	–	15	–	20	–	30	ns
t_{BLC}	BUSY LOW from CE LOW	–	15	–	20	–	30	ns
t_{BHC}	BUSY HIGH from CE HIGH	–	15	–	20	–	30	ns
t_{PS}	Port set-up for priority	5	–	5	–	5	–	ns
t_{WB}	R/W LOW after BUSY LOW	0	–	0	–	0	–	ns
t_{WH}	R/W HIGH after BUSY HIGH	13	–	20	–	30	–	ns
t_{BDD}	BUSY HIGH to data valid	–	15	–	25	–	55	ns
Interrupt Timing[12]								
t_{INS}	INT set time	–	15	–	25	–	35	ns
t_{INR}	INT reset time	–	15	–	25	–	35	ns
Semaphore Timing								
t_{SOP}	SEM flag update pulse (OE or SEM)	10	–	10	–	20	–	ns
t_{SWRD}	SEM flag write to read time	5	–	5	–	5	–	ns
t_{SPS}	SEM flag contention window	5	–	5	–	5	–	ns

Note
12. Test conditions used are Load 2.

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[+] Feedback

Switching Waveforms

Figure 5. Read Cycle No. 1 (Either Port Address Access)[13, 14]
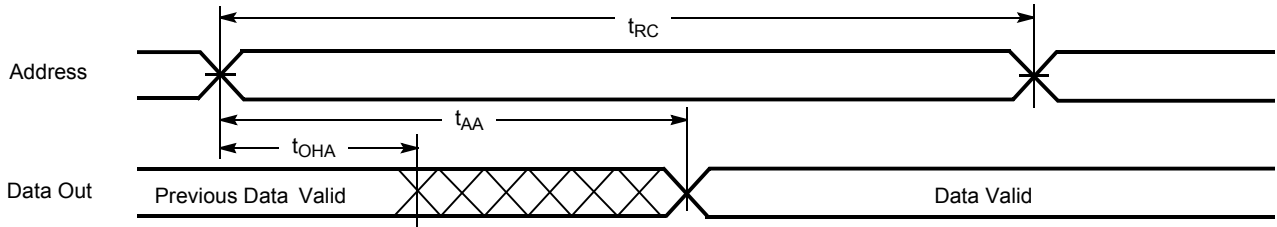
Figure 6. Read Cycle No. 2 (Either Port $\overline{CE}/\overline{OE}$ Access)[13, 15, 16]
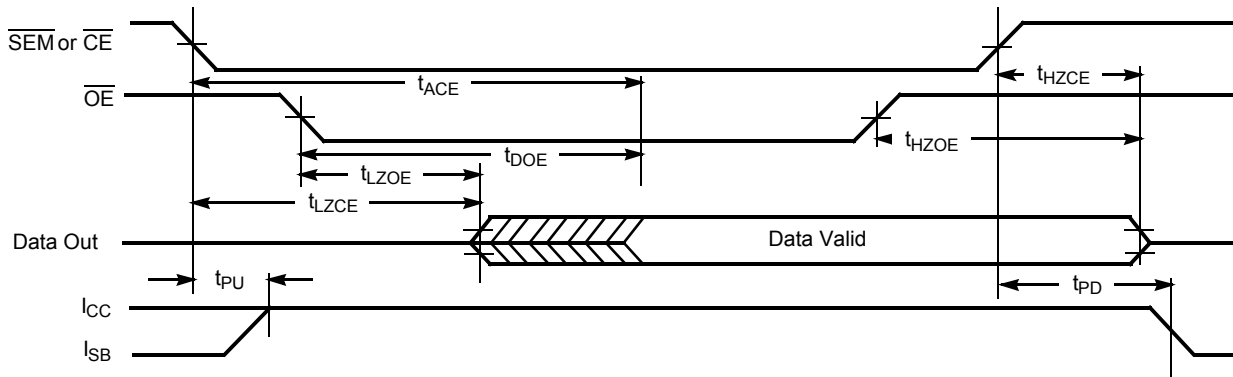
Figure 7. Read Timing with Port-to-Port Delay (M/$\overline{S}$=L)[17, 18]
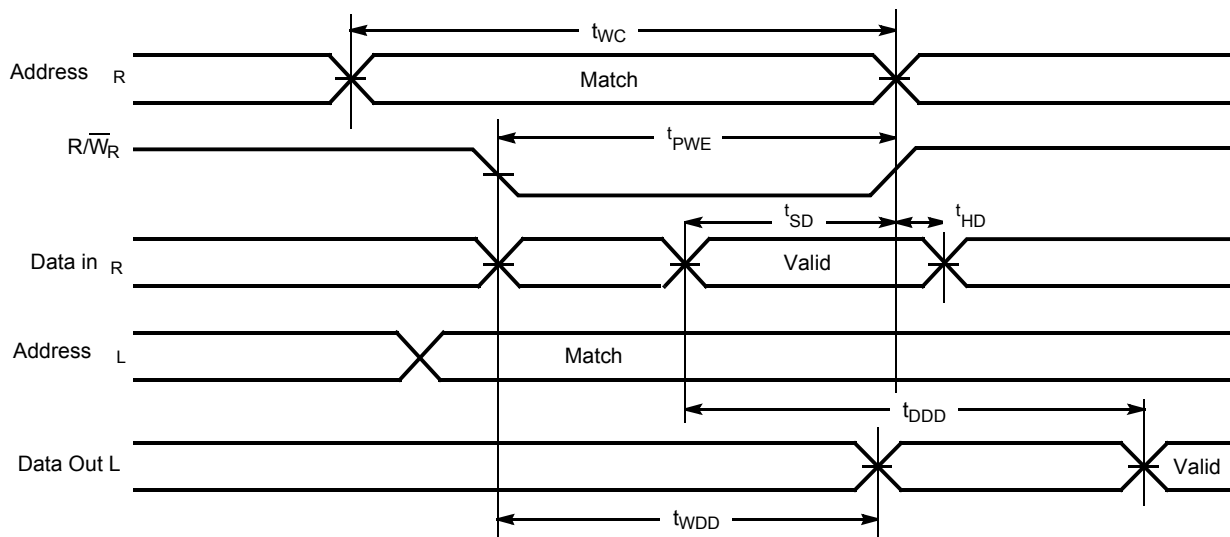
Notes
13. R/$\overline{W}$ is HIGH for read cycle.
14. Device is continuously selected $\overline{CE}$ = LOW and $\overline{OE}$ = LOW. This waveform cannot be used for semaphore reads.
15. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
16. $\overline{CE}_I$ = L, $\overline{SEM}$ = H when accessing RAM. $\overline{CE}$ = H, $\overline{SEM}$ = L when accessing semaphores.
17. $\overline{BUSY}$ = HIGH for the writing port.
18. $\overline{CE}_L$ = $\overline{CE}_R$ = LOW.

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[+] Feedback

Switching Waveforms (continued)

Figure 8. Write Cycle No. 1: $\overline{OE}$ Three-State Data I/Os (Either Port)[19, 20, 21]
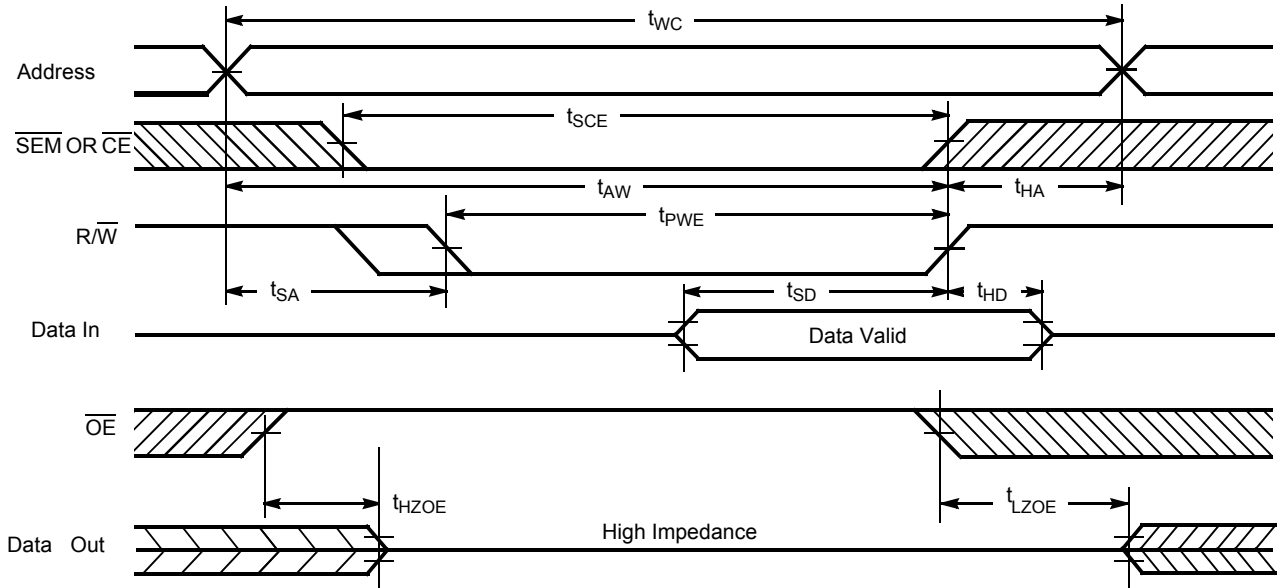
Figure 9. Write Cycle No. 2: R/$\overline{W}$ Three-State Data I/Os (Either Port)[19, 21, 22]
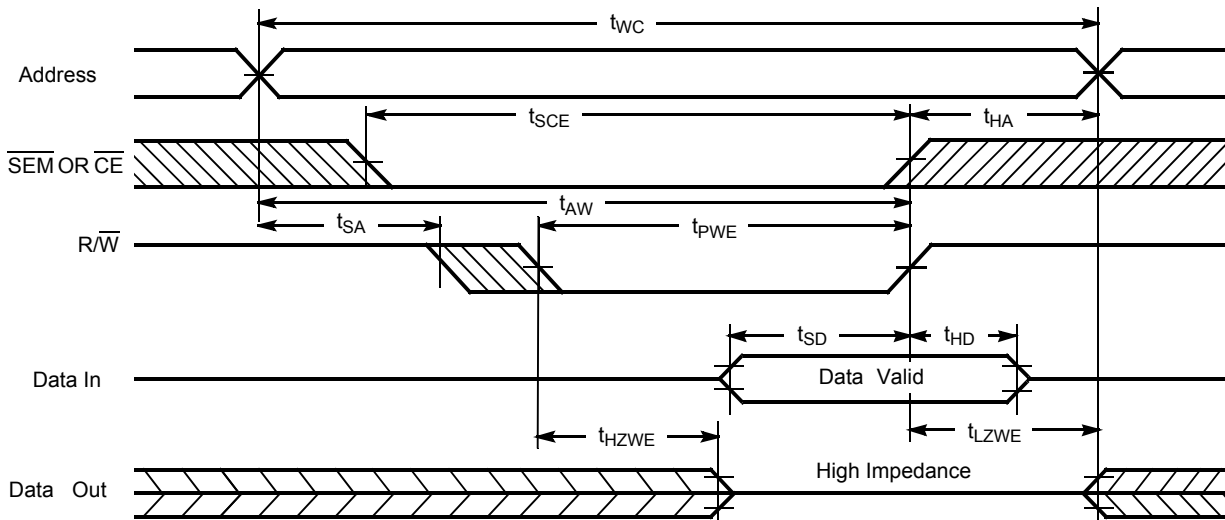
Notes
19. The internal write time of the memory is defined by the overlap of $\overline{CE}$ or $\overline{SEM}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write, and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
20. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or ($t_{HZWE} + t_{SD}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during a R/$\overline{W}$ controlled write cycle (as in this example), this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
21. R/$\overline{W}$ must be HIGH during all address transitions.
22. Data I/O pins enter high impedance when $\overline{OE}$ is held LOW during write.

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[+] Feedback

Switching Waveforms (continued)

Figure 10. Semaphore Read After Write Timing, Either Side[23]
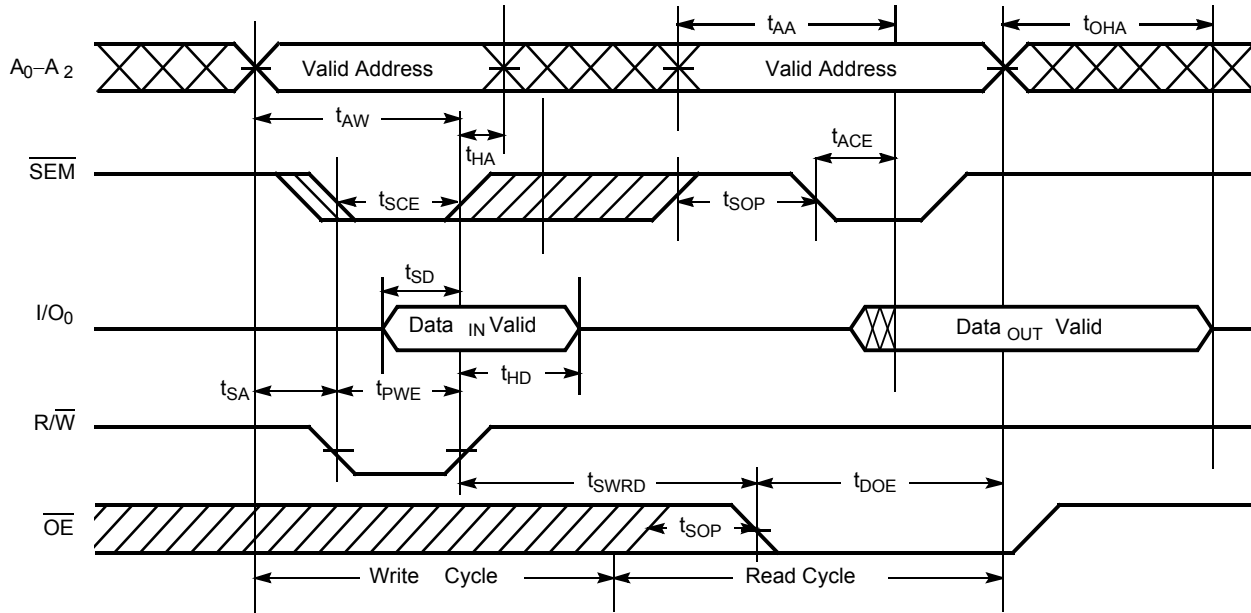
Figure 11. Semaphore Contention[24, 25, 26]
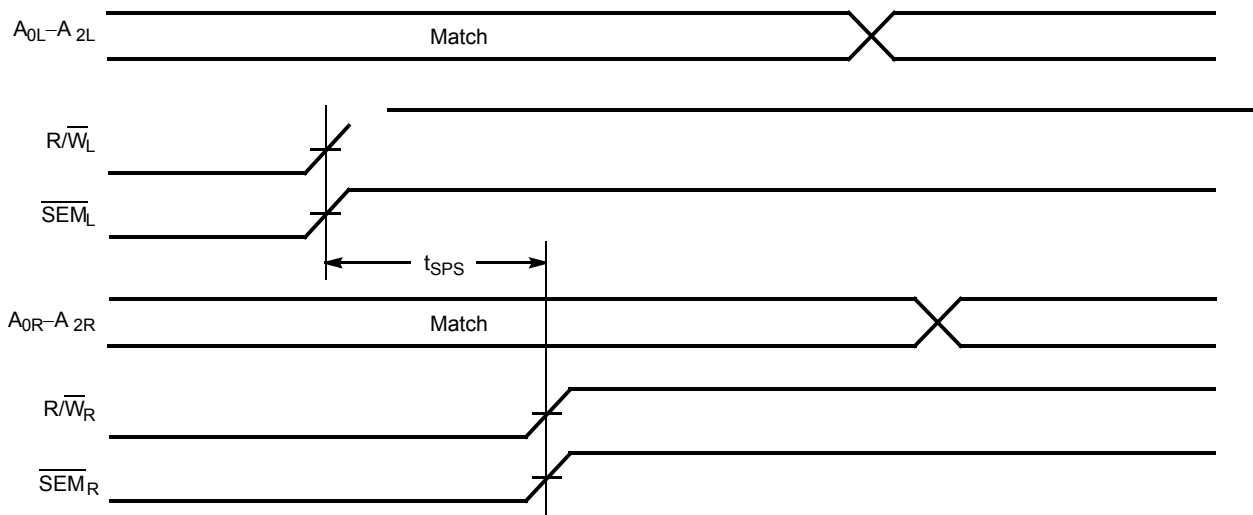
Notes
23. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).
24. I/O_{0R} = I/O_{0L} = LOW (request semaphore); $\overline{CE}_R$ = $\overline{CE}_L$ = HIGH
25. Semaphores are reset (available to both ports) at cycle start.
26. If t_{SPS} is violated, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Switching Waveforms (continued)

Figure 12. Read with $\overline{BUSY}$ (M/S=HIGH)[27]
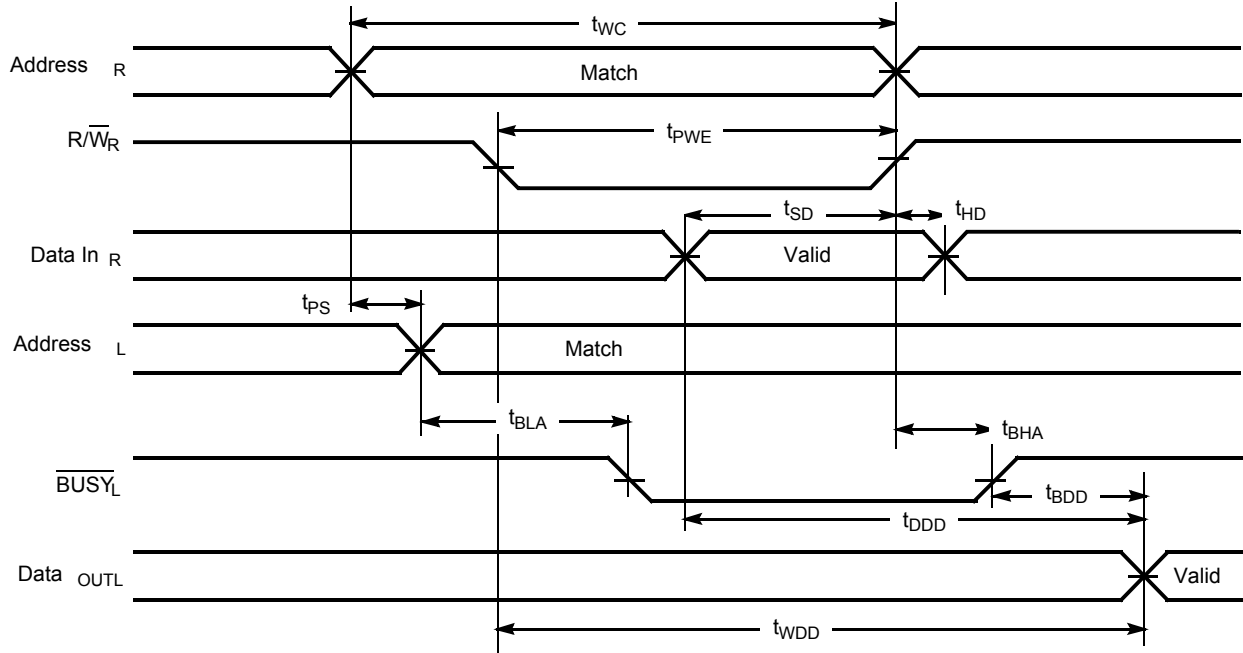
Figure 13. Write Timing with Busy Input (M/$\overline{S}$=LOW)

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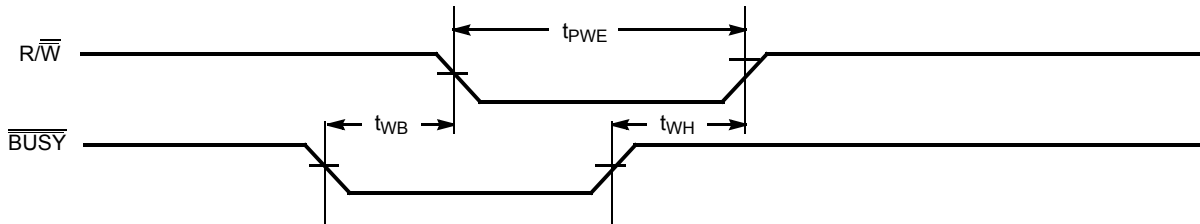
Switching Waveforms (continued)

Figure 14. Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)[28]

$\overline{CE_L}$ **Valid First:**

$\overline{CE_R}$ **Valid First:**
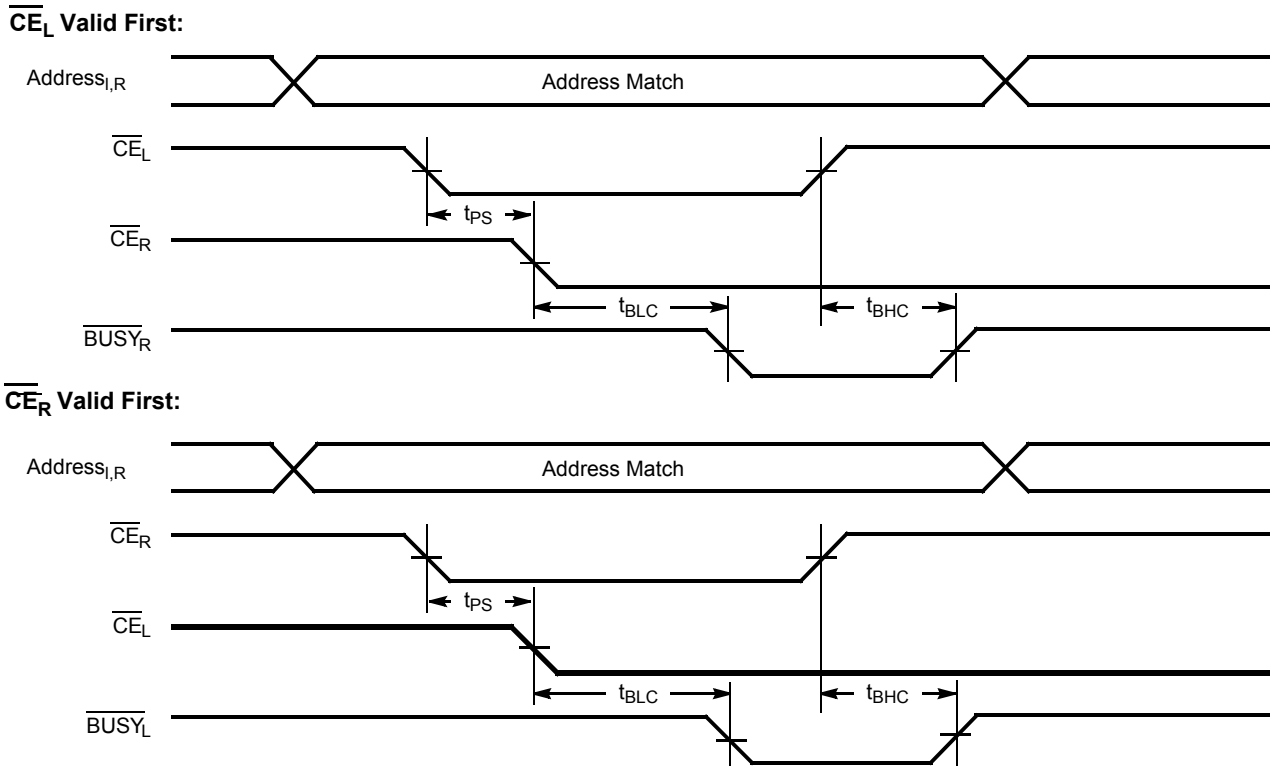
Figure 15. Busy Timing Diagram No. 2 (Address Arbitration)[28]

Left Address Valid First:

Right Address Valid First:
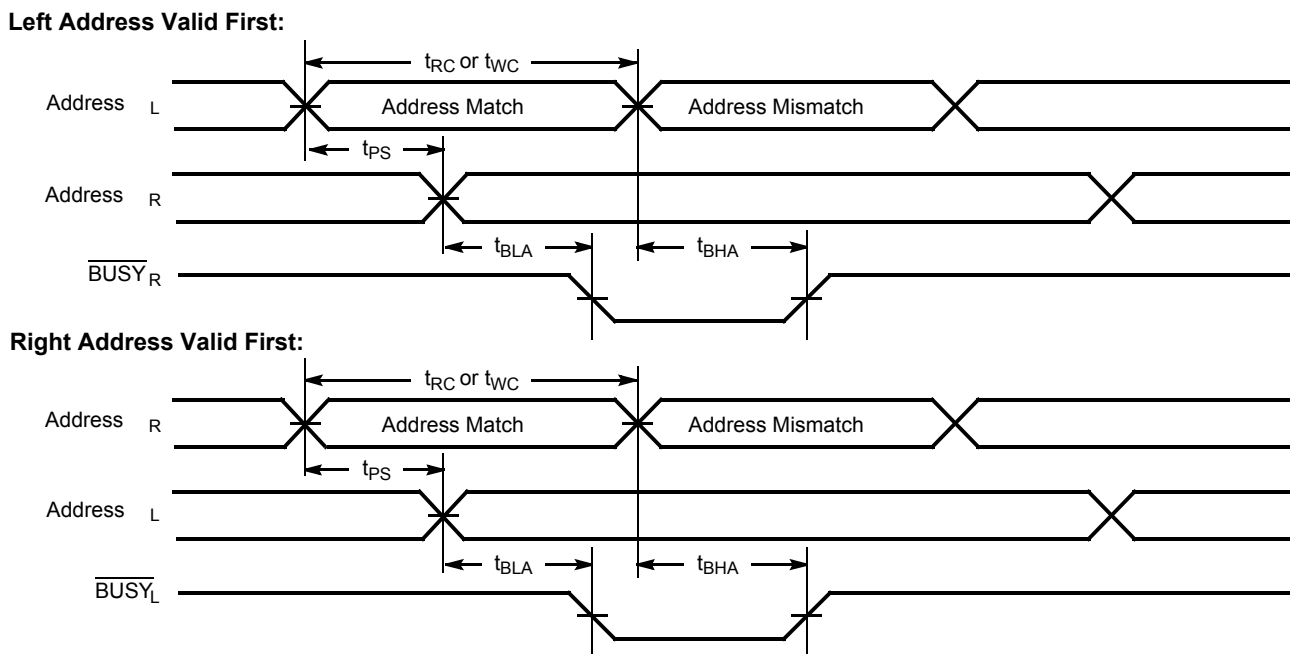
Note
28. If t_{PS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee on which side $\overline{BUSY}$ will be asserted.

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[+] Feedback

Switching Waveforms (continued)

Figure 16. Interrupt Timing Diagrams
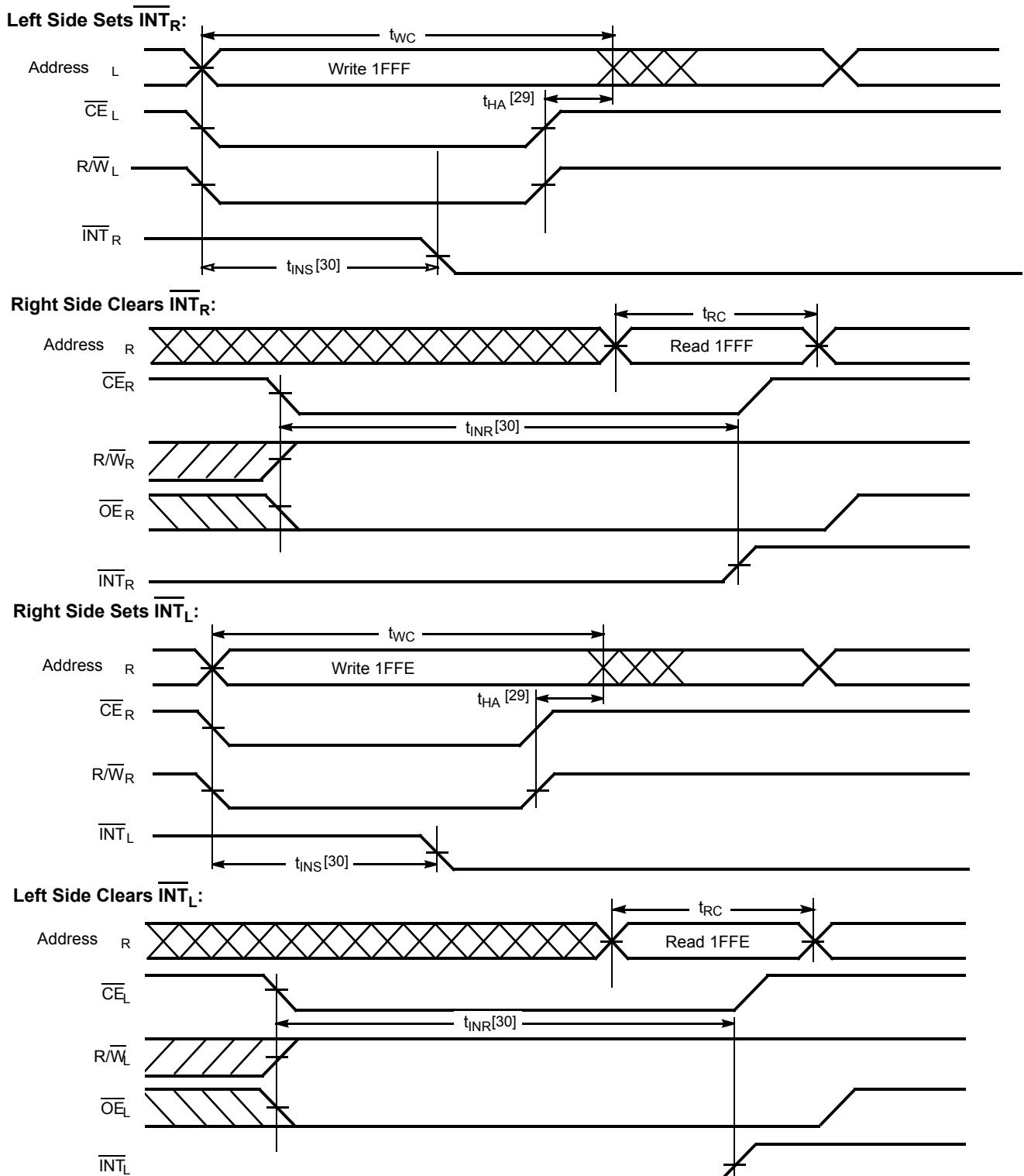
Notes
29. t_{HA} depends on which enable pin ($\overline{CE}_L$ or R/$\overline{W}_L$) is deasserted first.
30. t_{INS} or t_{INR} depends on which enable pin ($\overline{CE}_L$ or R/$\overline{W}_L$) is asserted last.

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Figure 17. Typical DC and AC Characteristics

Normalized Supply Current vs. Supply Voltage

Normalized Supply Current Vs. Ambient Temperature

Output Source Current Vs. Output Voltage

Normalized Access Time Vs. Supply Voltage

Normalized Access Time Vs. Ambient Temperature

Output Sink Current Vs. Output Voltage

Typical Power-on Current Vs. Supply Voltage

Typical Access Time Change Vs. Output Loading

Normalized I_{CC} vs. Cycle Time

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Ordering Information

8 K × 8 Dual-Port SRAM

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
15	CY7C144-15AXC	51-85046	64-pin Thin Quad Flat Pack (Pb-free)	Commercial
	CY7C144-15JXI	51-85005	68-pin Plastic Leaded Chip Carrier (Pb-free)	Industrial
	CY7C144-15AXI	51-85046	64-pin Thin Quad Flat Pack (Pb-free)	
25	CY7C144-25AXC	51-85046	64-pin Thin Quad Flat Pack (Pb-free)	Commercial
55	CY7C144-55AXC	51-85046	64-pin Thin Quad Flat Pack (Pb-free)	Commercial
	CY7C144-55JXC	51-85005	68-pin Plastic Leaded Chip Carrier (Pb-free)	
8 K × 9 Dual-Port SRAM				
15	CY7C145-15AXC	51-85065	80-pin Thin Quad Flat Pack (Pb-free)	Commercial

Ordering Code Definitions

```
CY7C   14X   -   XX   X X   X
```

Temperature Range: X = C or I
C = Commercial; I = Industrial

X: A= TQFP or J = PLCC

X: Pb-free (RoHS Compliant)

XX = Speed = 15 or 25 or 55 ns

14X = 144 or 145 = Part number identifier

CY7C = Cypress SRAMs
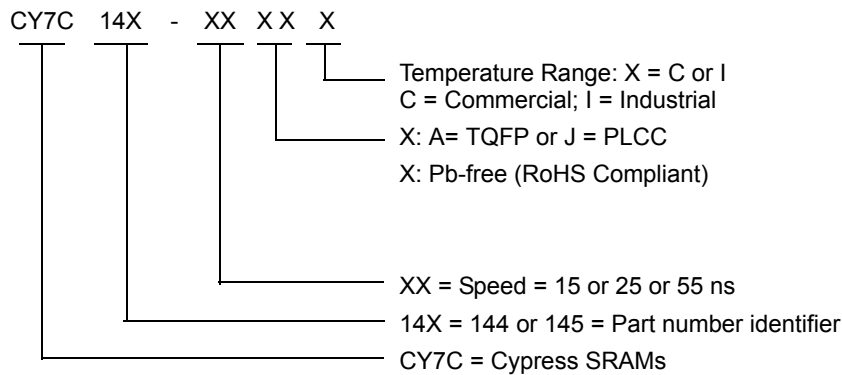
Package Diagrams

Figure 18. 64-Pin Thin Plastic Quad Flat Pack (14 x 14 x 1.4 mm), 51-85046
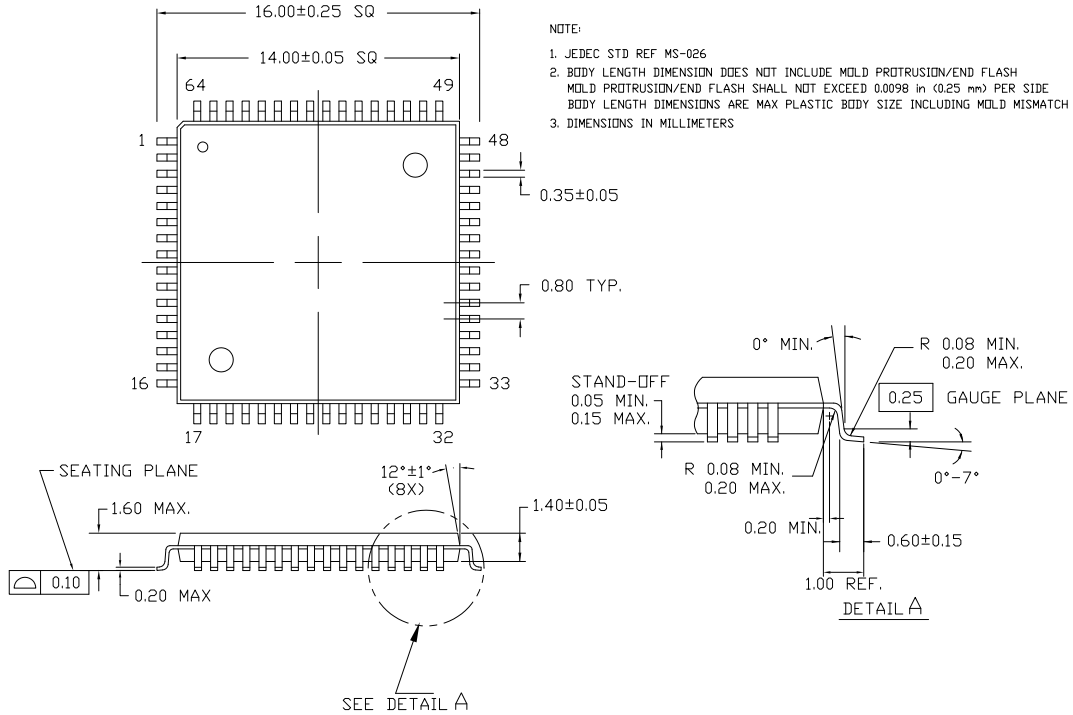
51-85046 *D

Package Diagrams (continued)

Figure 19. 80-Pin Thin Plastic Quad Flat Pack, 51-85065
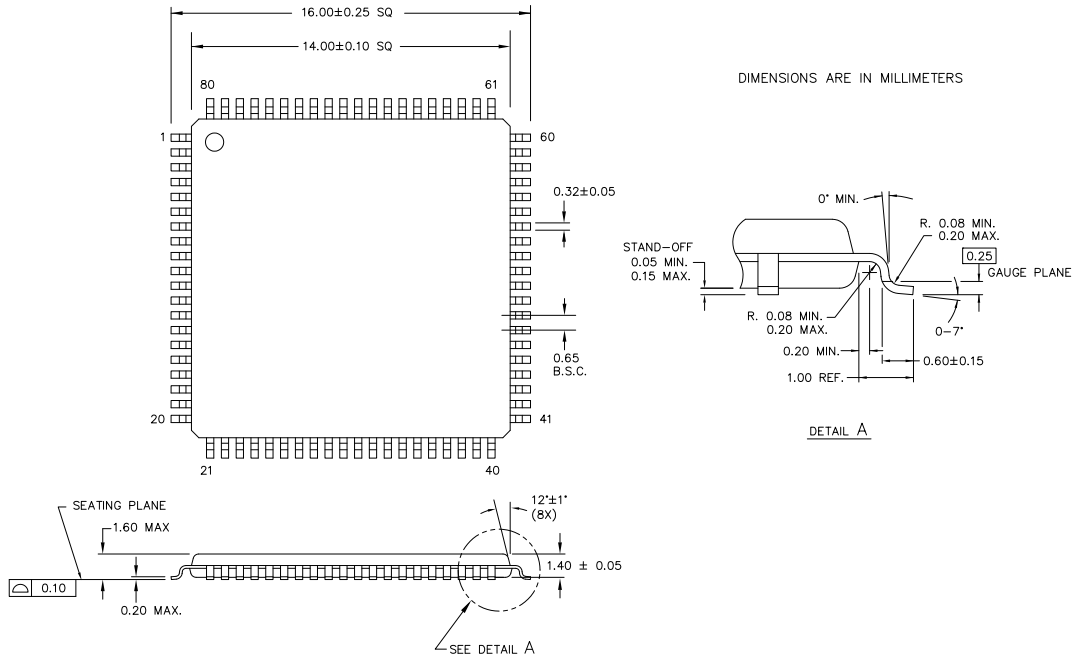
51-85065 *C

Figure 20. 68-Pin Plastic Leaded Chip Carrier, 51-85005

51-85005 *B

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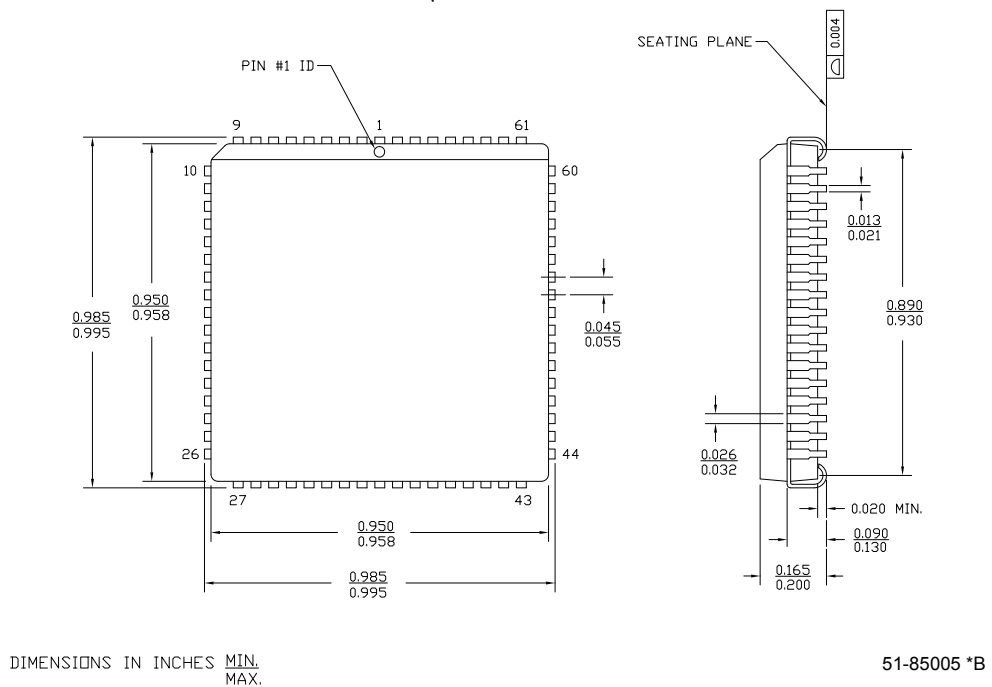
Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
TQFP	thin quad plastic flatpack
I/O	input/output
SRAM	static random access memory
PLCC	plastic leaded chip carrier
TTL	transistion transistor logic

Document Conventions

Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	Volts
µA	micro Amperes
mA	milli Amperes
Ω	Ohms
mV	milli Volts
MHz	Mega Hertz
pF	pico Farad
W	Watts
°C	degree Celcius

Document History Page

Document Title: CY7C144, CY7C145 8K x 8/9 Dual-Port Static RAM with Sem, Int, Busy
Document Number: 38-06034

Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	110175	SZV	09/29/01	Change from Spec number: 38-00163 to 38-06034
*A	122285	RBI	12/27/02	Power up requirements added to Maximum Ratings Information
*B	236752	YDT	See ECN	Removed cross information from features section, added CY7C144-15AI to ordering information section
*C	393320	YIM	See ECN	Added Pb-free Logo Added Pb-free parts to ordering information: CY7C144-15AXC, CY7C144-15JXC, CY7C144-15AXI, CY7C144-25AXC, CY7C144-55AXC, CY7C144-55JXC, CY7C145-15AXC, CY7C145-35JXC
*D	2623658	VKN/PYRS	12/17/2008	Added CY7C144-15JXI in the Ordering information table
*E	2699693	VKN/PYRS	04/29/2009	Corrected defective Logic Block diagram, Pinouts and Package diagrams
*F	2896210	RAME	03/22/2010	Updated Ordering Information Updated Package Diagrams
*G	3054633	ADMU	10/11/2010	Updated Ordering Information and added Ordering Code Definitions.
*H	3099184	ADMU	12/02/2010	Removed parts: CY7C144-55AC & CY7C144-55JC Removed speed bin -35 Updated as per new template Added Acronyms and Units of Measure table Added Ordering Code Definitions Updated all footnotes as per new template

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